Electromigration Behavior Of Electrotech Al(Cu) Versus CVD W Vias

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ABSTRACT

The electromigration behavior of Electrotech aluminum-copper (Al-Cu) vias is compared to that of Chemical Vapor Deposition (CVD) tungsten (W) vias. Al(Cu) vias were prepared by one of two processes: 1) the via was filled and then defined by Chemical Mechanical Polish (CMP) and 2) the via and top metal line were deposited in the same step (this is referred to as the "Sprint" process). CMP Al(Cu) via chains have a lower room temperature resistance than the CVD W via chains, although the temperature coefficient of resistance (TCR) is approximately the same. During electromigration testing, the resistance change with time of the W via chains exhibited more uniform resistance changes than the CMP Al(Cu) via chains. This had a direct impact on the shape parameter of the lognormal lifetime distribution, where σ was higher for the CMP Al(Cu) via chains. A closer examination of the failure distributions revealed the need to describe the CMP Al(Cu) via lifetimes by a three-parameter lognormal distribution as opposed to the conventional two-parameter lognormal distribution. Failure analysis of the CMP Al(Cu) samples indicated electromigration failures downstream from the via in the direction of the electron flow. Samples prepared by the Sprint process showed > 5x electromigration lifetime improvement as compared to either the CVD W or CMP Al(Cu) via samples.

I. INTRODUCTION

Chemical Vapor Deposition (CVD) W vias are known to result in decreased electromigration lifetimes as compared to planar interconnects, especially when the distance between vias is large (i.e., ≥300 μm) [1]. This has been shown for composite structures, where the interconnection metallurgy consists of a titanium-aluminum copper-titanium (Ti-AlCu-Ti) laminate. For example, Figure 1 indicates that at a test condition of 250 °C and 1 MA/cm^2, the measured lifetime of a W stud chain with a Ti-Al(0.5wt.%Cu)-Ti metallurgy is 50x smaller than that of a single level stripe with the same metallurgy. The reduction in lifetime for the W stud chain is a result of W acting as a diffusion barrier, preventing Cu from being replenished to the cathode [2,3,4]. As reported by Blech [5], however, the accumulation of Al atoms at the anode end of the conductor results in a stress gradient that opposes the electromigration driving force. When the distance between vias is short compared to the threshold product, $(jL)_c$, where j is the current density and L is the via spacing, little damage occurs in the adjacent Al-based lines. This phenomenon, known as the electromigration short-length effect, has important implications for lifetime measurements and projections to use conditions [6].

Typical metallization wiring schemes contain a wide variety of via spacings. One obvious solution to the W flux divergence problem would be to make all the W via spacings less than the critical length for a given current density. This solution, however, would increase the number of vias in the Integrated Circuit (IC) chip and would result in lower yield and possibly higher defect-driven reliability failures. A second possible solution would be to replace W with Al(Cu); this might (1) lower the via resistance, (2) create a Cu reservoir and (3) allow for a continuous path for Cu and Al diffusion throughout the metallization. This is made possible due to the existence of new Al(Cu) deposition schemes that involve improving the Al(Cu) mobility, resulting in satisfactory via fill for aspect ratios as high as 3:1 (feature height:feature width). One such new deposition scheme is provided by Electrotech, although the exact details of the means for increasing this mobility are not known to the authors.

The electromigration behavior of two varieties of sputtered Electrotech (ET) Al(Cu) vias has been determined and compared to CVD W vias. In the first, the via was filled and then defined by Chemical Mechanical Polish (CMP), while in the second, the via and top metal were deposited in the same step (see Figure 2). The latter process is referred to as the "Sprint" process.

II. PROCESS DESCRIPTIONS

Nominal four-layered (typically 25 nm Ti/950 nm Al(Cu)/25 nm Ti/40 nm TiN) samples were deposited in a single wafer Varian M2000 sputtering tool onto 125 mm diameter oxidized silicon (Si) substrates with a substrate temperature of 100 °C. The Al(Cu) was sputtered at 8 kW DC (direct current magnetron) in a 1.6 Pa (12 mTorr) high purity Ar plasma from an ultra-pure pre-alloyed target at a rate of 150 nm/min. Ti films were sputtered at 1 kW RF (13.56 MHz radio frequency) in a 1.6 Pa (12 mTorr) high purity Ar (99.999% Ar) plasma from an ultra-pure Ti (99.999%) target yielding a typical rate of 6 nm/min. TiN was reactively sputtered at 6 kW DC from a Ti target in a 15% N_2 (99.999%) - 85% Ar (99.999%) ambient. A total pressure of 1.33 Pa (10 mTorr) and a DC substrate bias of 100 V were used. Following blanket metal deposition fine lines were fabricated using optical lithography and reactive ion etching (RIE: in BCl_3-Cl_2-$CHCl_3$) forming lines 1.4-2.0 μm wide. Patterned wafers were annealed at 400 °C for

1 hr in forming gas (90% N_2-10% H_2) and coated with ≈ 1 μm (over the metal) of planar SiO_2. As a result of this anneal, Al and Ti react to form $TiAl_3$ [7,8]. Contact and via holes were subsequently opened in the sputtered oxide with a standard dry etch process that typically removed the $TiAl_3$ ($TiAl_3$ / TiN) layer beneath the via. Multi-level samples, consisting of two sputtered 4-layered films connected by W interlevel studs, were fabricated. The W was deposited by CVD in a Genus 8402 reactor onto a sputtered 40 nm Ti / 40 nm TiN seed layer and patterned by an etch back process. Al(Cu) interlevel studs were also fabricated using one of two processes; (1) Process I: the vias were filled with sputtered Electrotech Al(Cu), resulting in a planar blanket metal level which was subsequently removed by Al CMP and (2) Process II (Sprint): in which the via and metal 2 (M2) level were deposited in the same step forming a continuous via to M2 structure. The vias were initially lined with 40 nm Ti or 40 nm Ti / 40 nm TiN for both Process I and Process II. (See Figure 2 for schematic cross sections.)

III. EXPERIMENT

This report is based on the electromigration testing of two structures having lateral extrusion monitors 1 μm from the current-carrying lines. The first is a two level chain, referred to as the CK4_MAC1B via chain (Figure 3). It consists of 1.4 μm-wide metal 1 (M1) and metal 2 (M2) lines, with four 1.0x1.0 μm^2 vias. There are two pairs of vias, where the distance between vias measures 8 μm on M1 and 300 μm on M2. The second is a length dependent electromigration (LDEM) chain that alternates between M1 and M2 in increasing increments (Figure 4). The distance between vias on M1 and M2 starts at 3 μm and then repeats for 10, 30, 50, 100 and 300 μm. The width of the M1 and M2 interconnections is 2.0 μm and the vias are

1.6 μm in diameter.

Before any of the accelerated life tests were performed, the temperature coefficient of resistance (TCR) was obtained to assess the level of Joule heating. Electrical monitoring of the samples during electromigration testing was continuous, where failure was determined as an increase in resistance, an open, or an extrusion. A least squares algorithm was then used to fit the failure times to either the two-parameter or three-parameter lognormal distribution.

IV. RESULTS

This report is based on the electromigration testing of two jobs; A and B. Each job consists of samples having CVD W vias, as well as Al(Cu) vias prepared by the CMP or Sprint process. The Cu concentration in the vias is 0.5, 1.0 or 4.0 wt.% for job A, and 0.5 wt.% for job B. The CK4_MAC1B via chain and the LDEM via chain were used for job A, while only the CK4_MAC1B via chain was used for job B (see Table I for details).

A. Via Chain Resistance

One possible advantage of using Al(Cu) vias rather than W vias is lower via resistance. Table II shows the average resistances of the CK4_MAC1B via chain for jobs A and B. Although the sample sizes are small (11-12), the CVD W samples tend to have a higher resistance than the CMP Al(Cu) samples. Assuming that the differences in resistance are only due to differences in the via resistance, Table II indicates that a CVD W via is approximately 0.55 Ω more resistive than an Al(Cu) via for job A, and 1.76 Ω more resistive than an Al(Cu) via for job B. (These values were calculated using the average structure resistances listed in

Table II and accounting for the small number of vias (4) in the CK4_MAC1B via chain.)

B. Temperature Coefficient of Resistance (TCR)

The resistance of metals as a function of temperature is described by

$$R = R_0 \left[1 + \alpha (\Delta T)\right] \qquad \textbf{(1)}$$

where R is the sample resistance at the test temperature, R_0 is the sample resistance at a reference temperature, α is the temperature coefficient of resistance (TCR) and ΔT is the difference between the test temperature and the reference temperature. Table III indicates that the W and CMP Al(Cu) via samples have similar TCR values for both jobs A and B. A plot of resistance versus temperature is given in Figure 5 for the Al(Cu) and W via samples. Equation (1) is also used to determine the amount of Joule heating for a given set of temperature and current density conditions. Our data indicate that the Joule heating is < 5 °C at an M1 (M2) current density of 1 MA/cm² and an ambient temperature of 250 °C. Moreover, there is no significant difference in the amount of Joule heating between the CMP Al(Cu) and the CVD W via samples. This result may be attributed to the fact that the calculated Joule heating is a measure of the average Joule heating of the structure. The Joule heating at the W / Al(Cu) interface, which cannot be determined from resistance measurements since the interface resistance is much smaller than the overall structure resistance, may be quite high due to current crowding.

C. Resistance Change With Time During Electromigration Testing

As part of the electromigration testing procedure, the resistance of all samples was continuously monitored to detect electromigration-induced voiding. Increases in resistance are attributed to Al depletion at the cathode end of the chains [2,3]. In the case of CVD W vias, damage formation occurs downstream from the via in the Al-based interconnection [9]. The redundant $TiAl_3$ layers, which are more resistive than the Al(Cu) layers, allow the resistance of the chains to increase as the Al layers become depleted. (The resistivity of Al-0.5wt.%Cu is approximately 3.0 $\mu\Omega$-cm, while that of $TiAl_3$ is approximately 50 $\mu\Omega$-cm [10].)

Figures 6-9 illustrate the relative resistance change with time of the CK4_MAC1B via chains. In each case, a sample's resistance was not plotted when it became electrically open. During the early stages of the resistance change with time, all samples decreased in resistance. This decrease is not an electromigration-induced resistance change, but rather is caused by Cu precipitation as the Cu comes out of solution [11]. Figures 6 and 8 show the resistance shift vs. time for samples with CVD W vias from jobs A and B, respectively. Following the decrease in resistance, the W via samples linearly increased in resistance with respect to time. Typically, the W via samples increased 50-100% in resistance before opening. Figure 7 shows the resistance shift vs. time for samples from job A with CMP Al(1.0wt.%Cu) vias, while figure 9 shows the resistance shift vs. time for samples from job B with CMP Al(0.5wt.%Cu) vias. Figure 7 indicates that the Al(1.0wt.%Cu) via samples linearly increased in resistance but then fluctuated in resistance before open failure occurred. This "up and down" resistance behavior is not completely understood at this time, though a plausible explanation is the healing of electromigration-induced voids. The Al(0.5wt.%Cu) via samples from job B did not exhibit the same fluctuation in resistance as the Al(1.0wt.%Cu) via samples from job A. Once the Al(0.5wt.%Cu) via samples increased in resistance to a certain level (20-40%), they electrically opened. The difference in resistance behavior between the Al(1.0wt.%Cu) and Al(0.5wt.%Cu) via samples from jobs A and B, respectively, may have resulted from the difference in Cu concentration in the vias (1.0% versus 0.5%) as well as the difference in Cu concentration in the M1 and M2 interconnections (2.0% versus 0.5%). The fact that the W via samples increased to higher resistance levels than the CMP Al(Cu) via samples suggests that the former sustained more Al depletion before catastrophic failure occurred. Figures 8 and 9 also illustrate another important difference between the resistance change with time behavior of the CVD W and CMP Al(0.5wt.%Cu) via samples; the resistance change with time for the CVD W via samples shows little sample to sample variation, while that of the Al(0.5wt.%Cu) via samples shows much sample to sample variation. This has a direct effect on the shape parameter of the lognormal distribution, which we discuss in the next section.

D. Electromigration Lifetime Measurements

Electromigration experiments can be interpreted through drift velocity measurements or lifetime measurements. In the drift velocity case [5,12,13], the rate of mass depletion from the edge of a finite conductor is measured. In the lifetime measurement case [1,14,15], the usual convention is to determine the median time to failure, t_{50}, and shape parameter, σ, of the lognormal distribution. Failure is determined electrically as an increase in resistance, an open or an extrusion. The stress t_{50} and σ are determined by fitting the failure times to the following:

$$z = \frac{\ln(t_f) - \ln(t_{50})}{\sigma} \qquad \textbf{(2)}$$

where t_f is the time to failure and z is the inverse normal CDF (cumulative distribution function). In this study, we report lifetime statistics for two failure criteria; a) +20% resistance shift and b) electrical open.

The electromigration behavior of the CVD W and CMP Al(Cu) via samples are indicated in Table IV. The W via samples appear to show the tightest lognormal distributions (i.e. lowest σ values), with the one exception being the open fail criterion for job A. W via samples typically exhibit low σ values, except in situations where the threshold product, $(jL)_c$, is small compared to the distance between vias [6]. Lognormal CDF plots for the W via samples from job B are given in Figure 10, where the solid lines were generated from equation (2). Table IV also indicates that the CMP Al(Cu) via samples exhibit relatively high σ values for both a +20% shift and an open fail criterion. Lognormal CDF plots for the Al(4.0wt.%Cu) via samples are given in Figure 11, where the solid lines were generated from equation (2). The fact that the Al(4.0wt.%Cu) via samples have high σ values is indicated in Figure 11 by the steepness of the solid lines. (σ is simply the slope of the lognormal CDF plot.) Figure 11 also indicates that the electromigration lifetime distribution requires more than two parameters, since the failure data deviate from the two-parameter model (i.e. the solid lines) at low and high CDF values.

The use of a third parameter as part of an electromigration lifetime distribution has been previously reported [16], where the failure data are represented by a three-parameter lognormal distribution:

$$z = \frac{\ln(t_f - t_0) - \ln(t_{50} - t_0)}{\sigma} \qquad \textbf{(3)}$$

where t_0 is the incubation time, or the minimum time required before failure can occur. Figure 11 indicates excellent agreement between the three-parameter lognormal model, represented by the dashed lines, and the actual failure data for the Al(4.0wt.%Cu) via samples from job A.

Equation (3) found t_0 equal to 8.4 and 50.2 hours for a +20% resistance shift and an open fail criterion, respectively. Figure 12 shows a lognormal CDF plot for the CMP Al(0.5wt.%Cu) via samples from job B. The solid line was generated from equation (2), while the dashed line was generated from equation (3). Clearly, the three-parameter lognormal model fits the data better than the two-parameter lognormal model. Equation (3) found t_0 equal to 24.6 and 33.8 hours for a +20% resistance shift and an open fail criterion, respectively. Table V summarizes the electromigration results for the CMP Al(Cu) via samples according to equation (3). We will comment on the implications of a three-parameter lifetime distribution in the Discussion and Conclusions section, below.

Al(Cu) via samples prepared by the Sprint process behaved very differently than those prepared by the CMP process. This is indicated in Table VI, which compares the electromigration results for the CMP and Sprint Al(Cu) via samples as well as the CVD W via samples. Table VI indicates that the lifetime of the Sprint samples is significantly longer than the lifetime of either the CMP Al(Cu) or CVD W via samples. It should be pointed out that the Sprint samples typically had a thicker M2 layer than the CMP samples (see Table I). This is due to the difficulty in simultaneously obtaining uniform metal thicknesses and adequate via fill with the Sprint process. In any event, the thicker M2 should not affect the lifetime of job A samples since the LDEM chain can fail on either M1 or M2 (see Figure 4). The CK4_MAC1B via chain (Figure 3), however, is designed to fail in M2, so the lifetime of job B samples prepared by the Sprint process could have been affected by the thicker M2. For the purposes of this discussion, we assume that M2 for the Sprint samples is twice as thick as for the CMP samples. (This represents a worst case situation.) If we also assume that $t_{50} \propto j^{-2}$ at constant temperature, then half the current density, j, will result in a four-fold increase in lifetime, or t_{50}. (A j^{-2} lifetime dependency was first proposed by Black [17], and was later theoretically derived by Shatzkes and Lloyd [18]). The lifetime improvement for the job B samples prepared by the Sprint process is much greater than four times that of either the CMP Al(Cu) or CVD W via samples, so the enhanced lifetime could not have resulted only from a thicker M2. Due to an insufficient number of fails, we cannot accurately state the lifetime improvement of the Sprint samples as compared to the CMP Al(Cu) and CVD W via samples. A conservative estimate would place the improvement at > 5x for the structures tested in this study.

E. Failure Analysis

We compared the location of failures in the CK4_MAC1B via chain using 12 CMP Al(0.5wt.%Cu) via samples and 12 CVD W via samples. Each sample electrically opened before being removed from electromigration testing. Electron Beam Induced Current, or EBIC, was used to locate the failures in a Scanning Electron Microscope (SEM). The primary failure locations were found to be at or near vias #1 and #3 of the CK4_MAC1B via chain (see Figure 3). EBIC was unable to distinguish between failures in the vias or in the adjacent interconnects (i.e. M1 or M2). Table VII indicates the failure locations for the Al(0.5wt.%Cu) and W via samples, where most of the Al(0.5wt.%Cu) via samples failed at or near via #1, while most of the W via samples failed at or near via #3. As Table VII indicates, EBIC was unable to locate some of the fails.

In order to determine whether electromigration failures occurred in the vias or in the adjacent interconnects, SEM cross sections of several failed CK4_MAC1B via chains were generated. Since it is well known that electromigration-induced voiding in W via chains occurs in the Al-based interconnects [2,3,9], SEM cross sections of the CVD W via samples were not generated. Failures for the W via samples almost certainly occurred downstream from either via #1 or via #3 in the M2 interconnect (see Figure 3). No failures should have occurred in M1 since the distance between vias on M1 (8 μm) is much smaller than that on M2 (300 μm). (This is a direct result of the short-length effect [5]). SEM cross sections of the CMP Al(0.5wt.%Cu) via samples from job B indicate that failures occurred in the same place as expected for W via samples. That is, the failures occurred downstream from either via #1 or via #3 in the M2 interconnect. This is illustrated in Figure 13, which shows an electromigration open failure in the M2 line. It is interesting to note that this particular failure did not occur directly above via #1, but rather was displaced slightly downstream from the via. Figure 14 shows a failure for a different CMP Al(0.5wt.%Cu) via sample, where the void-open occurred even further downstream from via #1.

We also generated SEM cross sections of Al(0.5wt.%Cu) via samples prepared by the Sprint process that did not fail after > 1200 hours of electromigration testing. The samples were analyzed for voiding in the vicinity of the vias. None of the samples analyzed showed any indication of electromigration voiding, which is consistent with the electrical results.

V. DISCUSSION AND CONCLUSIONS

Typically, multi-level structures (Figures 3 and 4) fail earlier than single level metal lines because of the presence of abrupt material discontinuities in multi-level samples. These discontinuities cause current crowding and, in the case of W studs, also prevent Cu and Al from diffusing from one Al(Cu) line level to the next. In contrast, single level metal lines usually have an additional unlimited supply of Al and Cu atoms from adjacent large lines and pads that are not present in multi-level structures. The degradation of lifetimes measured for multi-level metallizations signifies the importance of choosing compatible materials for both the lines and studs. Joule heating, solute diffusion, electromigration and flux divergences at the stud / conductor interfaces must be considered.

In this paper the magnitude of the blocking sites was altered by replacing W with Al(Cu) vias. It appears that the flux divergence site may not be as complete with Al(Cu) vias as with W. The Al(Cu) vias would allow for both Al and Cu to diffuse more easily from one metal level to the next, whereas W serves as a more complete diffusion barrier. This may account for the fact that the lifetime of the CMP Al(Cu) vias is better characterized by the three-parameter lognormal distribution, whereas the lifetime of the W vias is adequately fit with the traditional two-parameter lognormal distribution. It is conceivable that there exists a minimum time before failure can occur for both the CMP Al(Cu) and CVD W via samples, but that this time is greater for the CMP Al(Cu) vias. As a result, evidence of a minimum time to failure for a given sample size is more apparent for the CMP Al(Cu) via samples as compared to the W via samples. It should be realized that for short stripe lengths, W vias will provide an enhancement of the electromigration lifetime due to the short-length effect [6]. It is anticipated that this would not occur for Al(Cu) vias, although data is required to confirm this speculation.

The use of the Sprint process additionally eliminates the $TiAl_3$ interface between the Al(Cu) via and the top (M2) metal level (Figure 2), resulting in a > 5x improvement in the electromigration lifetime. The elimination of this interface provides an easier diffusion path between metal levels for both Cu and Al as compared to the CMP Al(Cu) vias. For the W and Al(Cu) via processes, we assume that the $TiAl_3$ ($TiAl_3$ / TiN) interface on top of the M1 level has been removed during the via etch process. This assumption has been confirmed by SEM cross sections of multi-level samples. However, there can still be a thin layer of Ti ($TiAl_3$) or Ti / TiN lining the bottom and sidewalls of the via. We speculate that the lining on the bottom of the via is thin enough and/or discontinuous to allow Cu and Al to readily diffuse from one metal level to the next. A manufacturable Sprint process requires adequate deposition control such that a known uniform film thickness is obtained across the entire wafer. Furthermore, careful control of the aspect ratio to ensure uniform film thickness may be required. If these process controls can be implemented, then it is possible to increase the reliability of multi-level metallizations by replacing the W stud with an Al(Cu) via. Additionally, it may be possible to further improve the electromigration lifetimes of Sprint samples by increasing the Cu concentration in the Al(Cu) via to ensure a larger solute reservoir. (The results of this study with respect to Cu concentration in CMP AlCu vias were inconclusive, although they hinted at a slight improvement with 4.0wt.%Cu.)

The size and shape of precipitates in an Al(Cu) conductor can be controlled by annealing. However, presence of complete blocking boundaries at vias (CVD W studs, at stud intervals much greater than the Blech length) limits the electromigration lifetime reliability so that variations in the Al(Cu) line microstructure are not important [19]. The reliability of Al(Cu) lines and vias formed with the Sprint process may be optimized by tailoring their microstructure through a combination of deposition control and thermal annealing.

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TABLE I

M1 and M2 metallurgies used for jobs A and B. The CMP process includes both W and Al(Cu) vias. Note that the Sprint process results in a thicker M2 layer.

Job	Structure	Process	M1 Metallurgy	M2 Metallurgy
A	CK4_MAC1B	CMP	25nm Ti/800nm Al(2.0wt.%Cu)/ 25nm Ti/40nm TiN	Same as M1
	LDEM	Sprint	25nm Ti/900nm Al(0.5wt.%Cu)/ 25nm Ti/50nm Al(0.5wt.%Cu)	Same as M1, except 2000nm of Al(0.5wt.%Cu) between Ti layers
B	CK4_MAC1B	CMP	25nm Ti/950nm Al(0.5wt.%Cu)/ 25nm Ti/40nm TiN	Same as M1
		Sprint	25nm Ti/950nm Al(0.5wt.%Cu)/ 25nm Ti/40nm TiN	Same as M1, except 1500nm of Al(0.5wt.%Cu) between Ti layers

TABLE II

Average room temperature (25 °C) resistance of samples having either CVD W vias or CMP Al(Cu) vias. The structure tested is the CK4_MAC1B via chain, which contains 4 vias (see Figure 3). The standard deviation of the resistance is also listed. wt.%Cu refers to the Cu concentration in the vias.

Job	Via (W or AlCu)	wt.%Cu (in Via)	# Samples	Average Resistance (Ω)
A	W	---	11	26.38±0.83
	Al(Cu)	1.0	12	24.36±0.64
	Al(Cu)	4.0	12	23.98±0.60
B	W	---	12	28.91±1.26
	Al(Cu)	0.5	12	21.89±1.17

TABLE III

Average TCR values for the CVD W and CMP Al(Cu) via samples. The structure tested is the CK4_MAC1B via chain (see Figure 3). R_0 and α were extracted from equation (1), where the reference temperature is 50 °C. α has units of parts per million (ppm) per degree celsius (°C). wt.%Cu refers to the Cu concentration in the vias.

Job	Via (W or AlCu)	wt.%Cu (in Via)	# samples	R_0 (Ω)	α (ppm/°C)
A	W	---	4	29.43±0.10	2864±38
	Al(Cu)	1.0	3	27.16±0.10	2839±38
	Al(Cu)	4.0	3	26.61±0.09	2881±38
B	W	---	3	32.38±0.12	2571±14
	Al(Cu)	0.5	4	24.30±0.06	2928±24

TABLE IV

Values for t_{50} and σ from equation (2) for samples having CVD W or CMP Al(Cu) vias. The structure tested is the CK4_MAC1B Via Chain. wt.%Cu refers to the Cu concentration in the vias.

Job	Via (W or AlCu)	wt.%Cu (in Via)	j in M1 or M2 (10^5 A/cm²)	Fail Criteria	t_{50} (hrs)	σ
A	W	---	10.0	+20%	32.5	0.182
				Open	135.5	0.660
	Al(Cu)	1.0	10.0	+20%	10.5	0.601
				Open	68.3	0.585
	Al(Cu)	4.0	10.0	+20%	14.1	0.531
				Open	90.6	0.775
B	W	---	7.3	+20%	15.7	0.187
				Open	24.7	0.230
	Al(Cu)	0.5	7.3	+20%	117.2	1.008
				Open	142.2	1.110

TABLE V

Values for t_0, t_{50} and σ from equation (3) for the CMP Al(Cu) via samples. wt.%Cu refers to the Cu concentration in the vias.

Job	wt.%Cu (in Via)	j in M1 or M2 (10^5 A/cm²)	Fail Criteria	t_0 (hrs)	t_{50} (hrs)	σ
A	1.0	10.0	+20%	6.7	9.3	1.355
			Open	54.6	61.3	1.809
	4.0	10.0	+20%	8.4	12.6	1.241
			Open	50.2	70.5	2.263
B	0.5	7.3	+20%	24.6	102.8	1.363
			Open	33.8	121.0	1.754

TABLE VI

Electromigration results for Al(Cu) via samples prepared by the CMP or Sprint process. The results for CVD W vias are included for comparison. Values for t_{50} and σ were generated from equation (2). The Cu concentration in M1 and M2 is 0.5wt.% for both the Al(Cu) and W via samples. The Cu concentration in the Al(Cu) vias is also 0.5wt.%.

Job	Structure	Via (W or AlCu)	j in M1 (10^5 A/cm²)	j in M2 (10^5 A/cm²)	Fail Criteria	t_{50} (hrs)	σ
A	LDEM	W	10.0	6.7	+20%	32.2	0.208
					Open	44.3	0.297
		Al(Cu)-Sprint	10.0	4.8	+20%	*	
					Open	*	
B	CK4_ MAC1B	W	7.3	7.3	+20%	15.7	0.187
					Open	24.7	0.230
		Al(Cu)-CMP	7.3	7.3	+20%	117.2	1.008
					Open	142.2	1.110
		Al(Cu)-Sprint	7.3	4.8	+20%	**	
					Open	**	

* 0/12 fails after 1530 stress hours
** 1/12 fails after > 1200 stress hours

Table VII

Location of electromigration failures for the CMP Al(Cu) and CVD W via samples by Electron Beam Induced Current (EBIC). Via #1 and #3 refer to the CK4_MAC1B chain (Figure 3). The Cu concentration in the Al(Cu) vias is 0.5wt.%.

Via (W or AlCu)	# Samples	Fails at Via #1	Fails at Via #3	Unable to Locate
W	12	3	7	2
Al(Cu)	12	6	3	3

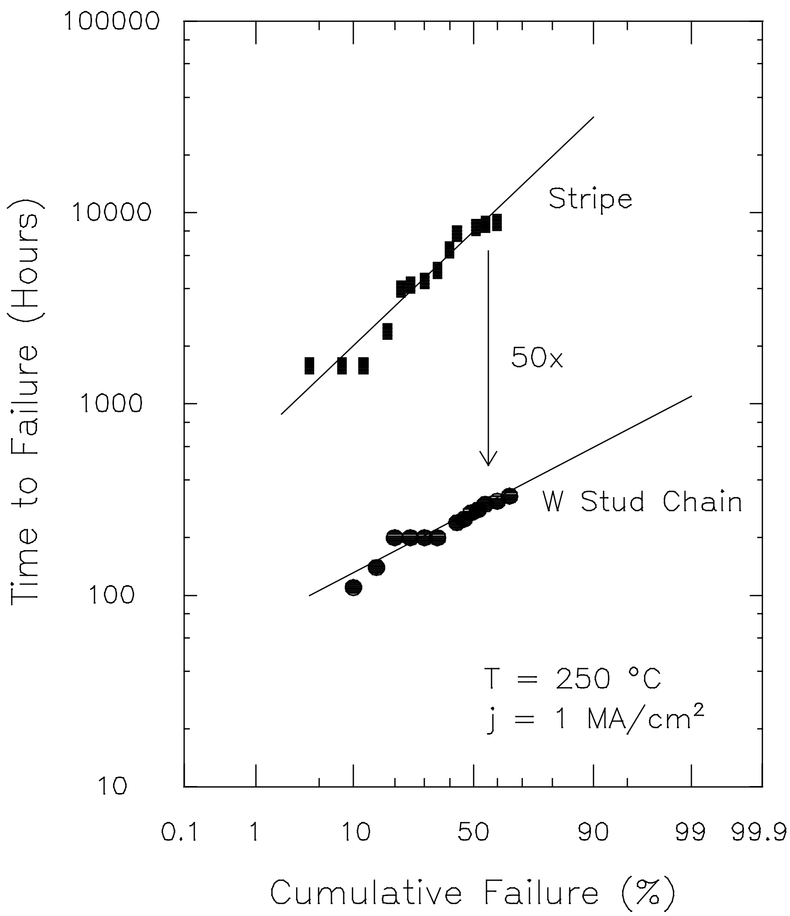

Figure 1 The electromigration lifetime of a two level W stud chain is significantly shorter than the single level stripe [1]. The interconnect metallurgy is Ti-Al(0.5wt.%Cu)-Ti.

Figure 2 Schematic cross sections of the a) CMP process (AlCu and CVD W) and the b) Sprint process (AlCu only). Optional TiN layers above top $TiAl_3$ layers are not shown.

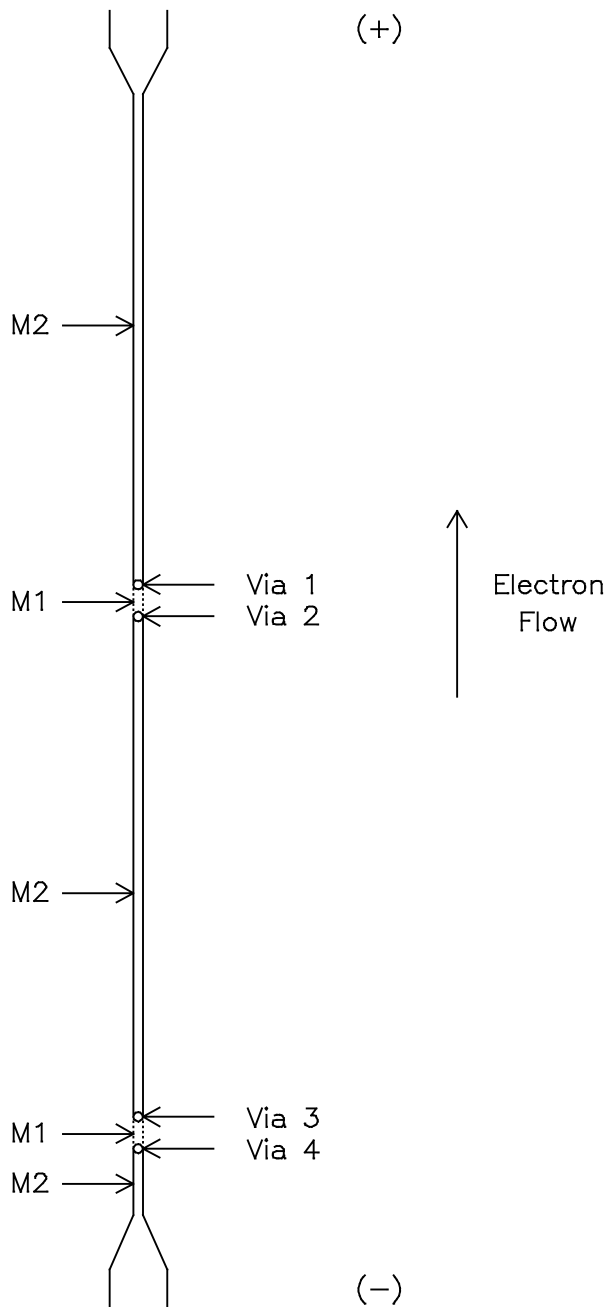

Figure 3 Schematic top view of the CK4_MAC1B via chain. There are a total of four vias, labeled 1-4. The distance between vias on M1 (dashed line) is 8 μm, while the distance between vias on M2 (solid line) is 300 μm.

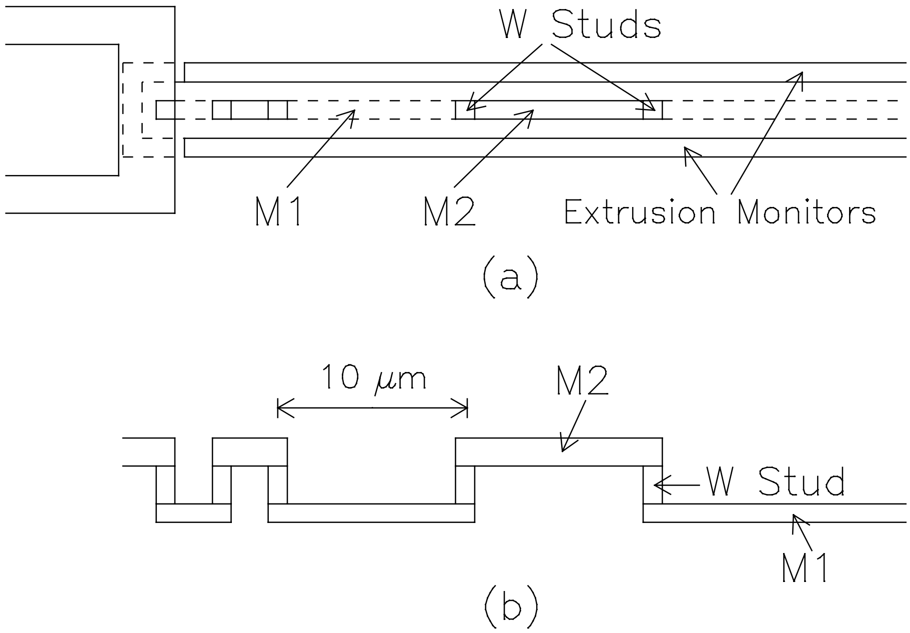

Figure 4 a) Schematic top view of the LDEM via chain and b) schematic cross section of the LDEM via chain.

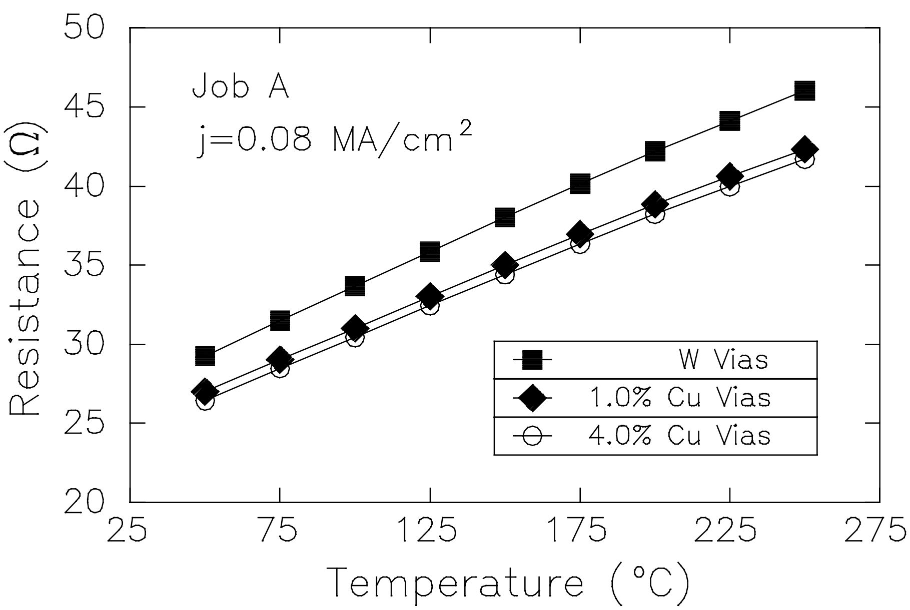

Figure 5 Average resistance vs. temperature at 8.0×10^4 A/cm^2 for the CVD W and CMP Al(Cu) Vias. There are 4 W via samples, 3 Al(1.0wt.%Cu) via samples and 3 Al(4.0wt.%Cu) via samples.

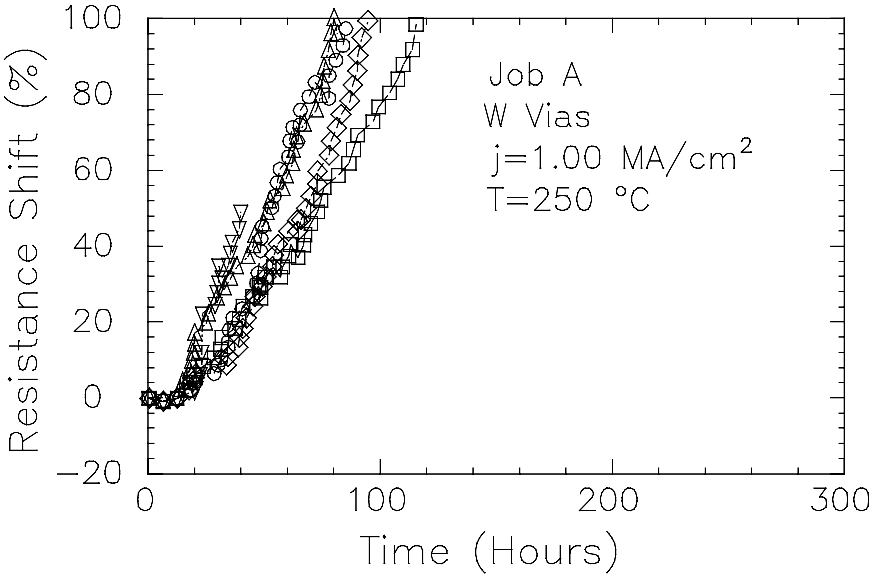

Figure 6 Resistance shift (%) vs. time for five of the CK4_MAC1B chains having CVD W vias from job A. The test conditions were 250 °C and an M2 current density of 1.0×10^6 A/cm².

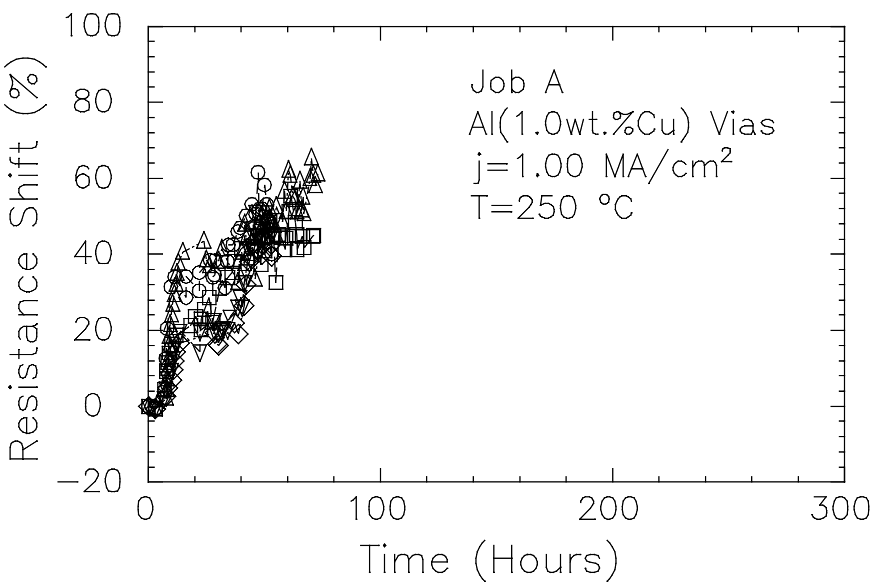

Figure 7 Resistance shift (%) vs. time for five of the CK4_MAC1B chains having CMP Al(1.0wt.%Cu) vias from job A. The test conditions were 250 °C and an M2 current density of 1.0×10^6 A/cm².

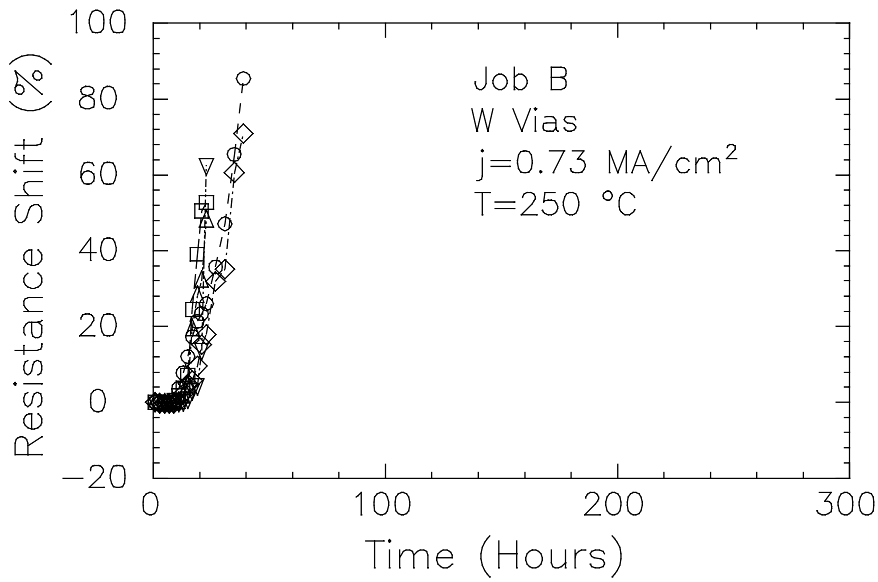

Figure 8 Resistance shift (%) vs. time for five of the CK4_MAC1B chains having CVD W vias from job B. The test conditions were 250 °C and an M2 current density of 7.3x10^5 A/cm².

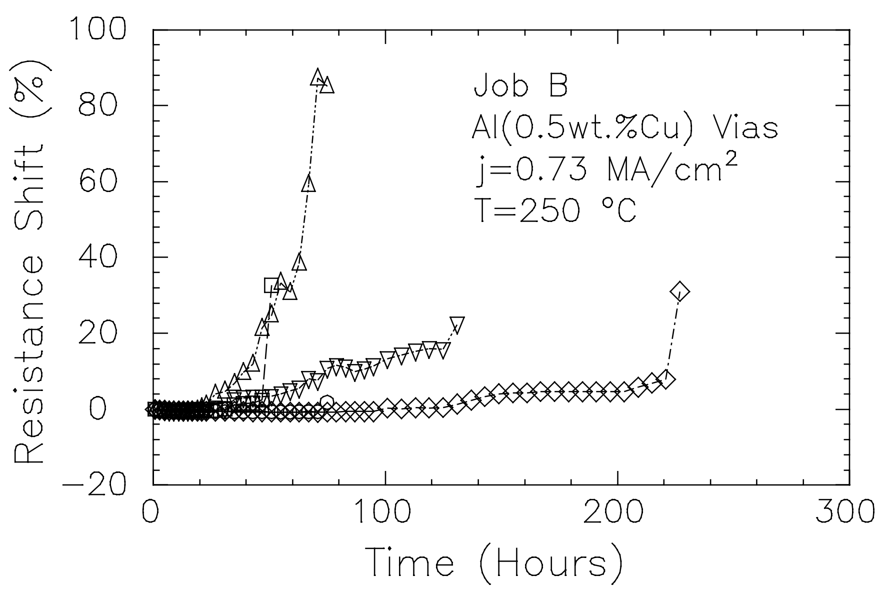

Figure 9 Resistance shift (%) vs. time for five of the CK4_MAC1B chains having CMP Al(0.5wt.%Cu) vias from job B. The test conditions were 250 °C and an M2 current density of 7.3x10^5 A/cm².

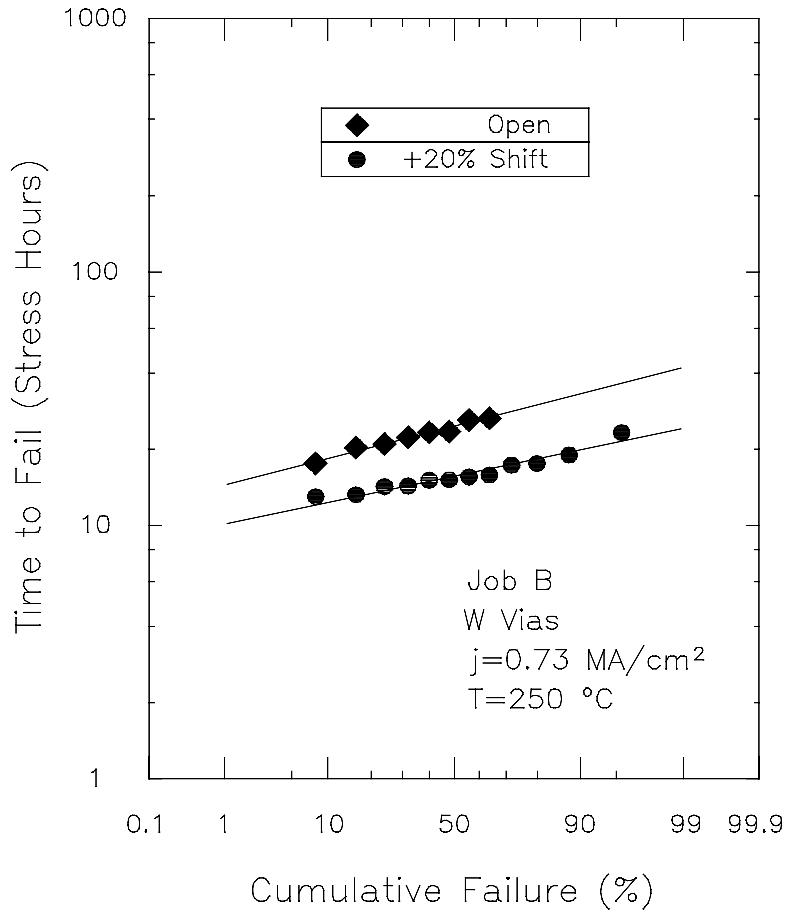

Figure 10 Lognormal CDF plots for the W via samples from job B. There are data for two fail criteria; +20% resistance shift and open. Each solid line represents the least squares fit of the data according to equation (2).

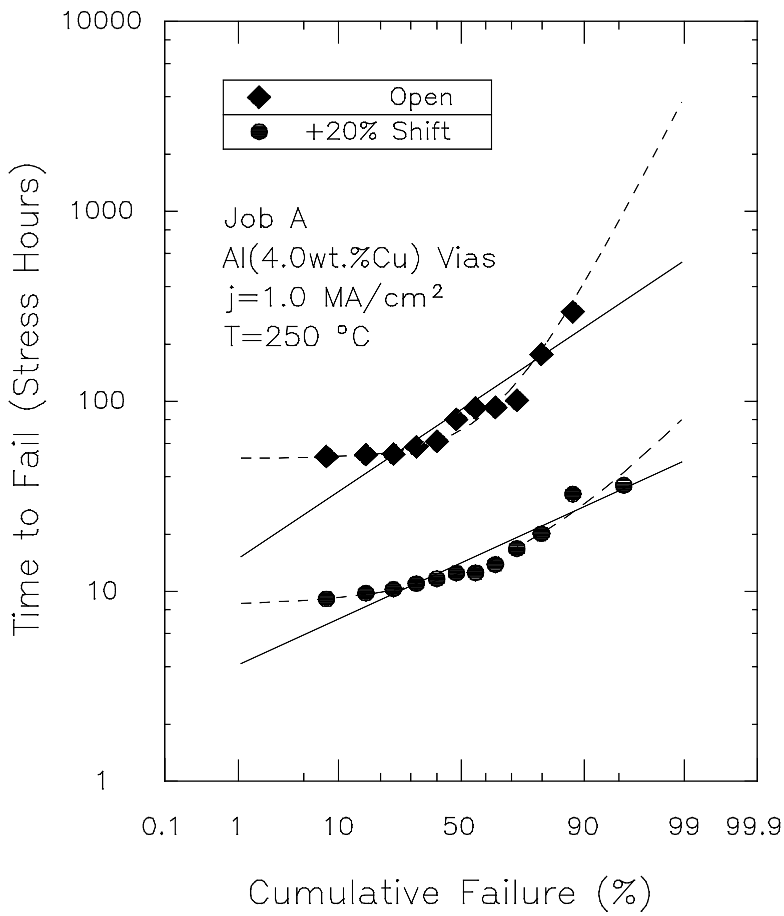

Figure 11 Lognormal CDF plots for the CMP Al(4.0wt.%Cu) via samples from job A. The solid lines for each fail criterion were obtained from equation (2), while the dashed lines were obtained from equation (3).

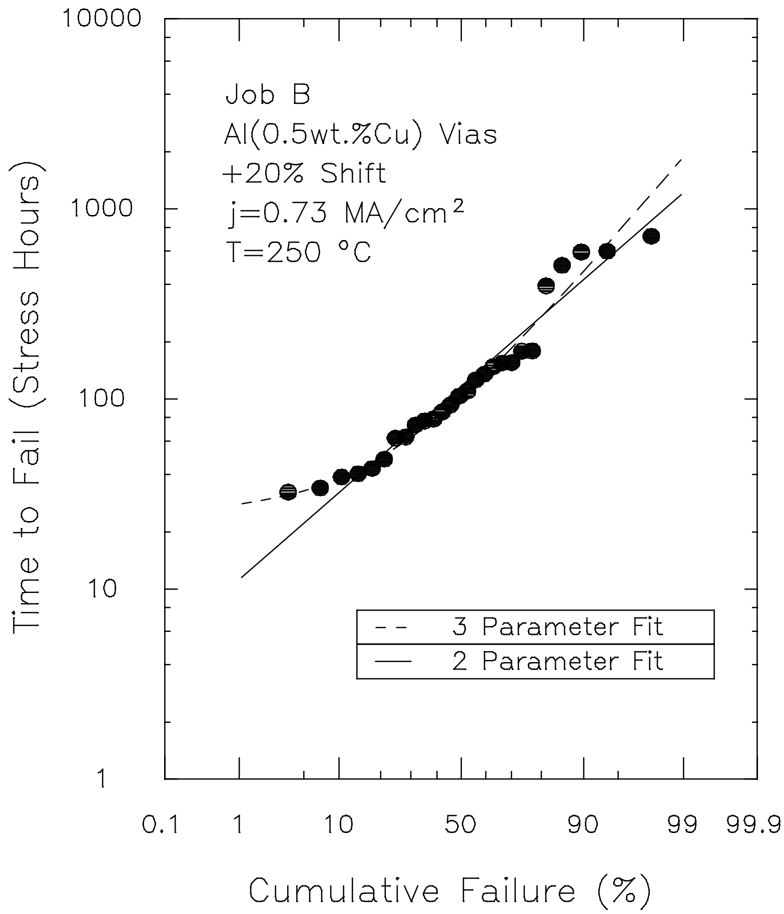

Figure 12 Lognormal CDF plot for the CMP Al(0.5wt.%Cu) via samples in terms of a +20% shift failure criterion. The solid line was obtained from equation (2) while the dashed line was obtained from equation (3).

Figure 13 SEM cross section of a CMP Al(0.5wt.%Cu) via sample from job B that electrically opened after 42 hours. The test conditions were 250 °C and an M2 current density of 7.3x10^5 A/cm².

Figure 14 SEM cross section of a CMP Al(0.5wt.%Cu) via sample from job B that electrically opened after 72 hours. The test conditions were 250 °C and an M2 current density of 7.3x10^5 A/cm².