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Research Report

Room Temperature Operation of a Quantum-Dot Flash Memory

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Abstract

A flash-memory device has been fabricated and demonstrated at room temperature by coupling a self-aligned, sub-50 nm quantum dot to the channel of a transistor on a silicon-on-insulator substrate. Large threshold voltage shifts of up to 0.75 V are obtained for small erase/write voltages (≤ 3 V) at room temperature. At 90 K, evidence of single electron storage is observed. The small size of this device is attractive for achieving high packing densities, while the relatively large output current (μA's), low off-state current (pA's), and simple fabrication, requiring only minor variations in standard processing, make it suitable for integration with current silicon memory and logic technology.

I. Introduction

The ultimate limit of a conventional electronic device is one that functions by controlling a single electron. This can be achieved by a device which transmits an electron through a small volume (a low capacitance island) coupled to two external reservoirs by a barrier whose resistance is larger than the resistance quantum. Such a device exhibits a Coulomb blockade, and gating of the electrochemical potential of the island allows control of the current (see e.g. [1] and [2]). Complementary [3] and clocked [4] logic schemes have been proposed to utilize these devices. However, the large impedance mismatches and low currents (nA's) inherent to these devices limit their compatibility with current technology.

In another approach, the charge quantization effects can be electrostatically coupled to the channel of a transistor in a flash-memory device. Such devices have been demonstrated in poly-crystal [5] and single-crystal [6, 7] silicon. The latter device uses multiple nano-crystals coupled to the channel of a conventional MOS transistor, which minimizes offset charge problems and allows ≈ 3 V operation with μA currents and 100 nsec write times. Here, we demonstrate the limit of this device — a single quantum-dot coupled to a channel. The result is an extremely small device which is compatible with the electrical and process requirements of current silicon logic and memory technology.

II. Device Structure, Results, and Discussion

A schematic of the device together with cross-sections is shown in Fig. 1. The layers which will form the quantum-dot floating gate (2.5 nm tunnel oxide / 8 nm amorphous Si / 9 nm control oxide) are deposited on a silicon(≈ 30 nm)-on-insulator (SOI) substrate, which allows for easy device isolation. The quantum-dot island is formed self-aligned to the silicon channel, and the gate and source/drain regions are doped simultaneously by As implantation.

In a coupled quantum-dot structure, small dimensions lead to both a small capacitance which affects the charging energy, and size-quantization which affects the eigenenergy of the stored electrons. Table 1 emphasizes the qualitative magnitude of these effects by estimating parameters for spheres of silicon embedded in SiO_2 and separated from the gate by a 7 nm control oxide in an idealized structure. The actual structure and dimensions of the fabricated device differ from these, but the table serves to stress that even under conditions when the quantum-dot charging energy is only comparable to thermal energy, a large threshold voltage shift occurs.

Figure 2 shows the hysteresis in the drain current of the device as a function of the initial gate voltage for the smallest device. Due to lateral implant straggle, this device is normally-on (i.e. has a negative threshold voltage), but larger devices are normally-off and exhibit similar memory effects. The device exhibits low off-currents (pA's) and silicon-logic compatible on-currents (μA's for $V_{DS} \approx 2$ V), limited here by source/drain resistances, not device physics. The threshold voltage shift is large (≈ 0.75 V), and the retention time is significantly longer than the time-scale of the measurement (seconds). Thus the charging/discharging process is inefficient near $V_{GS} = 0$ V (i.e. flatband conditions), but becomes efficient near 3 V (approximately the electron barrier height at the SiO_2/Si interface), which is desirable for a memory device.

Note that the threshold of the device in Fig. 2 is *higher* after charging the quantum-dot at $V_{GS} = -3$ V, indicating electrons have been stored, which is the opposite of what would be expected for a planar device with electrons tunneling between the silicon channel and the floating island (such as in [6]). However, the gate in this device wraps almost around the channel (Fig. 1(c)), so the inversion layer electrons are effectively being gated by both a front and back gate. Due to the large effective dielectric thickness of the top gate stack compared to the thin channel silicon and sidewall oxide, the electric field from the back gate is stronger, resulting in the polarity reversal of the charging gate voltage.

At low temperature (90 K), single-electron charging of the quantum-dot is observed. In Fig. 3, as the gate voltage is swept *slowly* (to allow the number of electrons in the quantum-dot to reach equilibrium with the channel) from -3 to +3 V, the drain current exhibits staircase plateaus with a periodicity of $\Delta V_{GS} \approx 0.7$ V as electrons tunnel off the quantum-dot. The cumulative number of steps (≈ 7) corresponds to the number of electrons stored in the dot prior to the sweep. Some of the plateaus are less pronounced, possibly indicating a second-order effect being caused by discrete levels in the silicon channel itself. These levels could be due to dopant atoms, or the channel may also be unintentionally constricted near the source/drain region due to pattern-dependent oxidation at the back SOI interface[8]. This could also be a cause for the reduced drain current at 90 K, though the majority of this reduction is attributable to dopant freeze-out.

Referring to Table 1, $\Delta V_{GS} \approx 0.7$ V corresponds to a control gate capacitance on the order of 0.25 aF. This is consistent with the observed device geometry, taking into account the opposing electric fields caused by the gate wrapping around the channel. The Coulomb charging energy for the quantum-dot (d(effective) ≈ 30 nm) is 12 meV, consistent with the 90 K observation temperature. Room temperature observation of these steps requires further size reduction.

While discrete electron effects are observable in this structure at lower temperature and are washed out at room temperature (similar to [7]), its beauty is in still being functional at room temperature with a small, finite number of electrons, making it significantly more immune to offset charge and Poisson size distribution effects than a standard single-electron device. In addition, the dimensions of this device are approaching the perceived limits for conventional silicon field effect transistors, yet efficient current drive and control has been maintained.

IV. Summary

We have reported the room-temperature operation of a small (sub-50 nm) flash-memory device which utilizes a silicon quantum-dot coupled to a conducting channel. The most significant features of this device are its use of low voltages (< 3 V for write/read/erase), large threshold-voltage shifts (≈ 0.75 V), large drive currents (100's nA's - μA's), and low off-state current (pA's), resulting in an effective low-power memory, compatible with current silicon logic technology. Further scaling of the quantum-dot dimensions is expected to yield single-electron control at room temperature, while maintaining this compatibility.

Acknowledgments

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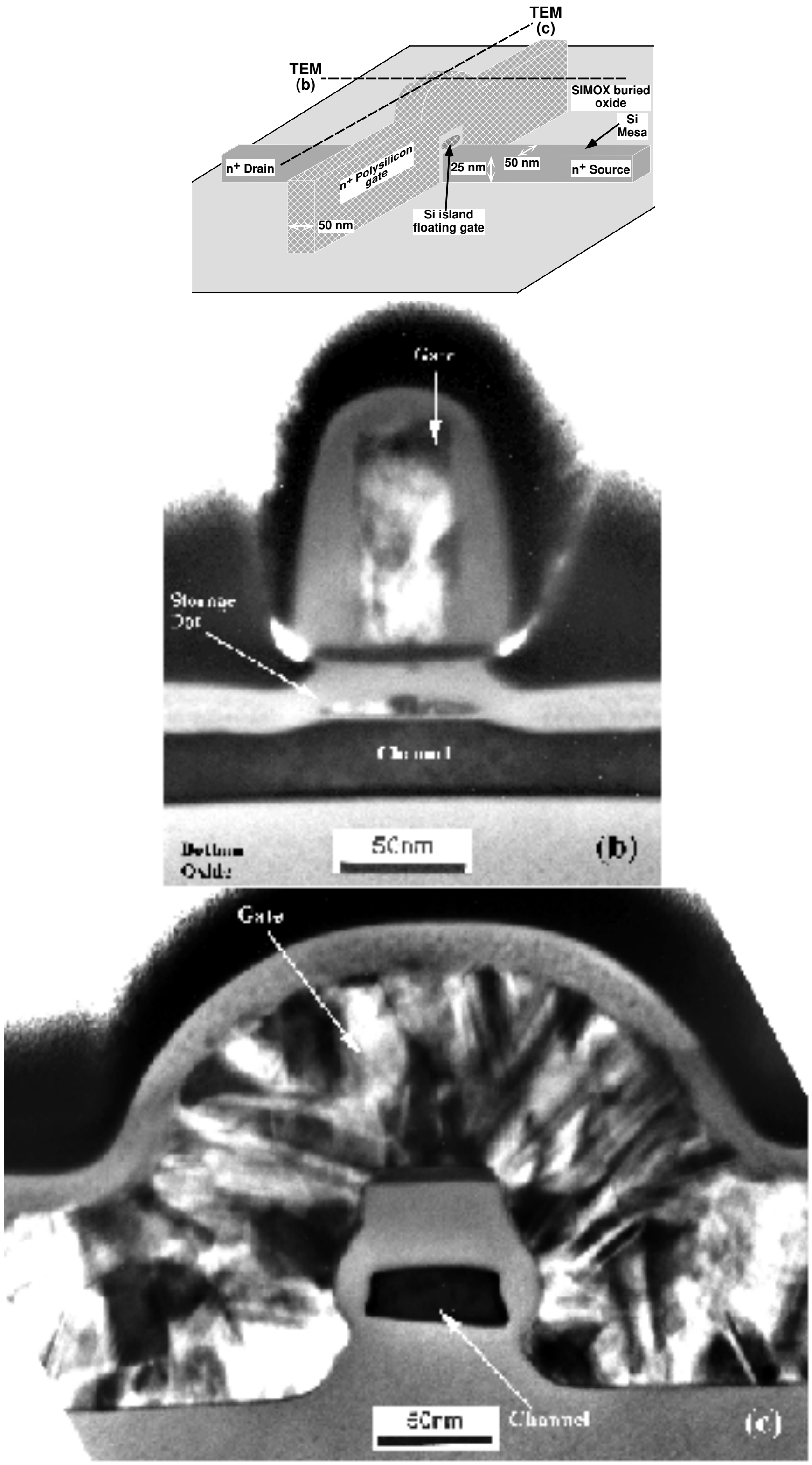
Quantum-Dot Diameter, $2r$ (nm)	Capacitance, $C \approx 4\pi\varepsilon_{ox} r$ (aF)	Charging Energy, $e^2/2C$ (eV)	Ground State Eigenenergy (eV)	Control Gate Capacitance, C_{CG} (aF)	Single Electron ΔV_T , e/C_{CG} (V)
30	6.51	0.012	≈ 0.003	4.10	0.039
20	4.34	0.018	≈ 0.007	2.11	0.076
10	2.17	0.037	≈ 0.030	0.63	0.255
5	1.08	0.074	≈ 0.104	0.17	0.924
3	0.65	0.123	≈ 0.290	0.07	2.460
2	0.43	0.185	≈ 0.600	0.03	> 5
1	0.22	0.369	≈ 2.600	0.01	> 20

Table 1 Approximate self-capacitance, charging energy, and ground state eigenenergy due to quantum confinement for a silicon sphere of given diameter embedded in an oxide. Assuming a control oxide thickness of $t_{CG} = 7$ nm (conformal to the sphere), the effective control gate capacitance is computed as $C_{CG} \approx \left(2\pi\varepsilon_{ox} r^2\right) / \left(t_{CG} + \left(\varepsilon_{ox}/\varepsilon_{Si}\right) r\right)$ The resulting threshold voltage shift due to single-electron storage is also computed.

Figure 1 (next page) (a) Schematic of a quantum-dot coupled flash-memory device. Transmission electron micrographs show the device in cross-section (b) along the channel and (c) along the gate. Note the quantum-dot island is unintentionally not visible in (c). The gate is ≈ 30 nm in length, and 100 nm in height.


TEM
(c)
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SIMOX buried oxide
Si Mesa
n+ Drain
n+ Polysilicon gate
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50 nm
n+ Source
Si island floating gate
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Gate
Channel
50nm
(b)
Gate
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(c)

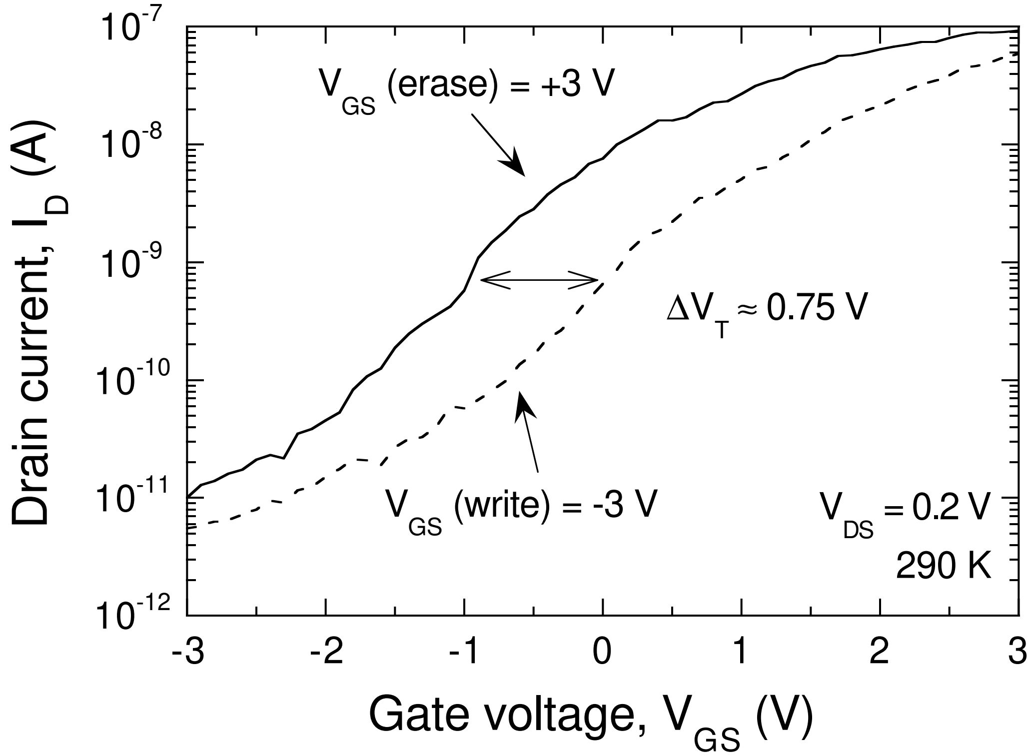

Figure 2 Room temperature drain current hysteresis in a small device (W x $L \approx 50$ nm lithographically) showing the threshold voltage shift after charging of the floating gate. Write/erase gate voltages indicate the voltage applied to the gate for 10 seconds prior to sweeping the gate voltage to produce each curve shown.

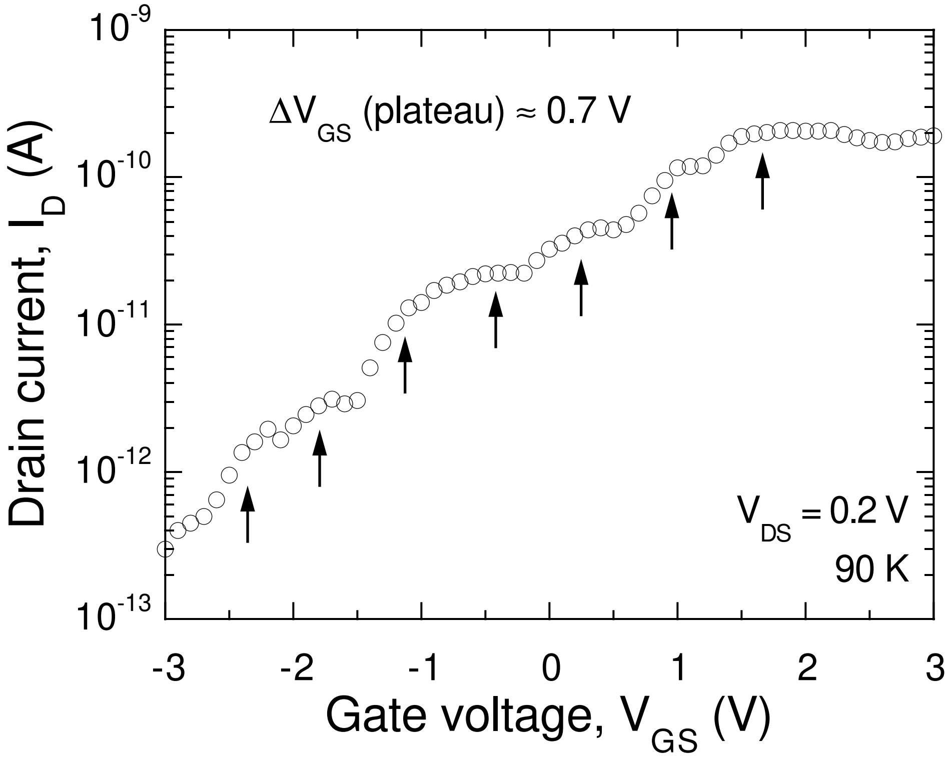

Figure 3 Low temperature drain current showing “staircase” structure as gate voltage is swept quasi-statically. Indicated transitions are associated with single electron charging of the quantum-dot embedded in the gate oxide.