RC 19974 (3/14/95)
Engineering and Technology

IBM Research Report

Low Cost FCA/BGA Single Chip Carriers

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1 Introduction

The debate over the virtues of peripheral contacts versus arrays of contacts takes place in both the chip and first level package arenas. One major driver for the use of area arrays is the increasing number of I/O required by new generations of silicon devices. At the chip level, the use of peripheral contacts for wirebond attach requires increased silicon device area in order to support the necessary I/O.[5] The same phenomenon occurs in the case of the first level package; a 304 pin quad flat pack (QFP) takes up much more board area than its ball grid array (BGA) counterpart. Additionally, the fine pitch (0.4 mm) used for the QFP contacts increases the difficulties and lowers the yield on assembly as well as making module test more difficult.
There are two major challenges to wider usage of BGA packages. The first is the current cost premium for ceramic BGA packages over QFPs while the second is the lack of experience of many assembly plants with BGA packages. This lack of an assembly infrastructure is one of the factors that contributed to the long delay between the introduction of surface mount components and their widespread usage.
Some of the cost concerns about BGA are being addressed by the introduction of plastic BGA (PBGA) packages for wirebonded chips such as those produced by Citizen and Amkor and used by Compaq and Motorola. Cavity up packages are limited in their ability to handle high power chips because the package geometry makes the use of a heat sink inconvenient. Cavity down implementations address some of these thermal management challenges, but may be more complicated from the perspective of substrate fabrication and module assembly.
With the increase in bus-widths and clock speeds, the corresponding increase in chip I/O is encouraging more chip houses to consider flip chip attach technology. The PowerPC collaboration between IBM, Motorola, and Apple and the utilization of C4 technology by Motorola may lead to the wider application of FCA technology. An assessment of the challenges involved in packaging high I/O count FCA devices in a cost effective manner has been undertaken using the PowerPC 601 and 604 chips as concrete targets for this exercise. To date this assessment has dealt primarily with substrate design and fabrication issues. No conclusions about IBM's product plans or future packaging offerings should be drawn from the work discussed here.

2 Chip and Module Footprints

A summary description of the chip footprint information for the 601 and 604 chips is given in Table 1. Because of differences in the chip footprint geometries, the PowerPC 601 presents more of a challenge to wire out in laminate technology than the 604. By analogy with studies of the escape problem for BGA modules on boards[2], the chip escape problem is simplified when power and ground connections are placed in the center of the chip while signal I/O are around the periphery. In this study both chips were packaged on standard 21 mm square substrates with 256 I/O on a 50 mil (1.27 mm) pitch.
The designs for these module substrates were implemented under several constraints. In particular, the layer count was to be minimized. Both the 601 and 604 substrate designs have a 2S2P cross-section. The vast majority of the escape wiring takes place on the chip side circuit layer. A summary of the linewidths and the total length of

	601	604
Chip Size (mm)	10.95×10.95	12.39×15.84
Signal I/O	186	172
Power I/O	226	253
Ground I/O	221	248
Total Chip I/O	633	673

Table 1: Summary of chip footprint information for PowerPC 601 and 604.

	Line Width (mils)	Line Length (inches)
601	2	9.8
	3	3.8
	4	35.5
604	3	0.04
	4	39.4

Table 2: Linewidth requirements of 601 and 604 module substrate designs.

line in the top circuit layer is given in Table 2. The plated through holes were a mixture of 8 mil and 10 mil holes on 10 mil and 12 mil capture pads respectively. Approximately 300 drilled plated through holes were necessary for both the 601 and 604 designs.

The fine pitched wiring in these substrate designs is required to escape signals through regions of local congestion. C4 attached chips have typically been packaged on multi-level ceramic BGA substrates with a high degree of z-interconnect capacity and the footprints of the chips reflect this. Once laminate chip carrier packaging is an accepted option, chip footprints can be modified to alleviate the congestion and permit even lower cost laminate packages to be employed.

3 Achieving the Necessary Wireability in a Printed Wiring Board Environment

In order to assess the available printed wiring board lithographic capabilities, a test vehicle was designed with serpentine patterns of various linewidths and spaces. This test vehicle was built by a number of different printed wiring board fabs and the results are summarized in Figure 1. The fine line capability needed for the chip wiring escape can be achieved using a number of approaches compatible with printed wiring board tool sets including the use of electrophoretically deposited resist[3] or pattern electroplating[6].

One of the major challenges facing any laminate implementation of an FCA/BGA package is posed by necessity of bringing chip I/O through the substrate to the BGA side by use of drilled plated through holes. The large number of such PTHs that are

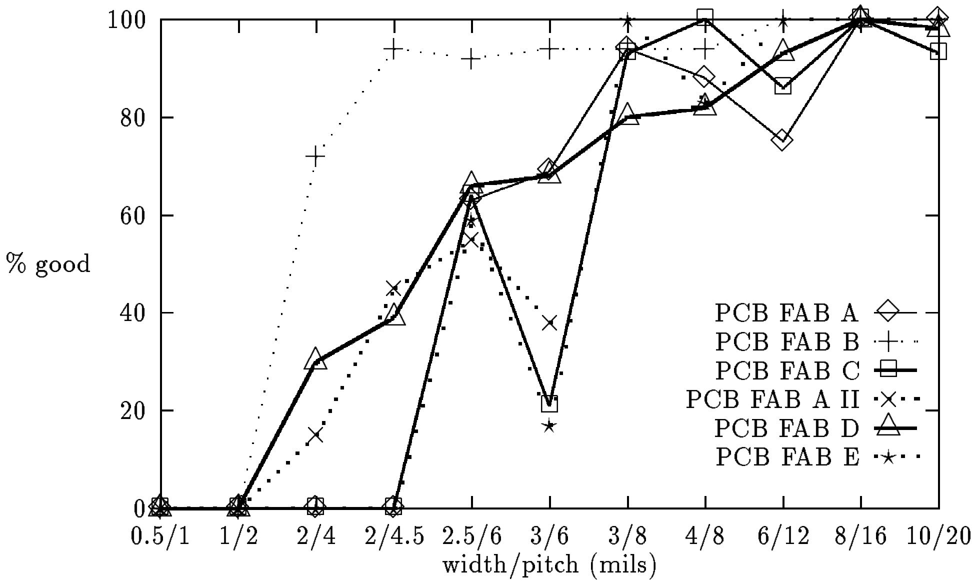

Figure 1: Summary of fine line capabilities of surveyed printed wiring board fabrication facilities based on test vehicle build results.

required affect the substrate cost and also take up wiring channels needed to escape the chip I/O.

Even with the drilling and fine line processing required to fabricate high I/O FCA/BGA laminate substrates, the results of this sizing indicate that a substrate cost of $0.01 per module I/O should be attainable in manufacturing volumes.

4 Other Issues

Substrate fabrication is only one of the issues that must be addressed in providing a manufacturable path to a laminate chip carrier. Assembly and associated reliability issues are areas requiring further work. A reliable FCA on laminate process requires a method for dressing the chip attach sites with an adequate volume of solder to ensure consistent joining. After chip join, an underfill or encapsulation is performed in order to enhance the reliability under thermal cycling of the assembled module. The importance of the interfacial adhesion of the encapsulant to chip surface has been identified as a crucial component in the reliability of an FCA on laminate module[1, 4].

5 Summary

The results of a design study assessing the ground rules required to fabricate FCA/BGA single chip modules for the PowerPC 601 and 604 chips have been presented along with data from a survey of fabrication capabilities. Prototype runs on a printed circuit board manufacturing line indicate that that a substrate cost of $0.01 per I/O should possible in production.

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