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IBM Research Report

Executive Summary of Characterization Results Compared to Modelling and Simulations

Dan Corcos, Danny Elad
IBM Research Division
Haifa Research Laboratory
Mt. Carmel 31905
Haifa, Israel

Thomas Morf, Lukas Kull
IBM Research – Zurich
8803 Rüschlikon
Switzerland

Research Division
Almaden – Austin – Beijing – Cambridge – Dublin - Haifa – India – Melbourne - T.J. Watson – Tokyo - Zurich

TeraTOP

Terahertz Photonic Imager on Chip

Contract No - 288442

WP3: THz Sensor 2/EM Coupled MEMS THz Antenna

Deliverable D3.6

Executive summary of characterization results compared to modelling and simulations

Authors: Dan Corcos, Danny Elad (IBM Research - Haifa)
Thomas Morf, Lukas Kull (IBM Research - Zurich)

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Contributor	Organization
Dan Corcos	IBM Research – Haifa
Danny Elad	IBM Research – Haifa
Thomas Morf	IBM Research – Zurich
Lukas Kull	IBM Research – Zurich

Release Approval

Date dd.mm.year	Organization	Person In Charge	Contact
	CSEM	John Farserotu	Phone: +41 32 720 54 82 mobile: +41 79 35 668 16 e-mail: john.farserotu@csem.ch

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1. Introduction

The present document summarizes the electrical characterization of the pixels developed for the TeraTOP project in Phase 2 according to the WP3 approach “THz Sensor 2/EM Coupled MEMS THz antenna”. The design of the Phase 2 sensor chip is based on the experience gained with the Phase 1 design and through some additional wafer runs submitted by IBM.

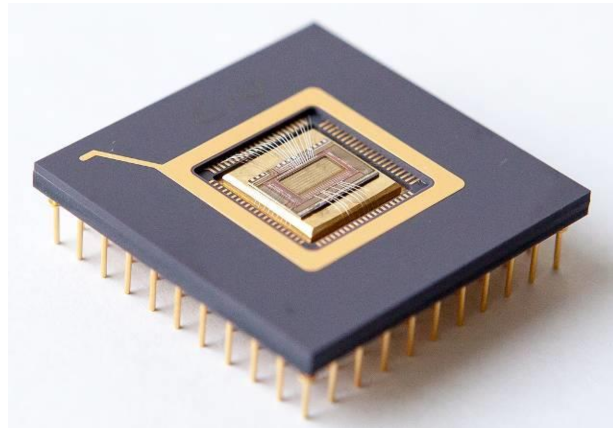
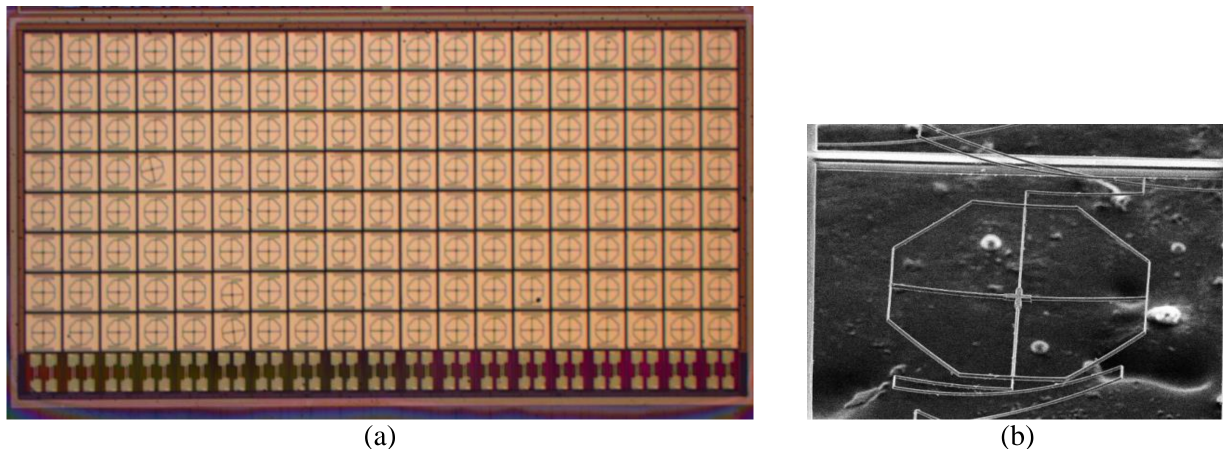


Figure 1. THz sensor chip with 19 x 8 pixels and readout electronics after MEMS post processing; the chip is packaged in a ceramic case.



(a) (b)

Figure 2. (a) Optical microscope photograph of the sensor region after the MEMS process. (b) Electron micrograph of a single pixel. The sensor transistors are accommodated underneath two of the four inner segments. (The surface visible in the background is the SEM sample holder).

The Phase 2 sensor chip includes a 19x8 pixel array with a reference “blind” pixel row as described in report D3.4, completed with the readout electronics described in D4.6. Figure 1 shows a bonded post-processed chip, prepared for testing. The chip is mounted on a pedestal, which has a gold finishing and, acting as backside reflector, it serves to enhance the optical response. Figure 2 shows the sensor array after MEMS processing and a SEM image of a single sensor. The pixel pitch is 250um. The bottom row contains the blind reference sensors.

The pixels described in this report were fabricated at IBM Research in Zurich using the processing steps described in report D3.5. The devices from Leti (WP5) were not yet available at the time of writing

this report.

The electrical parameters of the pixels were measured and compared to simulations. The new results were also compared to those of Phase 1, whenever possible. THz characterization is covered in D6.2.

2. Characterization Results

DC characteristics

The IV characteristics of the sensing transistors were measured for numerous devices both from regular and post-processed chips. We found the comparison of these characteristics to be a first important indicator of the health of the fabricated MEMS devices. Figure 3 shows an IV measurement of 18 devices before and 18 devices after MEMS post processing on a single chip each.

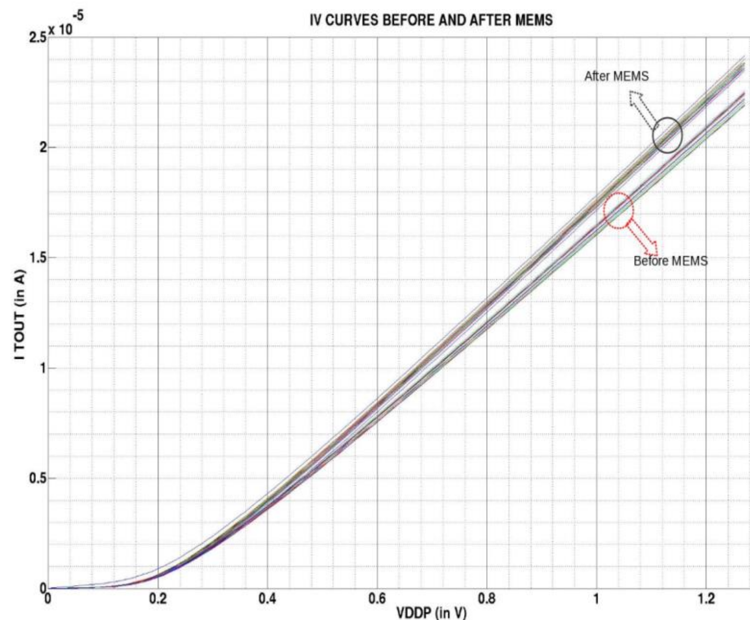


Figure 3. IV curves before and after MEMS.

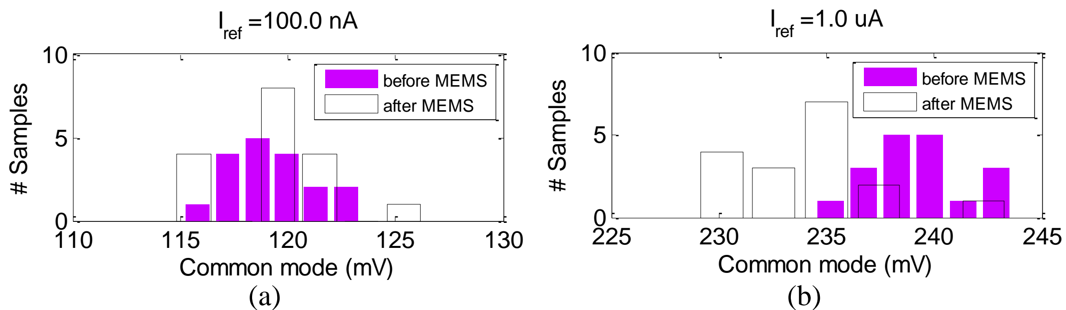


Figure 4. Calculated dispersion of the bias point (a) with 100 nA bias and (b) with 1 µA bias.

These measurements show that the IV curves of the post-processed chip are different from those of the unprocessed chip, but the DC characteristics are rather consistent between pixels of the same chip. For any given applied voltage, the measured current of the post-processed devices is larger. This variation is not caused by a threshold voltage shift, which would shift the knee voltage, but rather by a different,

larger, series resistance. It should be noted that the measurements before and after MEMS are not performed on the same chip since wire bonding is required to characterize the sensors. However, the variation in observed here is well within process variation.

It is important to know the dispersion of the operating point because a strong lack of uniformity cannot be compensated by the ROIC, thus giving rise to problems such as signal offset, amplifier saturation and gain imbalance. From the data of Figure 3 we calculated the mean operating point voltage (labeled Vcm) as well as its variance. Two operating points were considered: the one corresponding to the nominal ROIC working current of 1 µA and the optimum current for NEP in the range of 100 nA. The calculated dispersion is shown in Figure 4. A summary of this characterization, including the values obtained from Monte Carlo simulations were added to the table below.

Table 1. Summary of the operating point distribution at 100 nA and 1 µA.

	I_{ref} = 100 nA		**I_{ref} = 1 uA**	
	Vcm	σ	Vcm	σ
Before MEMS	119 mV	2 mV	239 mV	2.3 mV
After MEMS	120 mV	2.9 mV	235 mV	3.5 mV
Simulation	90 mV	2 mV	208 mV	2.2 mV

Although the limited number of tested devices doesn't allow for fully reliable statistical observations, we may learn that dispersion has not grown significantly following the MEMS process.

Noise characteristics

The noise Power Spectral Density (PSD) of several pixels from both unprocessed and post-processed chips was characterized using a spectrum analyzer. Since the demonstrator board developed in WP7 includes a high order low pass filter with cutoff at 500 Hz, we expect the MOSFET sensor's $1/f$ noise to be the dominant noise source. The application of (Deep) Reactive Ion Etching (DRIE/RIE) to CMOS devices is known to affect their structure and to influence their behavior. In particular, $1/f$ noise was shown to increase in intensity following such post-processing. The noise contribution of the ROIC was designed to be lower than the pixel's noise.

By collecting the PSD value at 1 Hz for √(1 Hz) bandwidth of several devices we obtain the noise characteristics shown in Figure 5. The measurements were repeated for increasing values of bias current.

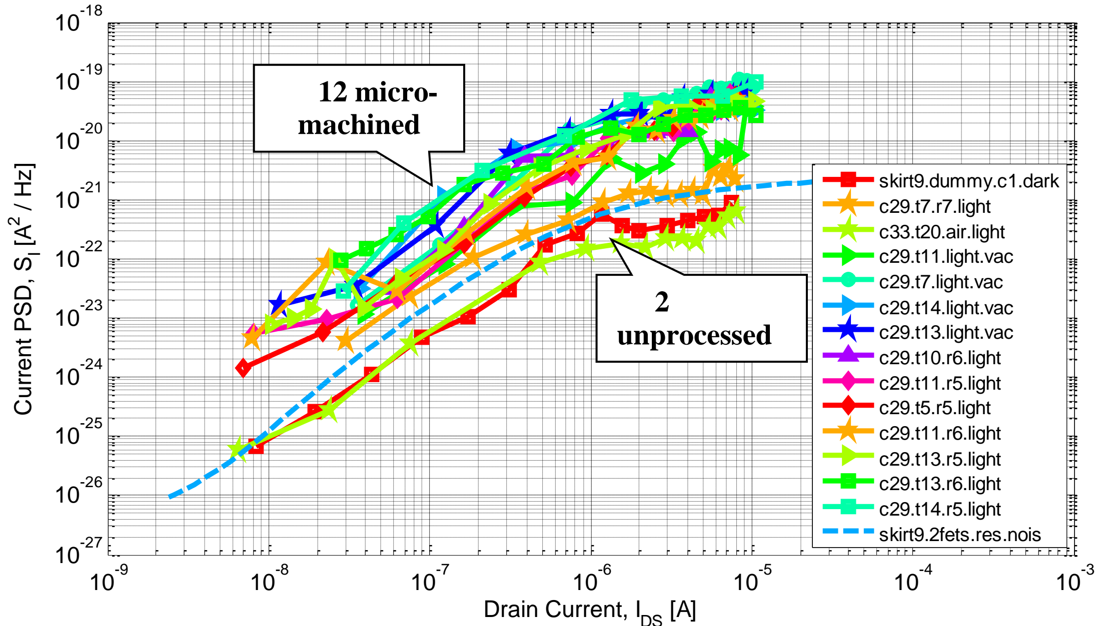


Figure 5. Measured noise PSD of 12 micro-machined pixels and 2 unprocessed pixels.

By observing these results we may note that:

1. The unprocessed devices are in line with our simulations
2. Following micro-machining the noise power greatly grew (4x to 100x)
3. The pixel to pixel variation within the same MEMS chip is also larger
4. The noise degradation is less severe below 100 nA.

The results are summarized in the bar plots in Figure 6, where two operating points are considered: 100 nA and 1 µA.

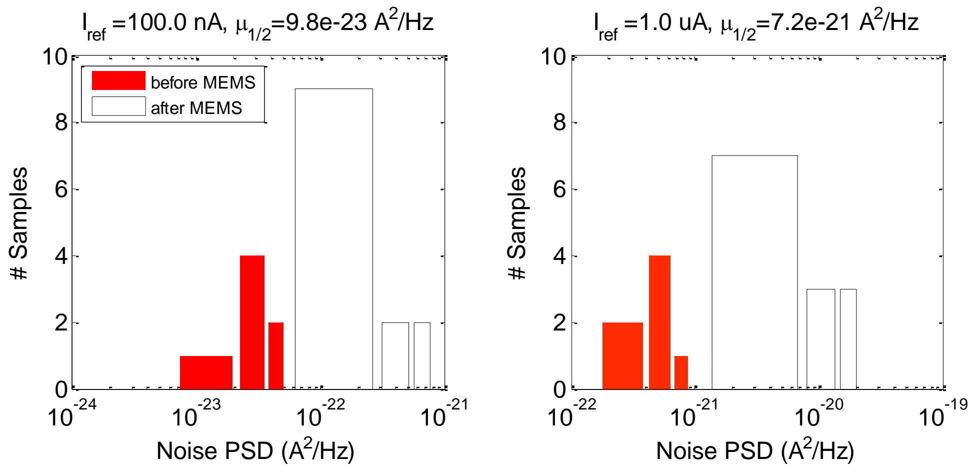


Figure 6. Distributions of the noise PSD before/after MEMS at 100 nA and 1 µA

The noise characteristics of Phase 1 and Phase 2 is compared below.

Table 2. Summary of the noise performance.

	Phase 1				**Phase 2**			
W/L	2 x 68.39 / 0.18 (24.6 μm²)				2 x 66 / 0.2 (26.4 μm²)			
R_{arms}	29 kΩ				38 kΩ			
	Simulation	**no MEMS**	**MEMS**	**Ratio**	**Simulation**	**no MEMS**	**MEMS best/mean**	**Ratio best/mean**
Si(1 Hz) @ 100 nA	2E-23	7E-24	9.3E-24	1.3x	2E-23	3.5E-24	4E-23 / 8E-23	11x / 23x
Si(1 Hz) @ 1 uA	8E-22	3E-22	5E-22	1.7x	5E-22	2E-22	6E-22 / 1E-20	3x / 50x

From the characterization reported above we find confirmation that the noise of the detectors used in Phase 2 is potentially lower than the noise of Phase 1 detectors. The dry bulk micromachining process adopted for post-processing the Phase 2 chips, however, was found to degrade the noise performance to a point where the sensitivity for passive THz imaging would be compromised.

3. Conclusions

The IV and noise measurements performed on the Phase 2 WP3 THz sensors before and after MEMS post-processing were described and compared to those of the previous generation. Simulations based on the PDK parameters were used as reference for the validity of the measurement results. Regular (unprocessed) devices were found to be accurately modeled with standard PDK parameters. The signal offset caused by process mismatch is as expected and it can be cancelled out with the readout circuit designed in WP4. The response of micro-machined devices was shown to be very dependent on the type of MEMS post-processing applied to the chip. In particular, the last release step plays a crucial role due to the difficulty of dissipating the heat of the almost fully released structures. Although the new DRIE based post-processing provides higher array population rate and uniform DC characteristics, as well as better suitability for large scale production than wet processes, it has a greater impact on noise intensity and uniformity than the solution adopted in Phase 1. The noise degradation shown by the pixels processed at die level is large and it considerably degrades the potential THz sensitivity. Care should be taken while performing the wafer level MEMS process in WP5 to limit this effect.