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Research Report

Voltage Drop Compensation for 3D Chip Stacks

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1. Background

There are different methods for stabilizing IC supply voltage such as installing box capacitors on chips on the substrate or on the back surface of the substrate, and forming a trench capacitor internally when the carrier is installed between the chip and substrate. However, these conventional methods have problems related to upper-layer element supply voltage stability due to the operation of the lower layer elements in the three-dimensional layers of semiconductor chips. Exclusive through silicon vias for the power supply may be able to resolve this problem, but if these exclusive through silicon vias for the upper-layer are made on the lower-layer chips, this can cause issues with integration and greatly increase cost. Therefore, technology that can stabilize the power supply for the upper-layer chips without forming via holes exclusively for the upper-layer chips on the lower-layer chips is necessary.

2. Summary of Invention

In order to control voltage drops on the upper layer of stacked Integrated Circuits (IC) chips and to resolve unstable power supply voltage, a silicon substrate with a high-performance thin-film or trench capacitor with many protruding electrodes on the chip surface is connected electronically with the upper-layer of the stacked chip. Semiconductor elements with two or more layers are connected electronically to the silicon elements including the capacitors using the surface electrodes of each chip.

1. Creating a silicon substrate with a high-performance thin film or trench capacitor.
2. Aligning and bonding the exclusive layers of the capacitor with the top layer of the stacked IC chips.
3. Controlling voltage drops in the upper-layer of stacked IC chips.

3. Description

Figure 1 shows the configuration of a three-dimensional stacked IC chips. When 3D stacked chips are used, there is a unique problem where the power supply is unstable for the upper-layer chips. As shown in Figure 1, the supply voltage and ground are provided from the Printed Circuit Board (PCB) to all layers through the silicon vias and bumps. Therefore, when devices for each layer operate at the same time, supply voltage drops caused by sudden current consumption may adversely affect circuit operation. The top layer of the stacked chip has the most unstable voltage supply. However, circuits with large load fluctuations and a large heat value

such as CPUs are usually installed above chips with lower heat values such as for memory. Chips with the largest load fluctuation and largest heat values are installed on the highest layer of stacked chips. Therefore, it is necessary to stabilize the power supply for the upper-layer chips or the top layer chip, and to protect the IC.

This invention proposes a method for installing the silicon substrate with a high-performance, thin-film dielectric capacitor on the top layer of the stacked chip using a soldered joint in order to control supply voltage drops in the upper layer of stacked chips, and to help stabilize the power source. Candidates for the dielectric material are barium titanate and barium titanate zircon. Figure 4 shows the configuration of the IC and capacitor. The bypass capacitor must have low impedance, which is effective at reducing noise, in order to send noise from the power source line to the ground. In the practice of this invention, the VDD and GND are supplied from the exclusive capacitor layer to the IC on another layer. Therefore, the backup capacitor and bypass capacitor are installed as close as possible to the supply bump. It is also possible to install the capacitor that is used exclusively for the capacitor layer on each layer. However, if a large value capacitor is installed on the logic layer, this will reduce the logic occupation area for the wafer, and the overall chip area will increase.

The configurations shown in Figure 2 and Figure 3 can be used for supplying the VDD and GND instead of using the through silicon vias. Figure 2 shows an example of a method for supplying the VDD and GND using a bump instead of the through silicon vias. As shown in figure2, the size of the bumps is so big that the top layer can be connected to bottom layer electrically by using these bumps. Figure 3 shows an example of a method for supplying the VDD and GND to the upper layer chip using wire bonding instead of the through silicon vias or bump.

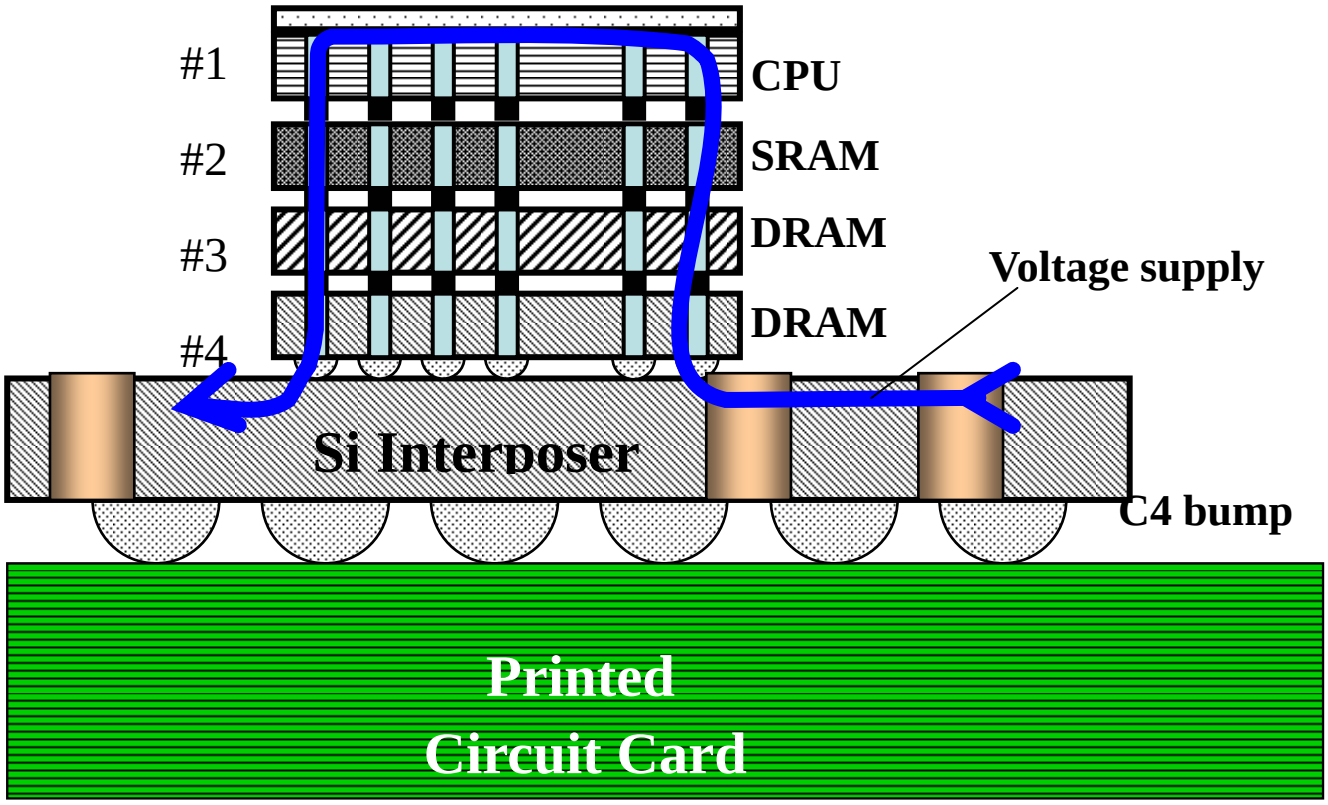

Figure 1. Structure of 3D chip stack.

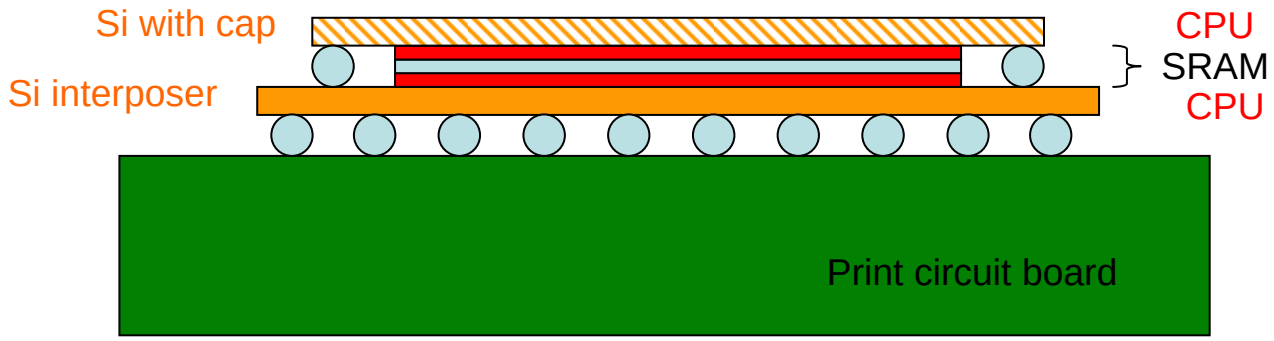

Figure 2. Structure of 3D chip stack with voltage drop compensation layer using large bump.

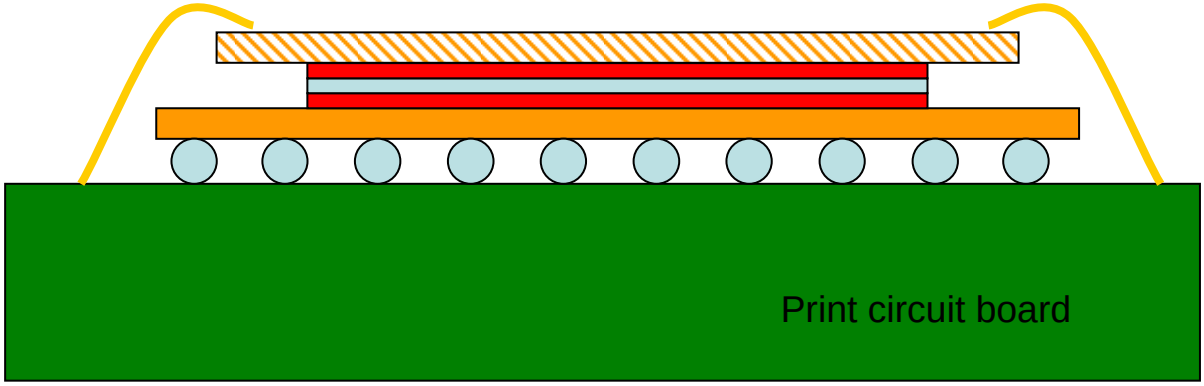

Figure 3. Structure of 3D chip stack with voltage drop compensation layer using wire bonding.

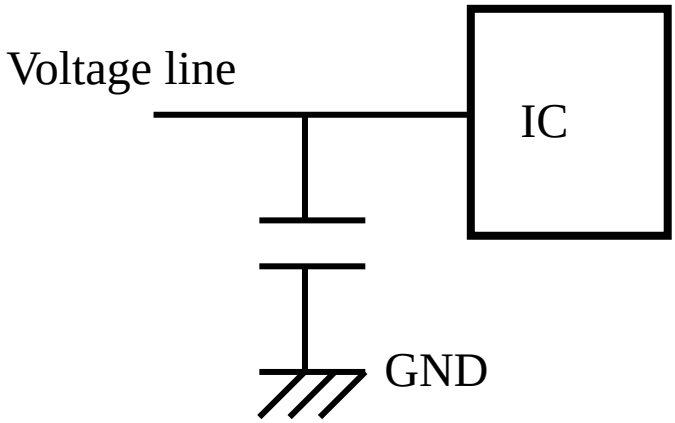

Figure 4. Capacitor for stacked 3D IC.