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Research Report

Vertical Interconnection Technology for 3D Integration

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1. Background

Semiconductor devises have continued to rapidly get smaller with higher integration in following Moore's Law. As a result, performance including speed, functionality, and power consumption has improved while costs have also been reduced. However, as the size of these devises has also decreased (such as 90nm and 65nm), which causes management issues such as increased investment and increased research and development costs, and has also caused technical issues such as increased transistor leakage current. Therefore, it has become more difficult to minimize the size at the same pace as the speed. It is believed that the development of the three dimensional System-in-Package (SiP), which combines multiple LSIs three dimensionally, is an effective solution to these issues.

In the conventional 3D lamination method for LSIs, through silicon vias are created in the silicon, insulation layer is deposited inside of the vias, and a conductive material is deposited using electroplating or a Chemical Vapor Deposition (CVD) to create vertical interconnection wiring. However, this method includes technically difficult processes. For example, metal needs to be deposited in the through-holes with a high aspect ratio. This process also takes much time. It takes time to do alignment, heating and pressure bonding when stacking multiple LSI layers each time. As a result, total throughput of fabricating 3D chip stack is low.

2. Summary of Invention

In this invention, the soldering bumps are inserted into the through silicon vias, and the metallic walls of the vias and the bumps are bonded by heating the soldering material to its melting point in order to establish electrical continuity between the top and bottom silicon. While the bumps are temporarily inserted into the through silicon vias where there are multiple layers, heat is reapplied to complete the bonding vias and bumps in all LSI layers at the same time.

1. Through silicon vias and metallic solder bumps are created in the LSI layer for stack beforehand.
2. Insulation material and the conductive material are deposited on the side walls of the vias. (Manufacturing costs can be reduced because the conductive material does not need to be used for the entire inside of the vias. In the conventional electroplating process, this takes several hours.)
3. Solder bumps made of metal with a low melting point are inserted into the through silicon vias and chips are stacked according to the desired number of layers.
4. Solder bumps are melted inside of the through silicon vias and the metallic walls and bumps bond so that all stacked chips can be bonded at the same time. (The inside of the vias are tapered so that the side walls

can bond easily with the solder bumps and cannot be removed from the holes after bonding. It may be possible to form the vertical through silicon vias and bonded with the metal on the side walls. However, the walls were tapered to have better configuration.)

3. Description

One conventional technique for packaging multiple laminated ICs is wire bonding. As shown in figure 1, when wire bonding is used for connecting upper and lower layers electronically, a problem exists where chips with a large number of Inputs/Outputs (I/Os) and integration circuits for high-speed transmission cannot be stacked because of limitations with the number of I/Os or due to the long length of the wiring. In order to resolve these problems, 3D integrated circuits with vertical interconnections using through silicon via technology was proposed. Figure 2 shows the configuration of a three-dimensional integrated circuit using through silicon vias. In this three-dimensional LSI stack method, vias are made in the silicon and insulation is added inside of the vias. Next, a conductive material is deposited using electroplating or CVD to create vertical interconnection wiring. However, this method includes the difficult process of depositing metal inside of the through-holes with a high aspect ratio. It has also been pointed out that this process takes much time. It takes time to align the LSI between the top and bottom according to the number of stack layers. Heating and pressure bonding also requires time when laminating multiple LSIs. As a result, throughput is low.

This invention proposes a lamination technique where the soldering bumps are inserted into the through silicon vias, and the metallic walls of the holes and the solder bumps are bonded by heating the soldering material to its melting point in order to establish electrical continuity between the top and bottom silicon. Figure 3 shows the configuration of the three-dimensional integrated circuit stacked using this invention. While the bumps are temporarily inserted into the through silicon vias where there are multiple layers, heat is reapplied to complete the bonding at the same time. This is the optimal configuration for avoiding stress to occur due to the mechanical load because the position of the bumps and the vias do not overlap.

1. Through silicon vias and metallic solder bumps are created in the LSI layer for stack beforehand.
2. Insulation material and the conductive material are deposited on the side walls of the holes. (Manufacturing costs can be reduced because the conductive material does not need to be used for the entire inside of the holes. In the conventional electroplating process, this takes several hours.)
3. Solder bumps made of metal with a low melting point are inserted into the through silicon vias and chips are stacked according to the desired number of layers.
Tin, lead, and indium can be used as the solder bump material because of their low melting points. Silver, copper, zinc, and bismuth can be added as a secondary element. The material should be selected based on solderability, strength, and oxidation.
4. Solder bumps are melted inside of the vias and the metallic walls and bumps bond so that all stacked chips can be bonded at the same time. (The inside of the vias are tapered so that the side walls can bond easily with the solder bumps and cannot be removed from the holes after bonding. It may be possible to form the vertical through silicon vias and bond between solder bump with the metal on the side walls. However, the walls were tapered to have better configuration.)

Hitachi has proposed a configuration where the metallic bumps are mechanically pressure welded to the inside of the silicon holes in order to connect chips. The similarity between Hitachi's proposal and this invention is injecting the bumps to the silicon holes. The difference is that, in this invention, the bumps are soldering material, and the solder is melted and bonded with the metallic walls of the holes in order to establish an electronic connection.

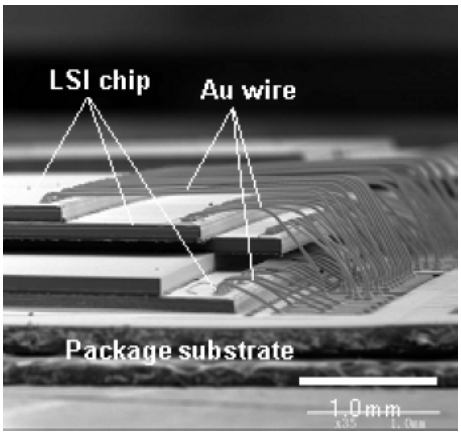
Figure 5 shows a semiconductor manufacturing process using the embodiment of this invention. Figure 6 shows a cross-section of the manufacturing process for a semiconductor device using a semiconductor wafer. In the LSI manufacturing process using the embodiment of this invention, the procedure for the semiconductor wafer manufacturing process is LSI formation, via formation, insulation film for inside via formation, wiring formation inside of the via, connection electrode (microbump) formation, and polishing the back surface of the wafer. After the LSI is manufactured, alignment is made at the wafer level or chip level after wafer dicing, and heat is applied to bond the stacked wafers or chips together. Bumps simply need to be inserted into the through silicon vias, a large load is not needed during bonding whether the wafers and chips are warped or not. This is the optimal configuration for avoiding stress to occur due to the mechanical load even though the position of the bumps and the holes do not overlap.

As shown in Figure 7, It is possible to create stacked wafers and chips by making a space (based on the embodiment of the invention) between the laminated wafers or chips for injecting the adhesive resin (underfill, resin) after 3D integration. In order to achieve this, metal with a high melting point such as copper needs to be deposited up to the desired height during the process before solder bumps are made. This method can be used when the installation material is used for filling the inside of the holes.

Connection is made electronically and mechanically by melting the bump inside of the through silicon vias. However, when the mechanical strength of the whole laminated wafer or whole laminated chip after lamination is increased, it is also possible to use the exclusive bumps and through silicon vias. In such cases, metallic layers are needed inside of the through silicon vias for bonding with the bumps, but it is not necessary to accumulate this metallic layer up to the front surface of the wafer. As shown in Figure 8, the bumps and through silicon vias need to be prepared around the chip or inside of the chip. In order to expand the contact area between the bumps and through silicon vias that are connected electronically, it is also possible to use bump and via layouts with different shapes (circles, squares, rectangles). Figure 9 shows another example using the embodiment of this invention.

■ Effect of the Invention

In this invention, it is not necessary to completely fill the inside of the through silicon vias with conductive material prior to stack. Therefore, it is possible to manufacture stacked wafers and chips with lower cost and lower TAT. This invention allows for bonding at the same time, which greatly reduces the lamination process time.



Conventional 3D stacked SiP using wire bonding

Problems: Additional bonding area on the substrate and long wires for connecting a chip to a substrate, limited I/O

3D with Through-Silicon-Via (TSV) holes + microbumps

Figure 1. Background of 3D LSI

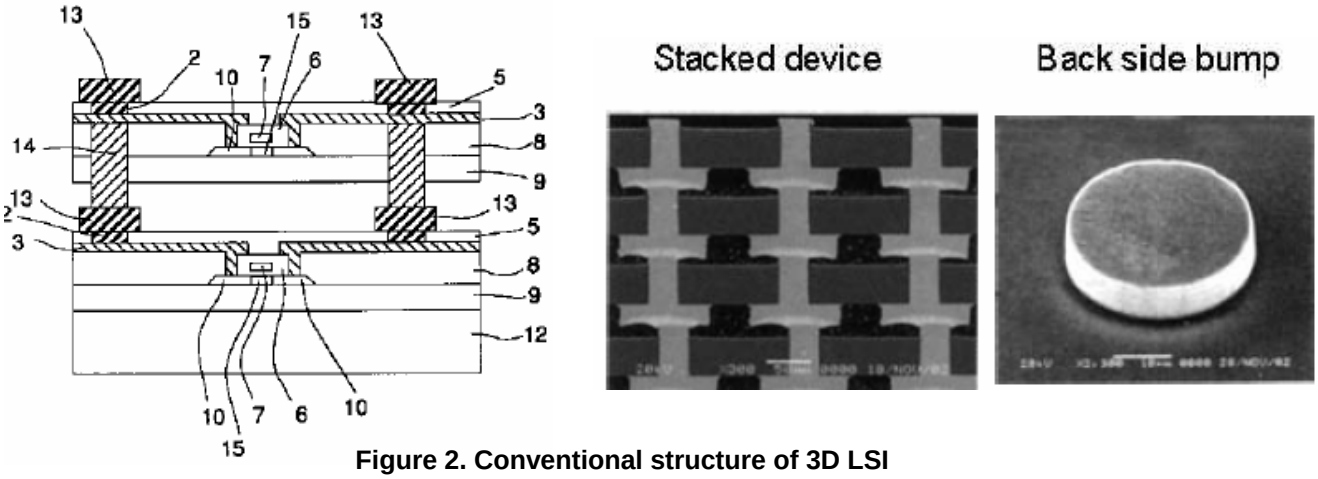


Figure 2. Conventional structure of 3D LSI

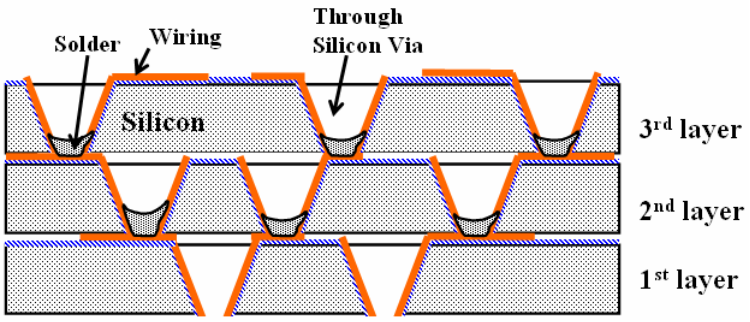


Figure 3. New vertical interconnection configuration.

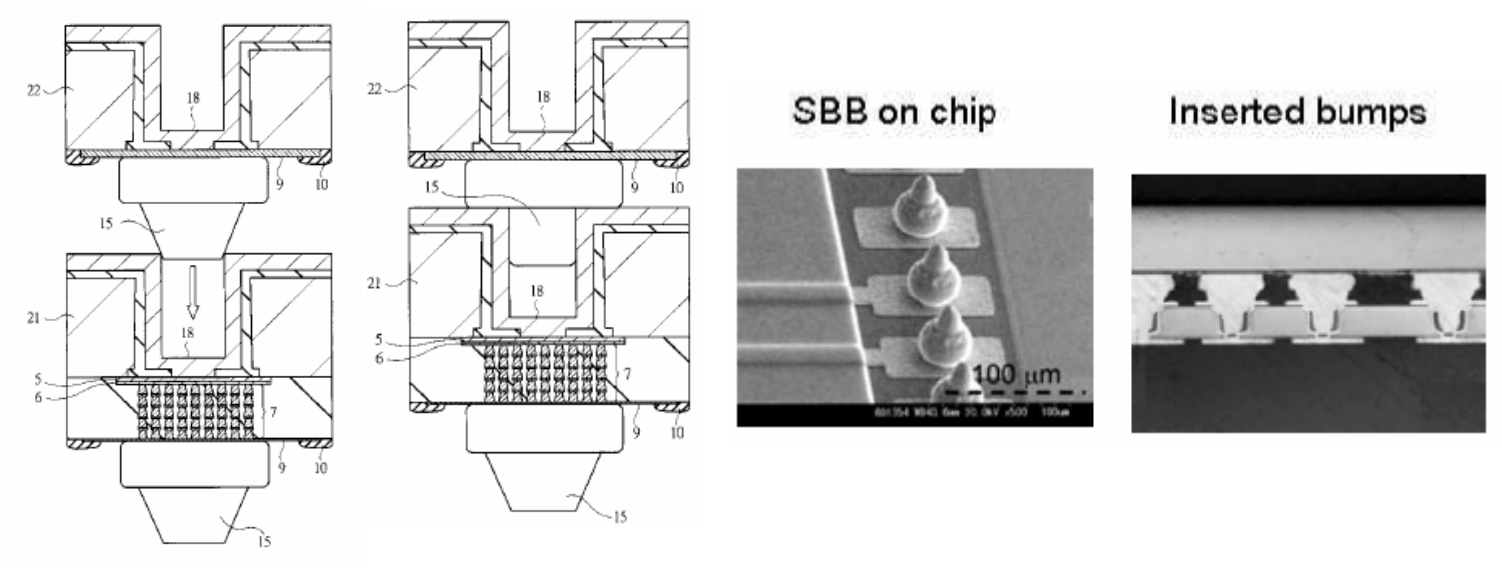


Figure 4. Structure of 3D LSI proposed by Hitachi

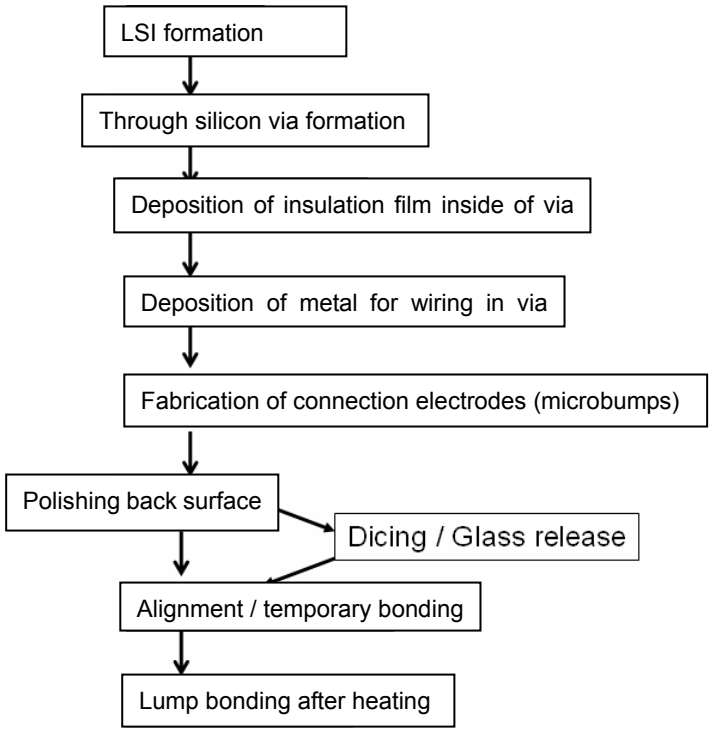
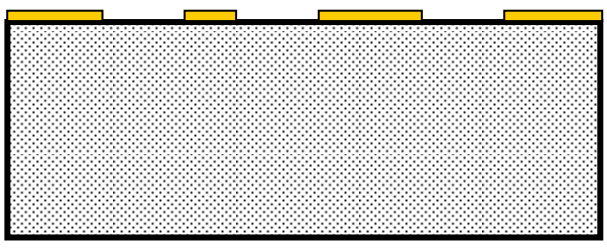
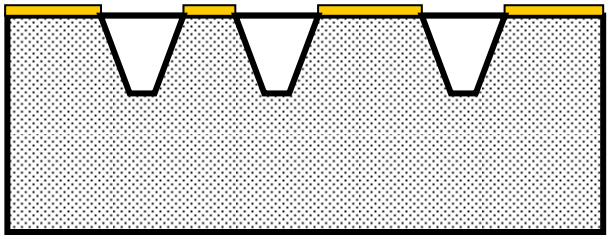


Figure 5. Fabrication process



(1) Lithography



(2) Si etching using Deep-Reactive Ion etching (RIE)

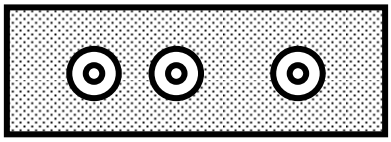
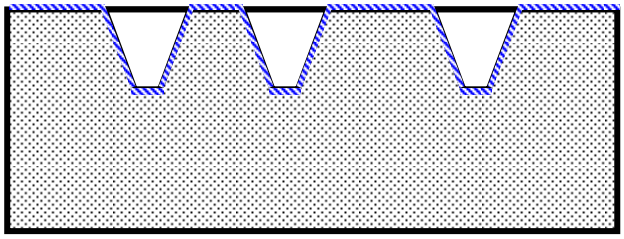
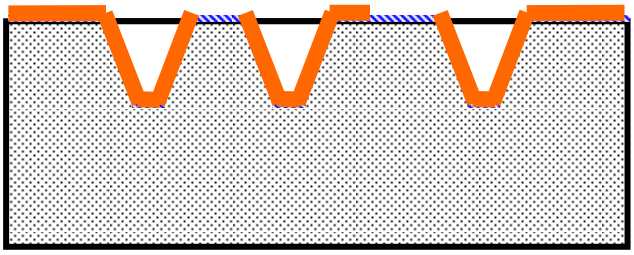


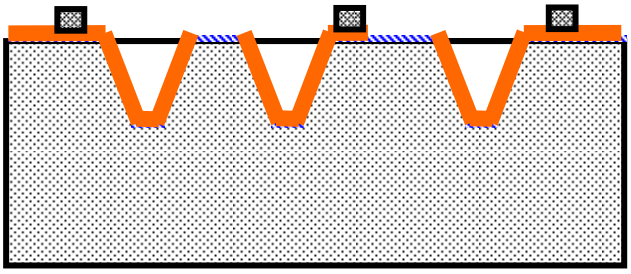
Fig. Top view



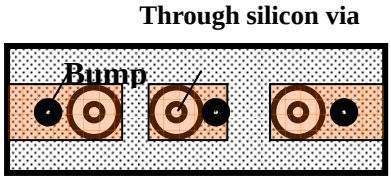
(3) Deposit isolation layer



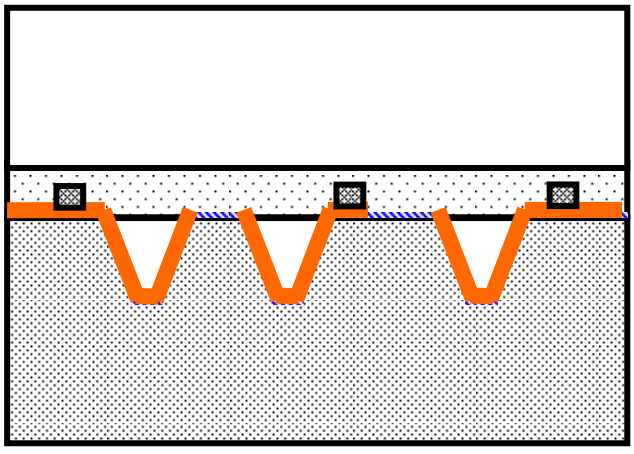
(4) Metal layer deposit and etching



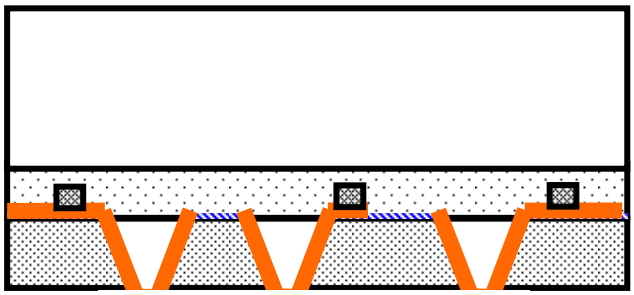
(5) Solder bump fabrication



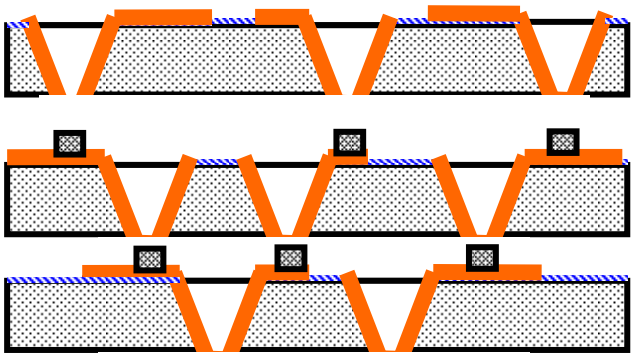
Top view



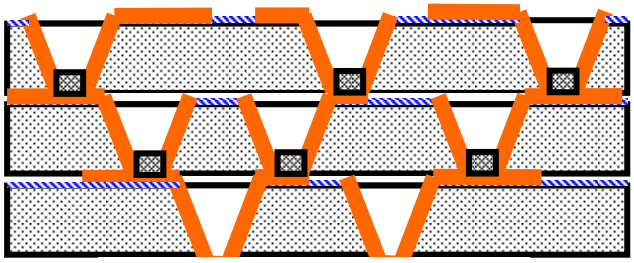
(6) Supporting glass or silicon attach



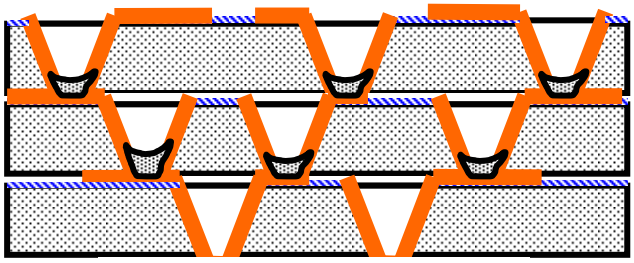
(7) Backside grinding and CMP, backside process



(8) Align stack layers



(9) Bumps are inserted inside vias and layers are temporary fixed



(10) After heating, solder bumps joint with TSVs

Figure 6. Fabrication process (Cross section)

Through silicon via (TSV) holes need to be tapered and the TSV holes are bigger than with 3D LSIs. However this technology also can be used for packaging level 3D. This process does not require underfill.

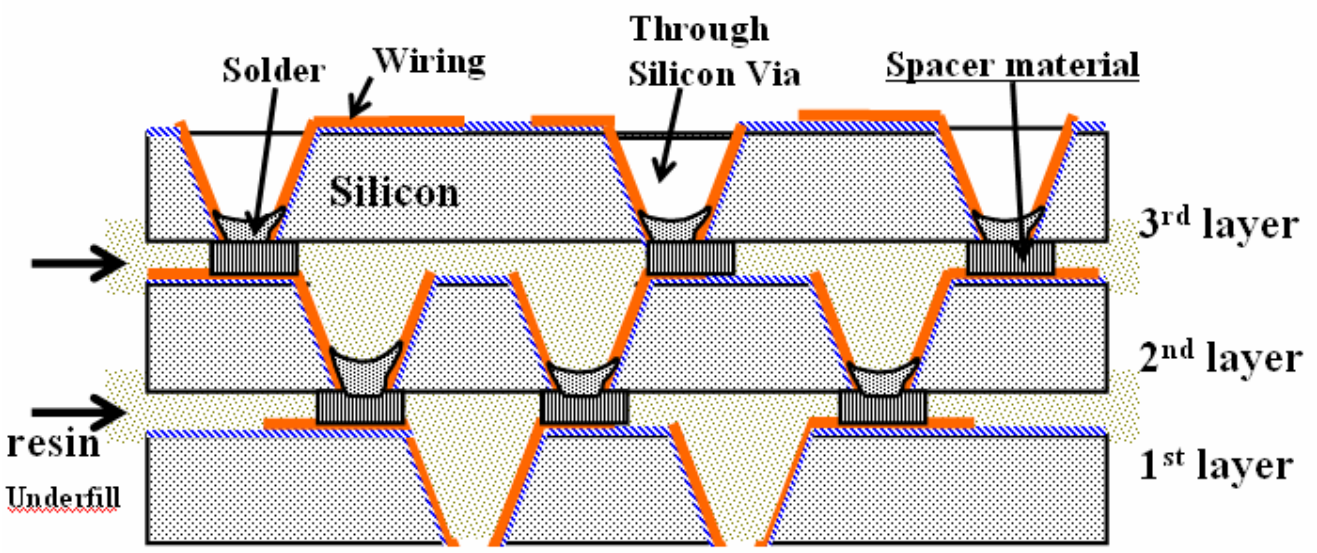


Figure 7. Three-dimensional integrated circuit using vertical interconnection with spacer material.

Figure 8. Sealing layout as additional strength for three-dimensional chip stack.

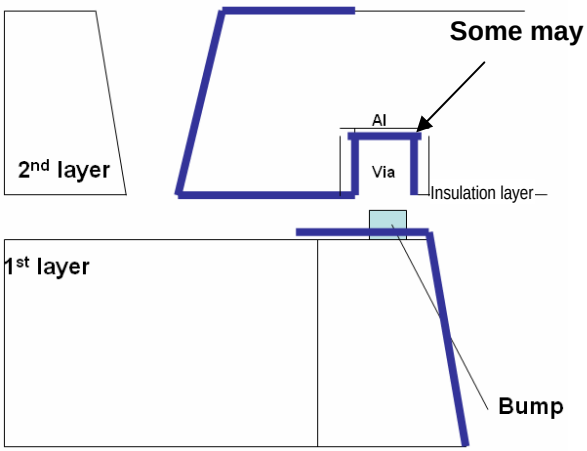


Figure 9. Example of different bonding method.