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Research Report

Driving Circuit for 3D Chip Stacks

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1. Background

Figure 1 shows the configuration of a three-dimensional chip stack. Three-dimensional chip stack can be used for stacking mixed devices in addition to stacking the same devices. As shown in Figure 1, the supply voltage and ground are supplied to all layers by the Printed Circuit Board (PCB) through silicon vias and bumps (in some cases, through a silicon interposer). When three-dimensional chip stack are used, the power source is usually provided from the lower layer where the PCB is located. Therefore, there is a unique problem that occurs with stacked chips where the chip on the top layer is unstable due to the power supply. Another problem is that when the devices for each layer operate at the same time, the current is concentrated on the power supply wiring, and power source voltage drops that occur during sudden current consumption can greatly affect the circuit operation of each layer. If a circuit with large load fluctuation and a large heat value such as a CPU or MPU is laminated and operates, it is necessary to stabilize the supply voltage for the whole stacked chip.

2. Summary of Invention

In this invention, the operation signal of each layer in a stacked semiconductor chip starts at different times in order to avoid concentrated current consumption. When the chips for each layer operate at the same time, the current in the power source wiring is concentrated, which can result in large voltage drops in the power supply layer, which in turn can affect circuit operation. Therefore, the operation start time for each layer is staggered in order to reduce supply voltage fluctuation so that input/output characteristics can be stabilized. The delay time for each layer is set beforehand and the order for layer startup can be changed freely. .

1. The operation time and delay for each layer is determined beforehand, and the settings are saved to the setting register in each layer.
2. The operation start signal is sent to each layer.
3. Values in the register are read by the sequencer and the operation start signals are input to the control circuit after the set delay time.
4. Each circuit begins operation according to the delay for each layer.
5. The operation start signal for each circuit of each layer is staggered so that it is possible to avoid concentrated power consumption.

3. Description

When a three-dimensional integrated circuit is used, power for the stacked circuit layers may be unstable because the power is supplied only from the bottom due to its configuration. The circuit layer on the top is especially affected because it is located farthest from power supply. Figure 7 shows the power line of a three-dimensional integrated circuit. When the circuits for each layer operate at the same time, the current is concentrated on the power supply wiring, and power source voltage drops that occur during sudden current consumption can greatly affect the circuit operation of each layer.

The purpose of this invention is to supply stable supply voltage and extend the lifespan of the vertical wiring by delaying the start time of different circuit operations of each layer and also by dispersing the peak current using staggered power consumption.

Figure 2 shows the configuration of the driving circuit, which is installed on each layer. This consists of an interface circuit, which outputs the operation delay signal, and a control circuit. Figure 3 shows the configuration of the interface circuit shown in Figure 2. Data related to the operation delay time for each layer is stored in the settings register. Operation delay times are measured by the counter in the interface circuit. The sequencer in the interface circuit outputs the operation start signal according to the delay that is set by the counter output. The control data signal is input in addition to the external clock and exclusive strobe signal to the interface circuit. The control data signal contains serial data, and usually, only the operation start signal is sent for each layer. However, it can also send other data. In this case, the data is processed as Flag n by the control circuit as shown in Figure 4. When it is difficult to read the data using the external CLK, it is possible to use the strobe signal with a frequency that is different from the external CLK instead of using the external CLK. The control data signal is read every time the strobe signal or CLK starts up. The read signal is used by the control circuit in the driving circuit shown in Figure 2. The delayed operation start signal is also used by the control circuit. Figure 4 shows the relationship between the strobe signal or CLK and control data signal. The control data signal starts at the start bit, which is when data begins, and then the operation start signal follows. The number of bits that needs to be sent is determined and then is sent. Figure 5 shows the delay status for the operation start for the start flag (operation start signal). Regarding the operation start delay for each layer, when the start flag is 0, the sequencer starts the counter, and the counter begins the countdown. When the countdown reaches 0, the operation start signal is activated. By setting different values for each layer in the register, it is easy to control the operation start time for driving a particular circuit in the layer through the controller circuit. Figure 6 shows an example of when different operation start times are set for each layer. This operation start delay time and the order for the delay can be changed according to the application of each layer. Therefore, by setting the optimal delay times beforehand, it is possible to achieve stable operation so that the peak consumption current is dispersed. For example, by using this invention, the memory refresh operation time for an application on a layered memory can be staggered. Also, when different application circuits for different layers start up at the same time and all pixels of an image sensor are accessed at the same time such as in a photo detector, the consumed current will be concentrated. Therefore, it is better to use the circuit to delay the start operation. Fig 8 shows a configuration of 3D chip stack with different applications in which this invention can be used.

If the same applications are installed on each layer and certain circuits are the same, it is easier to install the circuit for each layer.

When communication is made between each layer, it is necessary to return the operation start times for each layer that were delayed back to the original time. These times must be returned back the same amount as the delay time by making an output latch.

■ Effect of the Invention

When different devises are stacked, the operation start times are adjusted for each layer and the peak of the consumed current is dispersed so that stable power supply voltage can be ensured for the whole laminated chip. The failure time for wiring is in proportion to the inverse of the current density to the nth power. Therefore, by avoiding concentration of the power consumption current, the lifespan of the vertical interconnection wiring can likely be extended and failures can be reduced.

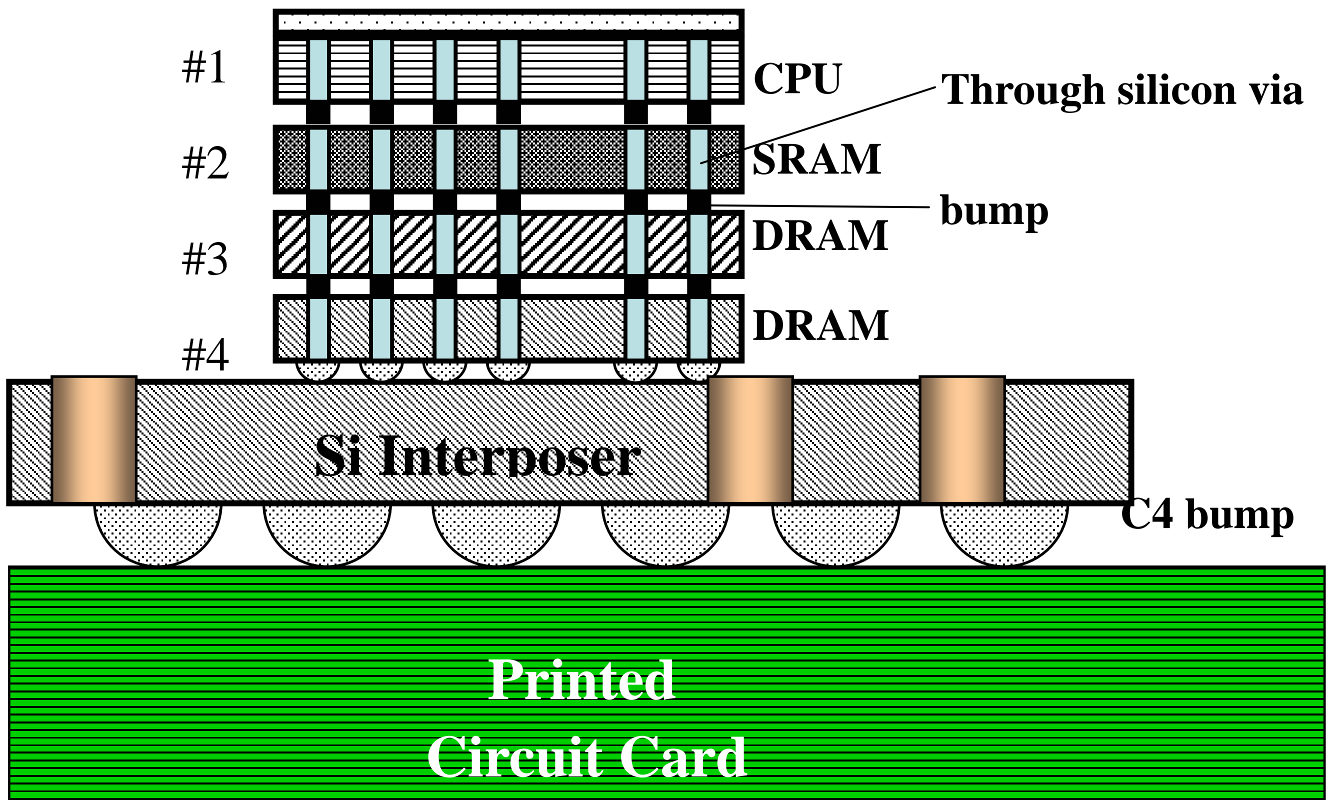


Figure1. Structure of a 3D chip stack

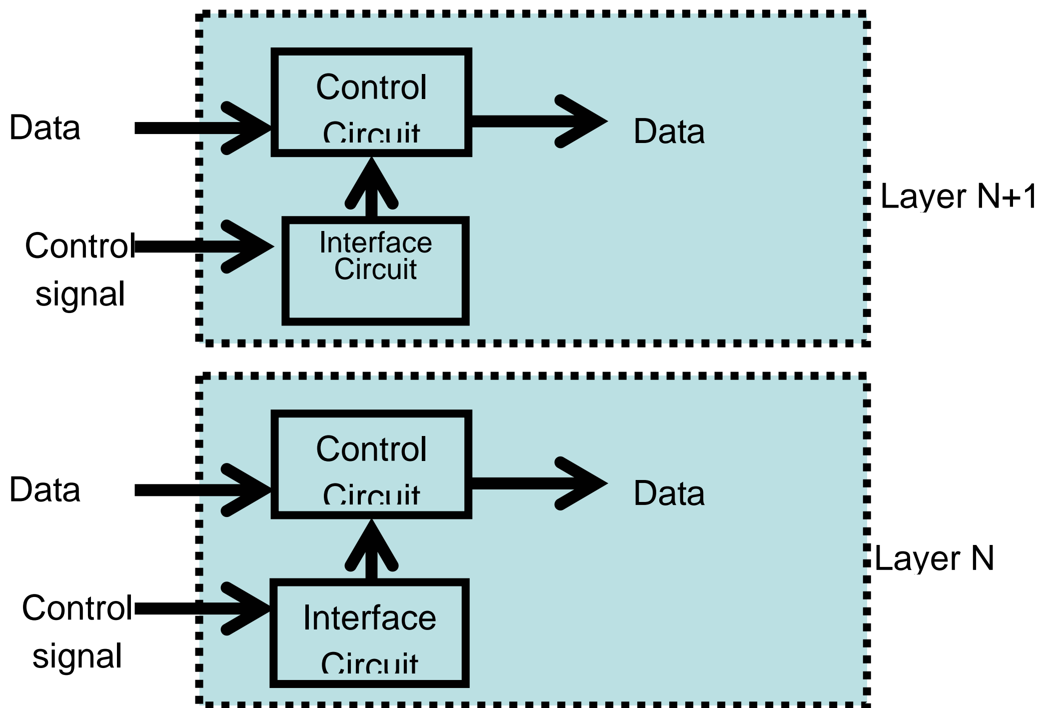


Figure 2. Driving circuit

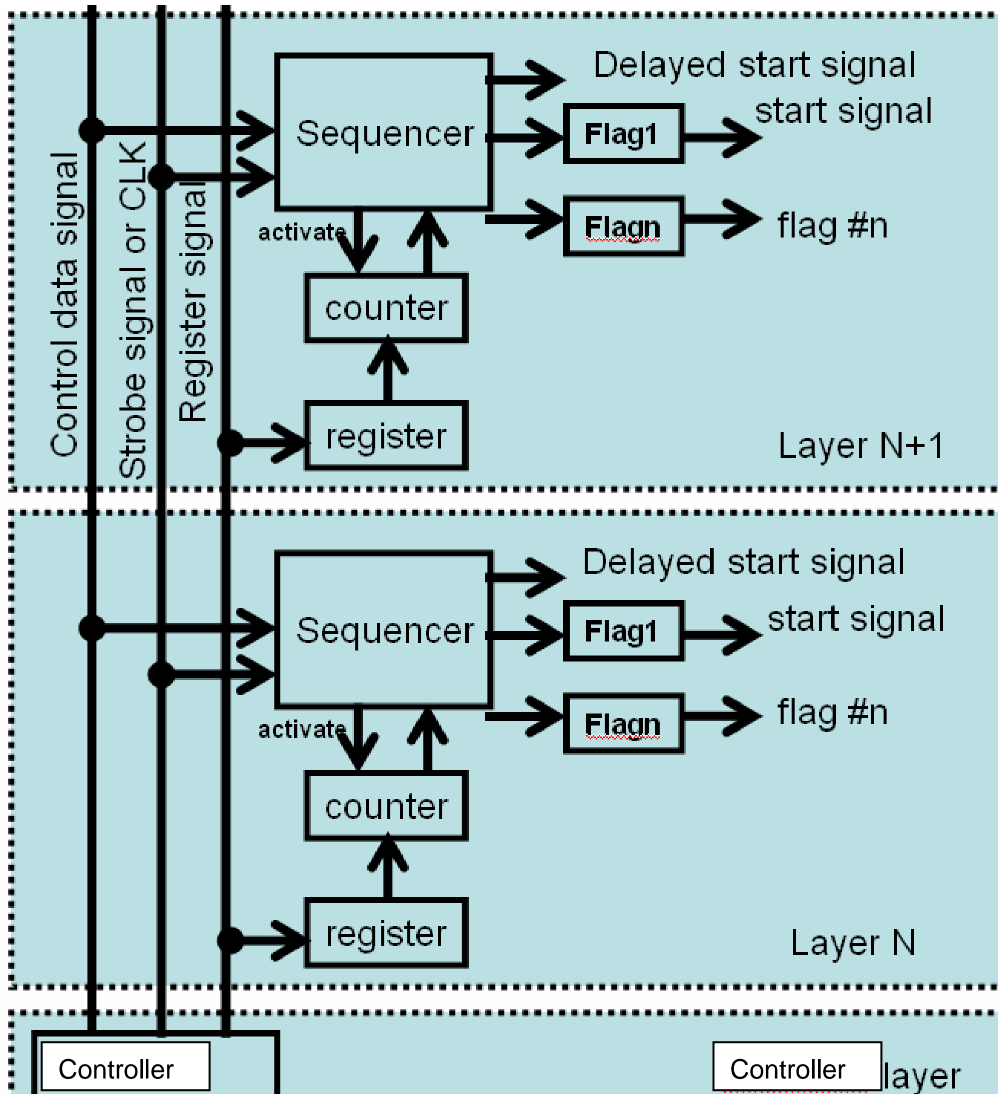


Figure 3. Interface circuit

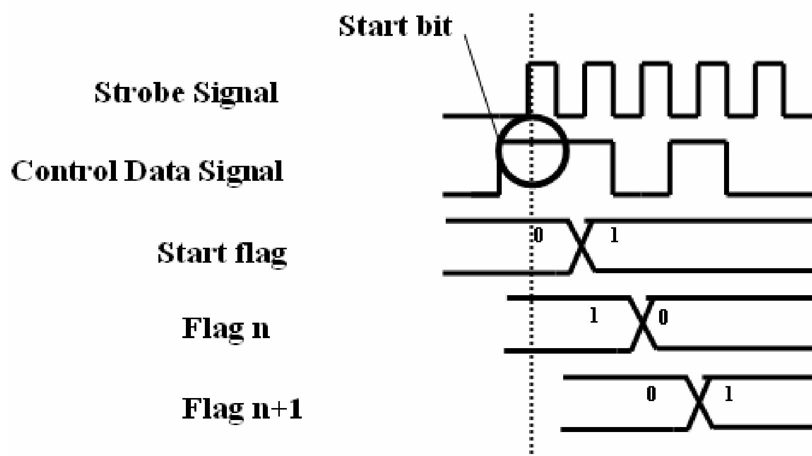
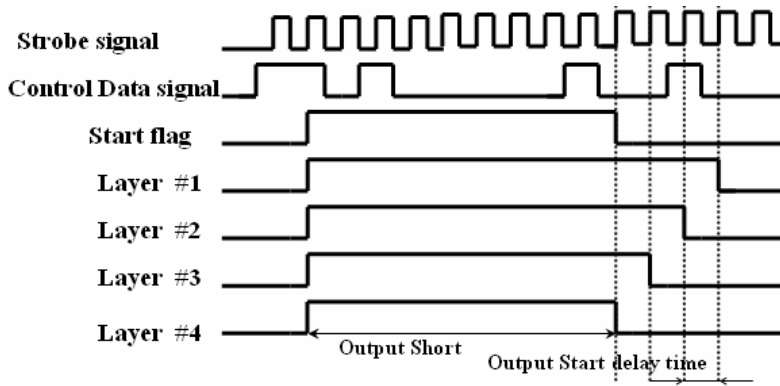
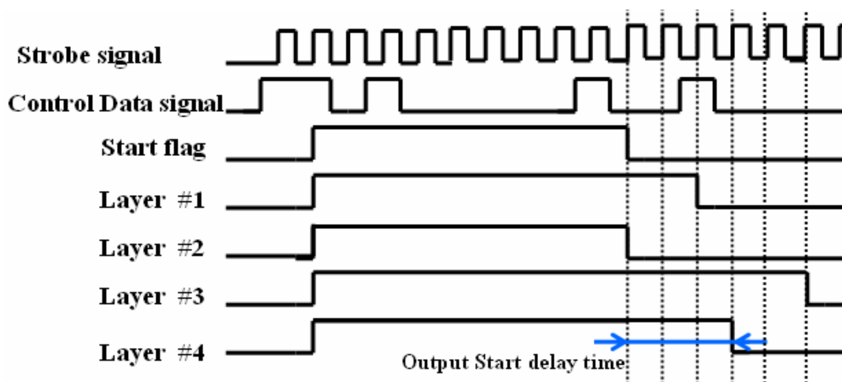


Figure 4. Strobe signal and control data signal.



Layer number	Contents of setting registers
#1	3
#2	2
#3	1
#4	0

Figure 5. Delayed start signal in each layer according to the table value.



Layer number	Contents of setting registers
#1	2
#2	0
#3	5
#4	3

Figure 6. Delayed start signal in each layer according to the table.

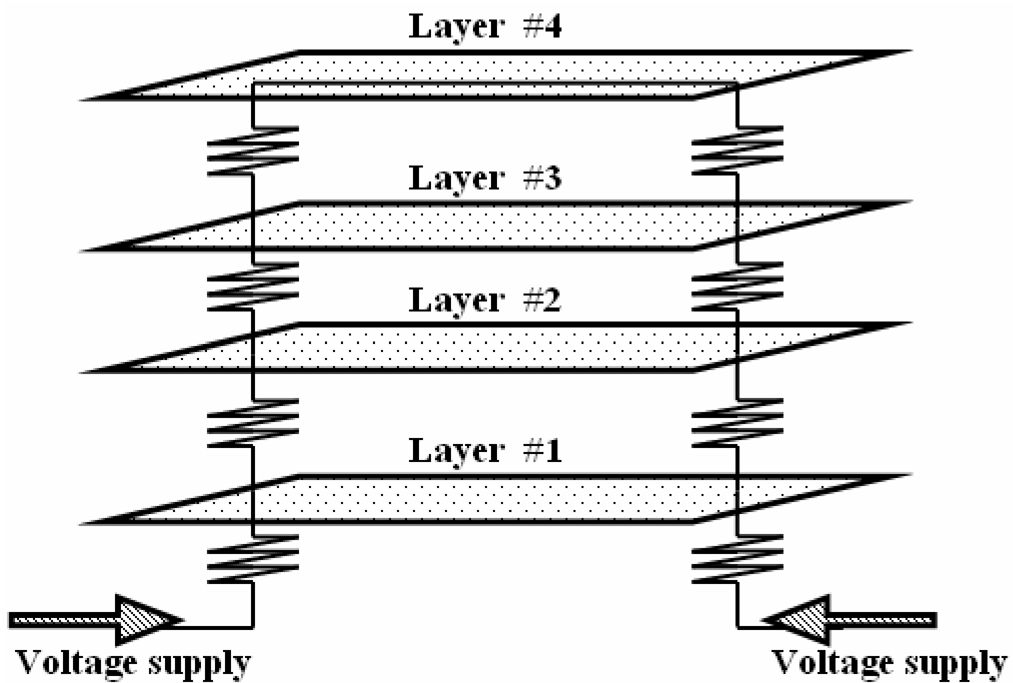


Figure 7. Voltage line in each layer of the 3D chip stack.

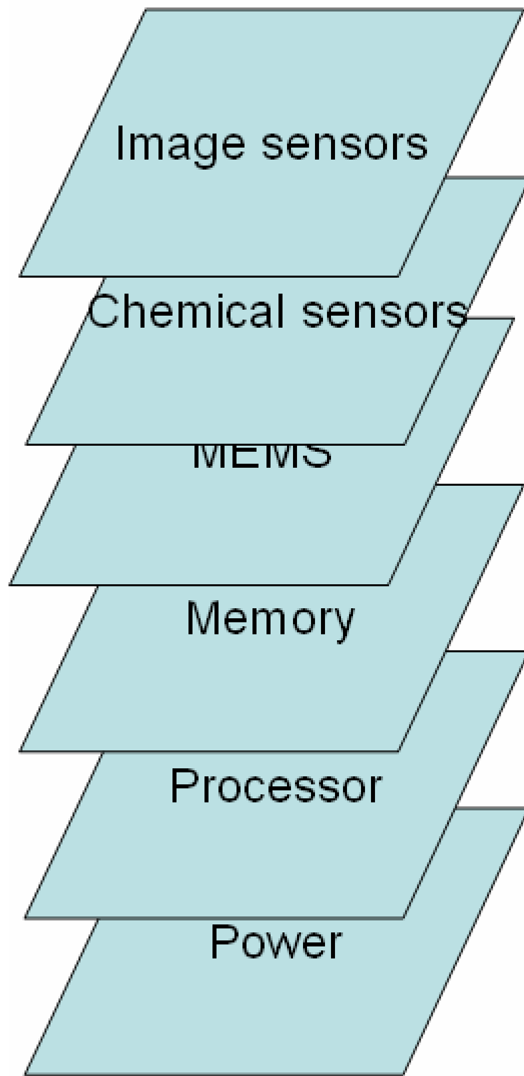


Figure 8. 3D chip stack with different applications.