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Research Report

Alignment Technology for 3D Chip Stack

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1. Background

There are three types of three dimensional integration processes; the Chip-to-Chip process, Chip-to-Wafer process, and Wafer-to-Wafer process. In Japan, Chip-to-Chip processing is further advanced than the other two processes due to the package orientation. However, technology verification and new technology development in the Chip-to-Wafer and Wafer-to-Wafer processes have not advanced much due to certain issues (yield and costs) despite studies being conducted.

2. Summary of Invention

This invention proposes a new low-cost, high-throughput Chip-to-Wafer 3D chip integration technique and a technique for high-precision auto alignment using soldering surface tension. Soldering bumps for alignment is prepared and temporary alignment is made using soldering surface tension. Next, bumps for signals are bonded to execute automatic alignment in micron order. Devices that are used for lump lamination for multi layer stacking include a vibration function and are used to temporarily bond the supports for inserting chips in the cavity with the alignment solder. This alignment method using solder is not limited to bonding methods that use a cavity.

(a) Chips are inserted into the cavity.
(b) Alignment bumps are melted using heat.
(c) Alignment can be executed using soldering surface tension. At this time, the bumps for signals, power source, and grounding are not connected to the pads.
(d) A load is given to the contact between the pads and the bumps for signals, power source, and grounding. The bumps are then bonded by heating the bumps for signals, power source, and grounding to their melting point.

3. Description

The flip-chip bonding method is used for conventional Chip-to-Wafer bonding. In the flip-chip bonding method, after alignment between the protruding terminals referred to as the bumps, which are laid out in an array, and pads on the substrate is made, heating and pressure bonding is executed when each chip and substrate is electronically connected. Therefore, when multiple chips are stacked, the alignment and heating/pressure bonding processes need to be repeated according to the number of stacked chips. Also, when the stacked chips are manufactured in an array on a wafer, these processes need to be executed repeatedly according to

the number of chips in the array. As a result, this conventional method requires much time for executing alignment and heat/pressure bonding processes, and has throughput is low.

This invention proposes a new low-cost, high-throughput Chip-to-Wafer 3D chip integration technique and a technique for high-precision auto alignment using soldering surface tension. Soldering for alignment is prepared and temporary execute automatic alignment is made using soldering surface tension of alignment bumps. Next, fine pitch signal bumps are bonded to execute automatic alignment in micron order because automatic alignment was already executed by alignment bump.

Figure 1 shows the chip cavity used for this new Chip-to-Wafer chip lamination technique. The cavity is a hole where the chips are inserted and can be used as a standard for alignment when the chips are stacked. It also holds the chips so that they do not slide laterally during the heating/pressurizing process for bonding. When the cavity is used for chip stack, chips that are inserted into the cavity according to the number for stack, heat and pressure are applied, and the laminated chips are created. By using the cavity as the standard surface for alignment, it is not necessary to execute a process for aligning the cavity and each chip that is above or below the cavity. Therefore, it possible to stack multiple chips at the same time. When the stacked chips are created in an array on the wafer, all processes can be executed together by using cavities laid out in the shape of the array. Therefore, manufacturing throughput is greatly improved, and devices with alignment functions are no longer needed. As a result, three-dimensional stacked chips can be manufactured at a lower cost. However, the chip-to-wafer 3D integration technique with cavity technology has challenges of fine pitch alignment. There is a difference in size between the cavity and chip so that multiple chips can be easily inserted into the cavity and so that the template can be easily removed after chip stack. And the difference in size between the cavity and chip may restrict fine pitch alignment. Figure 2 shows the misalignment of the chips that occurs inside of the cavity.

Figure 3 shows the process for self alignment when chips on multiple layers are laminated at the same time, which is one of the embodiments of this invention. The template that contains the cavities is temporarily bonded after the chips and wafers for lamination are aligned. Figure 3 (a) shows the chips being inserted into the cavity, and Figure 3 (b) shows the misaligned overlapping chips in the cavity. In this case, the template with the stage and cavity is vibrated so that the chips will be aligned without touching the side walls. Figure 3 (c) shows the bumps for alignment melted by heat. Here, the bumps for alignment use solder with a lower melting point than the bumps for the signals. Alignment is executed using soldering surface tension. The large bumps for alignment are taller than the height of the bumps for signals, power source, and grounding and wider than the size of the bumps for signals, power source, and grounding. Therefore, it is possible to execute self alignment for the signal bumps even if there is misalignment by over one signal bump pitch. At that moment, the bumps for the signals, power source, and grounding are not connected with the pads. The bumps for alignment and the smaller bumps for signals and power source can be made from the same material. Figure 3 (d) shows the load given to the contact between the pads and the bumps for signals, power source, and grounding. The bumps are then bonded by heating the bumps for signals, power source, and grounding to their melting point. The bumps for alignment may contact with the signal bumps where they are close together because the alignment bumps are compacted. Therefore, it is necessary to install the signal bumps where they cannot be bridged when the alignment bumps are compacted, or to configure the chips so that the alignment

solder bump overflow can be released.

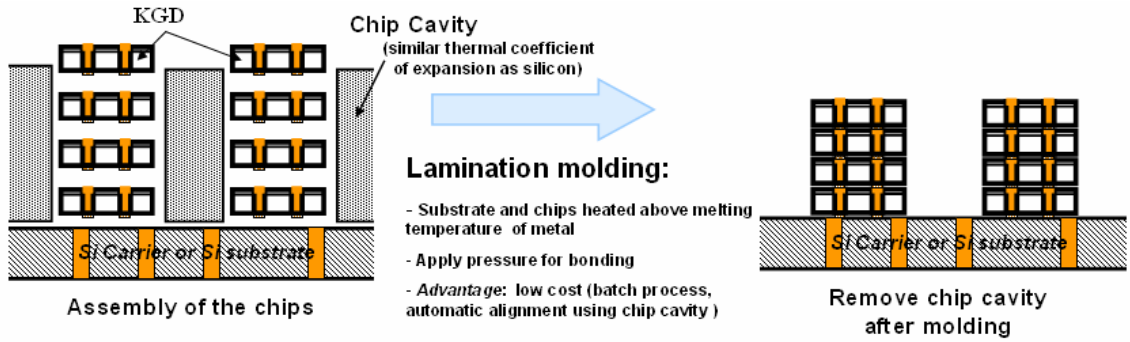


Figure 1. Chip-to-Wafer bonding technique using the chip cavity method.

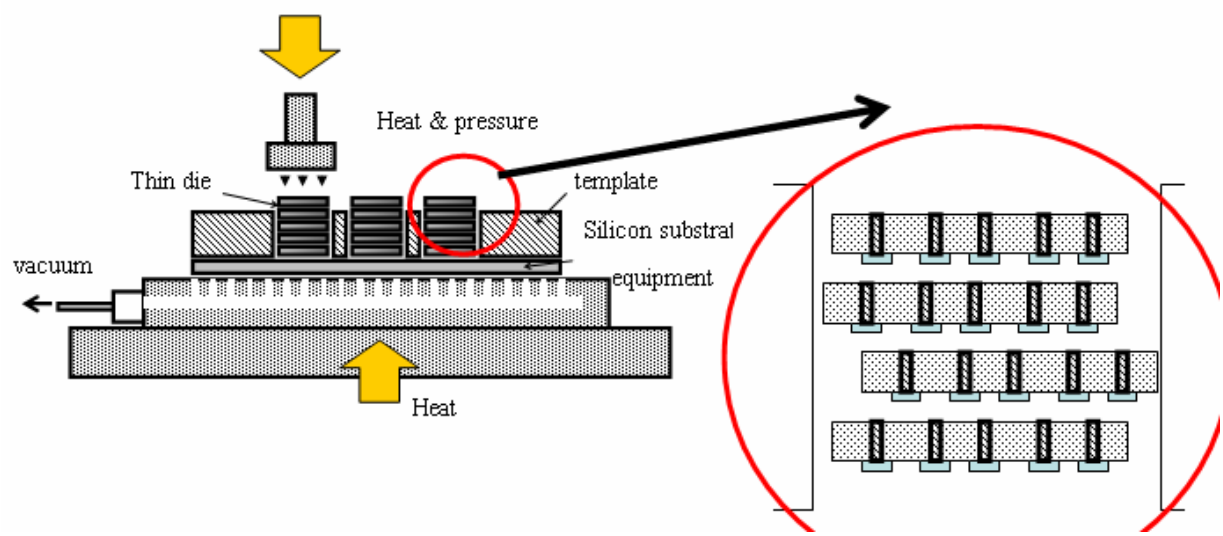
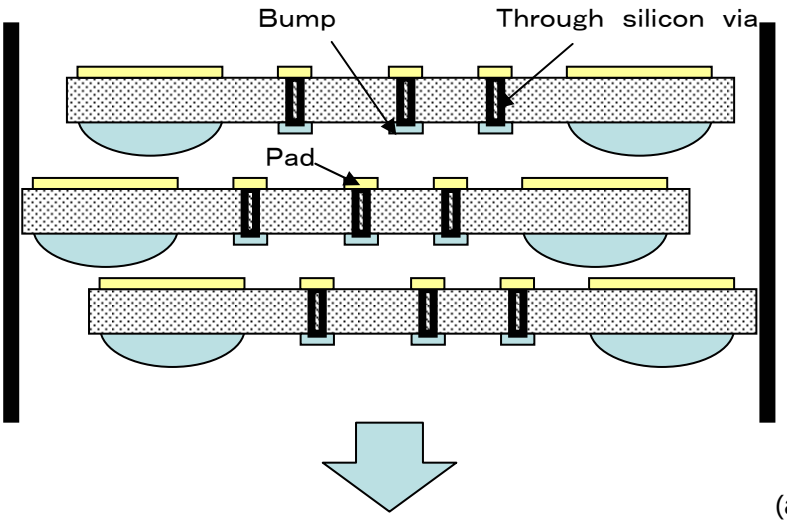
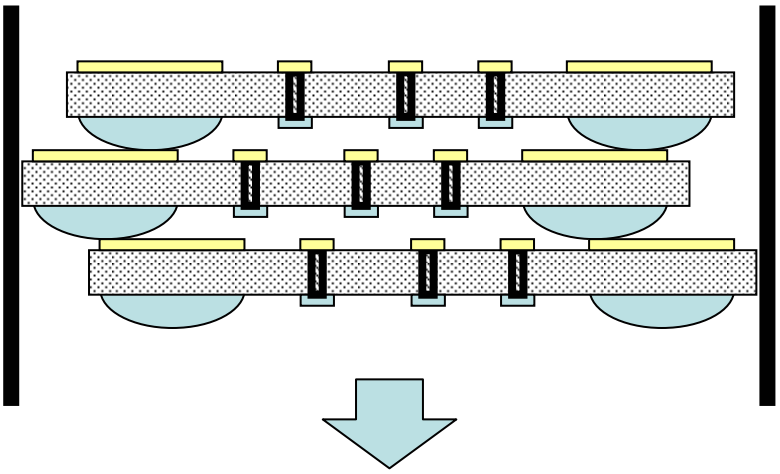


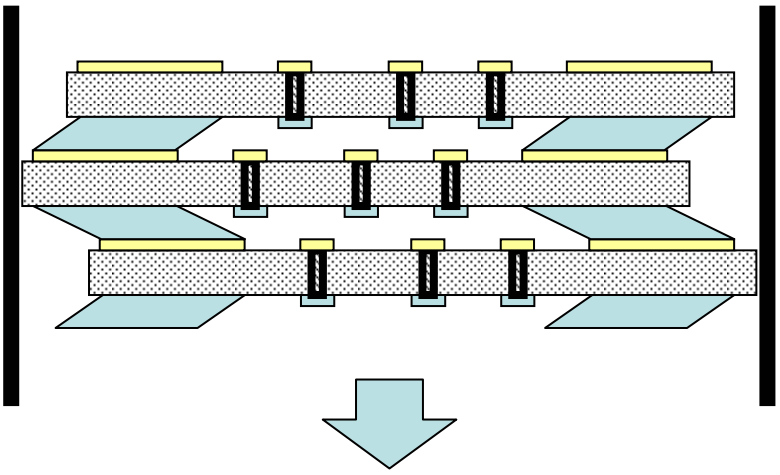
Figure 2. Chip misalignment inside of the cavity.



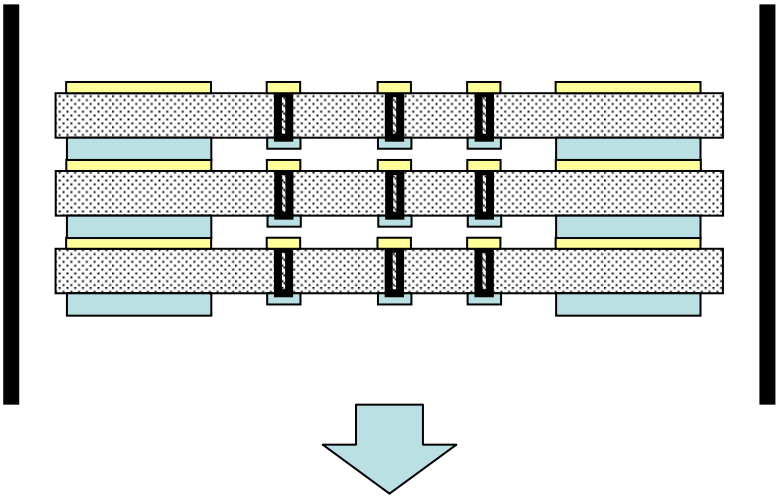
(a) Chips are inserted into the cavity.



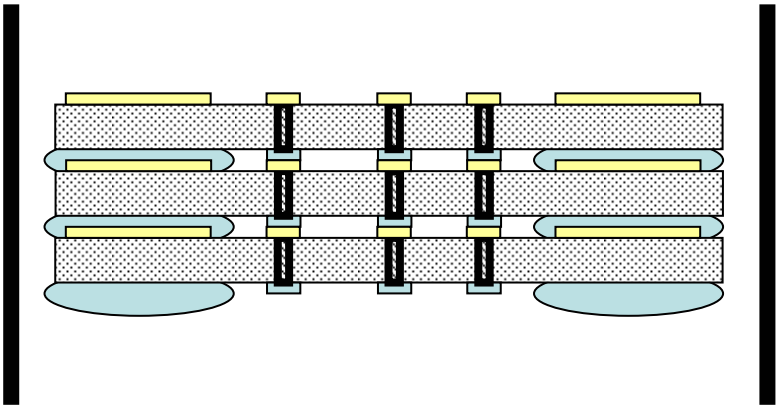
(b) Laminated chips in the cavity are misaligned.



(c-1) Alignment bumps are melted using heat.



(c-2) Alignment can be executed using soldering surface tension. At this time, the bumps for signals, power source, and grounding are not connected to the pads.



(d) A load is given to the contact between the pads and the bumps for signals, power source, and grounding. The bumps are then bonded by heating the bumps for signals, power source, and grounding to their melting point. The alignment bumps are compacted and expand, so configuration for the chips should be made so that the solder overflow can be released.

Figure 3. Self-alignment process for stacking multiple layers of chips at the same time.