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Research Report

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High-Resolution AMLCD made with a-Si:H TFTs and with an Al-Gate and IZO Last Structure

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1. Abstract

Using a low-cost a-Si:H-TFT process with an Al gate and IZO last structure a direct-view active matrix display with the highest information content has been fabricated in a phase-2 mass production line in DTI Himeji. The display, a 16.3" diagonal 200ppi-QSXGA (Quad SXGA) incorporates 7680 columns and 2048 rows. Each subpixel measures 42μm(h)x126μm(v).

2. Introduction

Recently, the market for desktop monitors based on a-Si:H-TFT active matrix display technology has increased rapidly and has great potential for further growth. Active matrix displays combine the advantages of flicker free images, low power consumption, and no radiation emission with excellent form factors and light weight compared to CRTs. Furthermore, in terms of image content, the active matrix display technology has clearly the capability to go far beyond what is possible with CRTs. Despite these advantages, there is continuous pressure to further reduce the cost of active matrix displays to be competitive compared to other technologies, especially the CRT. Most of the desktop monitor active matrix displays which will be sold in the year 1999 or 2000 will have XGA or SXGA format and will therefore compete directly with cheap CRTs. One of the most efficient ways to reduce array fabrication cost is the reduction of the number of lithographic processing steps. An Al-gate reduced mask process with a back-channel cut type TFT has been described by Samsung[1]. Planarized reduced mask back-channel cut type TFT processes have been described by NEC[2] and OIS[3]. In these processes, the transparent conductor layer is patterned last to form the pixel electrode. For high resolution and high information content displays, a low resistance gate metal such as Al is needed along with shorter channel length TFTs than are typically used in current a-Si AMLCDs. In a previous publication[4] we have described a QSXGA display which was built on a research pilot line using a 6-mask process with inverted staggered trilayer type TFTs. In this work we have shown that color QSXGA desktop monitor displays can be successfully fabricated in a mass production line using a reduced mask process with an Al gate line and an IZO last structure. The 16.3"-QSXGA active matrix arrays were fabricated on 360 x 465 x 1.1 mm substrates using trilayer type TFTs. Novel process steps included the use of an Al(Nd) alloy[5,6] for the gate metal to avoid hillock or whisker formation and Indium Zinc oxide (IZO) as the transparent conductor material since it can be etched without attacking Al[7]. The design of the unit cell is described and the results of process characterization test sites summarized.

3. Design

For the QSXGA design using the Al-gate and IZO last process, gate line resistance, TFT performance, and the interconnection

resistance have to be carefully considered. From the QSXGA design with the 6-mask process [4] it was shown that an R_s of 0.18 Ω/sqr. for the gate lines provided sufficiently short RC delay times. Al(Nd) gate metal with an R_s of 0.124 Ω/sqr. will improve the shape of the gate pulses. Assuming more uniform TFT performance with an average mobility of 0.7 cm^2/Vs the pixel TFT's W/L size was designed to be 10 μm/8 μm in order to provide more tolerance in the drain/source overlap on the I-stop (the I-stop is the insulator in a trilayer type TFT which defines the channel region). This TFT size assures chargeup within the 6 μs gate line pulse to any gray level with dot inversion. Figure 1 shows the unit cell layout design for the Al gate and IZO last process using a C_s-on-gate design. Each pixel needs two vias to open the passivation to the data metal, one on the storage capacitor and another at the TFT's source contact. The data line width is 5 μm except for the crossover region where the width is 7 μm.

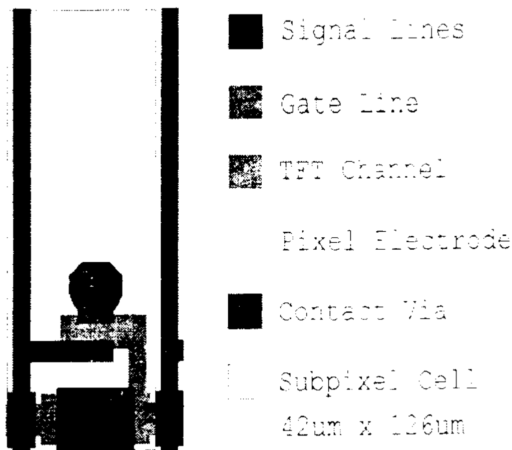

Fig. 1 Unit cell layout of one subpixel showing the layers used in the array.

For ESD devices in the periphery, the interconnection between gate metal and data metal is realized through IZO stitching. The IZO has a typical R_s of 80 Ω/sqr. so multiple vias in parallel were used to provide a low interconnection resistance in some cases. The contact via to the gate metal is critical since it is deeper, going through both the passivation and gate insulator layers.

4. Process Characteristics

Key process issues for high resolution and high image content displays are the lithographic alignment accuracy, the conductivity of the gate and data lines, and control of the TFT channel length. These, and other parameters have been measured for the QSXGA TFT arrays using test sites[8], the results are summarized in Table 1.

Data-Gate X offset	$0.16 \pm 0.12\,\mu m$
Data-Gate Y offset	$0.12 \pm 0.07\,\mu m$
Gate Metal Rs	0.124 ± 0.003 Ω/sqr.
Data Metal Rs	0.082 ± 0.002 Ω/sqr.
Mobility (saturation)	0.83 ± 0.05 $V^2/cm\text{-}s$
$I_{ON}(V_G\ 20V, V_D\ 10V)$	$1.14 \pm 0.25\,\mu A$

Table 1. Process Characteristics (values are averages and standard deviations)

The Data-Gate Y offset is more critical then the X offset because of the orientation of the TFT. As shown in Fig. 2, the data to gate metal overlay error varies systematically with the location on the plate. The variation is shown in the insert by the arrows. The symbols represent the average offset value for 8 plates and the outer lines the standard deviation of the values.

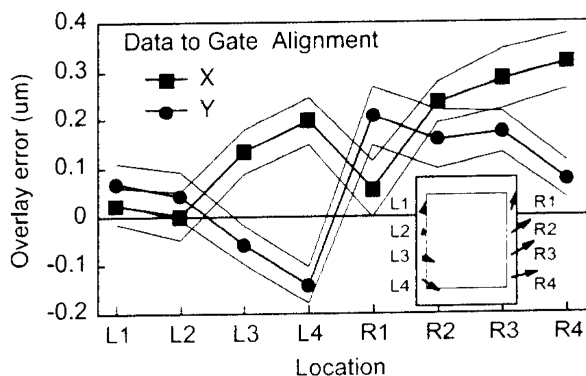

Fig. 2 Systematic variation of data to gate metal overlay error.

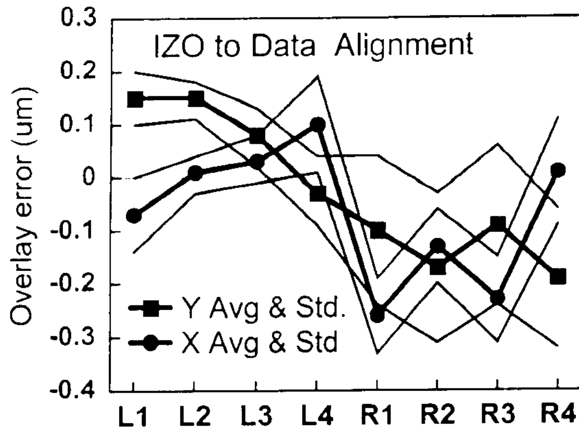

Fig. 3 Systematic variation of IZO-data metal overlay error.

The IZO to data X offset is more critical then the Y offset since the data lines and pixels are orientated along the X axis. It is important to achieve good alignment so that the capacitive coupling from the pixel electrode to the neighboring data lines is equal. As shown in Fig. 3, the IZO to data metal overlay error also varies systematically with the location on the plate. The symbols represent the average offset value for 8 plates and the outer lines the standard deviation of the values.

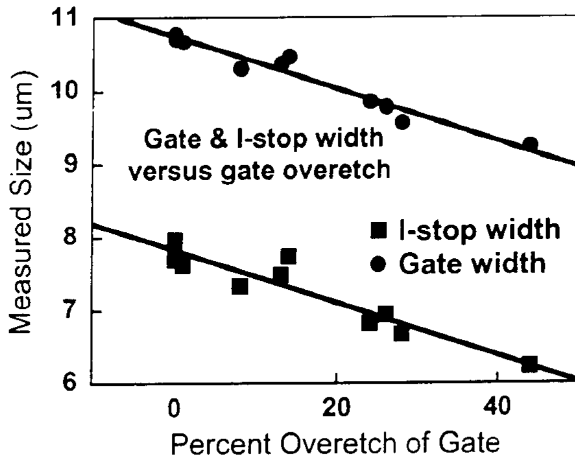

Fig. 4. Variation of the gate and I-stopper width (TFT channel length) with gate overetching.

The control of the channel length of the TFT is very critical for high resolution and high information content displays. With a trilayer type TFT, the I-stopper is defined using a combination of back and front exposure so that the I-stopper is self-aligned to the TFT gate and the TFT channel length is dependent on the size of the gate metal feature. The width (measured optically) of the gate metal under the TFT and the I-stopper (TFT channel length) are plotted versus the percent overetch of the gate metal in Fig. 4.

The on-current and mobility values reported in Table 1 are from 9 x 30 μm test devices and the reported I_{on} value was scaled down to the value expected for the 8 x 10 μm array TFT. The electrical characteristics of a typical test TFT are shown in Fig. 5.

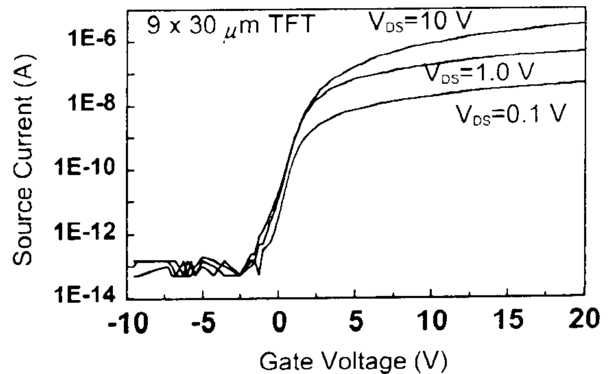

Fig. 5 Typical TFT performance.

5. Summary

It has been demonstrated that even the current highest image content and resolution desktop display, a 16.3" QSXGA with 200ppi color resolution, can be fabricated using the a reduced mask count Al-gate and IZO last process, Fig. 6. The Al(Nd) gate lines show neither hillocks nor whiskers during processing. The amorphous IZO serves not only as the pixel electrode but also as an interconnection layer between gate metal and drain/source metal. This process offers a

substantial reduction in cost due to a smaller number of processing steps.

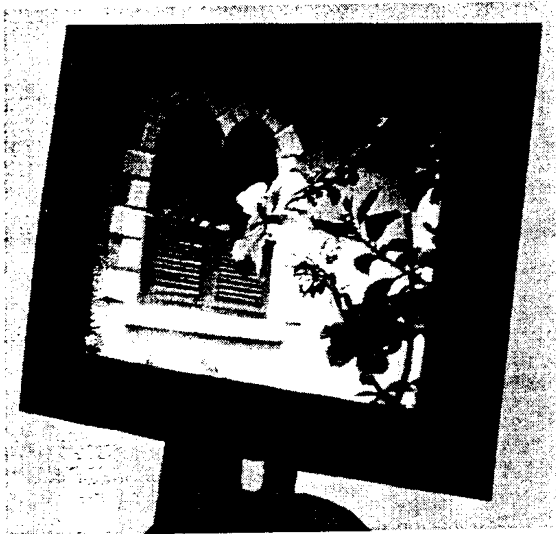

Fig. 6 Photograph of QSXGA Display.

6. Acknowledgments

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