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Direct View Active Matrix VGA OLED-on-Crystalline-Silicon Display

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24.2 Direct View Active Matrix VGA OLED-on-Crystalline-Silicon Display

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Abstract

This paper describes the pixel and array circuitry, which includes a CMOS SRAM cell and a precision current source at each pixel, of a direct view VGA active matrix OLED-on-crystalline-silicon display, developed jointly by IBM Research Division and eMagin Corporation. The display has applications for low-power personal information appliances such as a computer wristwatch. The display obtains data and control signals directly from the memory bus of the appliance's processor.

1. Introduction

High performance computers having ARM and similar processors and dense memory are becoming smaller and lower in cost. They are becoming pervasive, wearable, or part of almost any appliance. A wrist-worn computer watch is one possible application and is a challenging new area of human-computer interface research, since it is available to the wearer at work, at home and almost anywhere in between [1]. User input, computer output to the user, and communications are required with a minimal use of power. The computer's output to the user is primarily its display.

A computer watch display, although small in size, needs to be easily read at night, in room ambient and in direct sunlight for which high brightness and contrast are needed. High resolution displays are needed for ease of reading and to take full advantage of the computing resources. Finally, the display needs to use very little average power, because the size of watch does not leave much room for battery capacity.

A few passive matrix LCDs and active matrix LCDs are available in a size suitable for a wrist watch. Both passive and active matrix technologies require refreshing, which typically uses 2 to 3 milliwatts of power. This is high for the wristwatch application. Passive driven LCDs are also limited in resolution. The highest addressed, suitably sized, display found is 120 by 96. The addressing may be increased by using active matrix. Suitably sized VGA active matrix displays, such as found in projection displays, are available. However, all LCDs require a backlight for night time viewing. A watch LCD backlight dissipates about 60 milliwatts. Momentary illumination reduces average power but would require an action by the user. A backlight may also add undesirable bulk to the watch package.

Small OLED displays may dissipate less power than a backlit LCD. Power for luminance is needed only for the OLEDs that are on. For displaying time, the luminance power can be relatively low compared to a backlight since only 1 to 2 % of pixels may be on. As with passive matrix LCDs, passive matrix OLED displays are limited to about 100 to 200 rows and must be driven at a 60 hertz or higher rates to avoid flicker, requiring 2 to 3 milliwatts of addressing power. Brightness is limited to about 100 to 200 candela/m^2. However, the brightness may not have sufficient contrast for sunlight viewing. Passive matrix driving also requires high instantaneous current densities resulting in lower OLED efficiency.

A high resolution OLED display on a stable backplane that does not require refreshing is ideal for the computer wristwatch application. For this display, IBM Research and eMagin Corporation developed a direct view monochrome OLED VGA active matrix display using a crystalline silicon backplane, and in which the OLED is designed to provide up emission through a common cathode of ITO. To eliminate power for refreshing, a single SRAM cell is incorporated in each pixel. The SRAM array needs only to be written once to retain the display data as long as power is applied.

An IBM 0.35 micron 3.6 V CMOS process is used. Allowing for the OLED cover glass attachment and a cathode connection, the diagonal of the display, limited by the mask field size of the photo lithographic steppers, is 1.08 inch with a pixel pitch of 34.3 microns. The display is not consider to be a microdisplay since its diagonal is greater than one inch, and it is designed for direct view.

While this is not the first OLED-on-crystalline-silicon display to be reported, we believe this to be the first direct view OLED-on-crystalline-silicon display of this pixel density reported [2,3].

2. Pixel Design

The pixel circuit consists of an SRAM for storing the pixel data and a switching precision current source having voltage and current protection circuitry.

Figure 1 shows the SRAM circuitry associated with each pixel. NMOS transistors Q1 and Q2, and inverters I1, I2 and I3 form the SRAM cell. Separate word read and word write inputs are used, allowing the use of a single bit line. The writing power dissipation using a single bit line SRAM is half that of a complimentary bit line SRAM cell. Faster and lower power operation is obtained by designing I2 to be weak, which makes writing data into the I1-I2 latch easier. When reading, I3 isolates the bit line capacitive loading on the output of I1, which

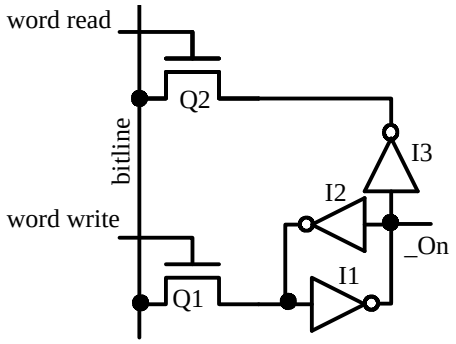

Figure 1 Pixel SRAM circuit

otherwise might disturb the latch data. A similar circuit having a more complicated read and write signal sequences has been previously reported [4].

Figure 2 shows the pixel current source circuit. PMOS Q3 is the current generating transistor and operates with a gate to source voltage that is higher than threshold and a source to drain voltage that is higher than pinch off, allowing operation in the saturation or constant current regime. The channel width, channel length and gate to source voltage is optimized at 150 nA for the available area in the pixel to minimize the influence of threshold voltage variations and channel width variations across the chip on the uniformity of the current. The simulated 3 sigma pixel current source uniformity across the array is less than 1.05:1. This is three times better than previously published [5]. The nominal source to gate voltage of Q3 is ~1.25 V. The channel length (L), 79.12 microns, is much larger than the channel width (W), 2.64 microns. The channel-length-modulation with source to drain voltage is inversely proportional to L. Due to the long channel length, the current varies less than 0.3% as the source to drain voltage of Q3 is varied from 0.75 V to 3.6 V. This is significantly better than is shown for a polysilicon current source [6]. The current source is also very power efficient requiring as little as 0.75 V to give the desired current. Vref, the gate signal for Q3, is common to all other pixels in the display for overall luminance control. Vref is adjusted to give a calibrated maximum luminance, thereby compensating for initial circuit and OLED tolerances.

PMOS Q4 operates as a duty factor or luminance control switch. RB_DF, gate signal for Q4, is also common to all other pixels in the display.

PMOS Q5 functions as the pixel on/off switch. The SRAM output, _On in figure 1, is connected to the gate of Q5.

PMOS Q6 operates as a cascode transistor to extend the current source compliance voltage range from ~3 V to about ~6 V. The well of Q6 is connected to its source assuring that all terminal voltages are < 3.6 V. This arrangement allows the drain to nwell to function as a diode during reverse biasing which is used to remove undesirable forward bias charge build up.

NMOS Q7 assures linear duty factor operation by quickly discharging parasitic capacitors and limits the anode voltage of the OLED to 1 diode drop above ground for OLED reverse biasing.

PMOS Q8, Q9 and Q10 keeps the drain voltage of Q6 from becoming more negative than about -3V, thereby avoiding breakdown voltages across PMOS Q6. A thin film resistor limits current and power dissipated in the event of an anode to cathode short. This protects adjacent good pixels so that they do not fail due to excessive temperature and reduces ground and -5 V distribution voltage drops. Q8, Q9, and Q10 also allow inspection of OLED uniformity at the wafer level by applying -7.5 V between the -5V and ground, using probes.

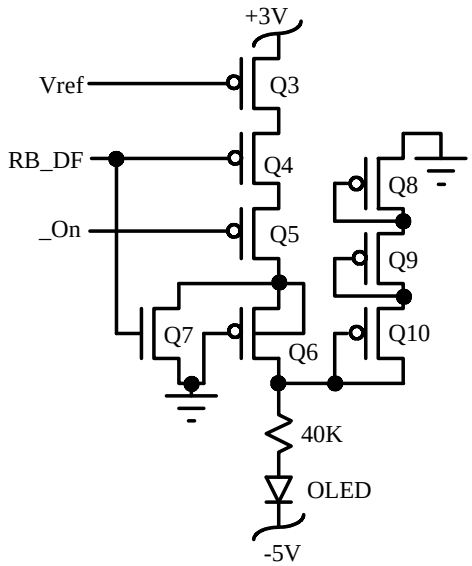

Figure 2 Pixel current source circuit

3. Driver Design

Figure 3 shows a block diagram of the array circuitry. Instead of using raster scan drivers, a memory bus interface is incorporated. At the system level, a display controller is eliminated since it is not required to periodically refresh the display. The processor also uses the memory bus to transmit display control information eliminating additional circuitry.

The memory bus interface consists of 15 address lines, 16 data lines and write enable, chip select and output enable active low control lines (_WE, _CS and _OE). The display SRAM array and display control register are addressed by row and column block decoders. The display is organized as 16-pixel column blocks (words) in the row direction. Word select logic, consisting of two AND gates, is imbedded in each word in the array. The word select logic, consisting of two AND gates, reduces the capacitive load on the word line by locally buffering the capacitive loading of the 16 SRAM inputs. This is called a divided word line structure [7]. Read buffers are used instead of sense amplifiers since reading is only required for testing. Low power high speed reading of the display contents is not useful at the system level.

A 16 bit display control register sets the duty factor for luminance control, selection of an internal or external clock, reverse biasing for the OLEDs, standby, and a clear function. The display control register output signal lines are indented with an '*'. Eight bits are used for setting the duty factor. Since the internal clock, a 11 stage ring oscillator and a 12 stage counter, dissipates ~ 3 milliwatts, an external 32.768 Khz clock, EXTCLK, that is used by the processor, can be selected to eliminate the power dissipation of the internal clock. A clear bit can be set to simultaneously write a low state to all the pixels at once. This can further reduce display writing power when writing a new image since only the new pixel words having "on" pixels need to be written, without writing the previously written on pixels to an off state.

The brightness control circuit includes the internal clock and the circuitry to create a pulse width modulated duty factor signal that is defined by the 8 duty factor bits written into the control register. The average luminance can be varied from 0 to 500 cd/m^2

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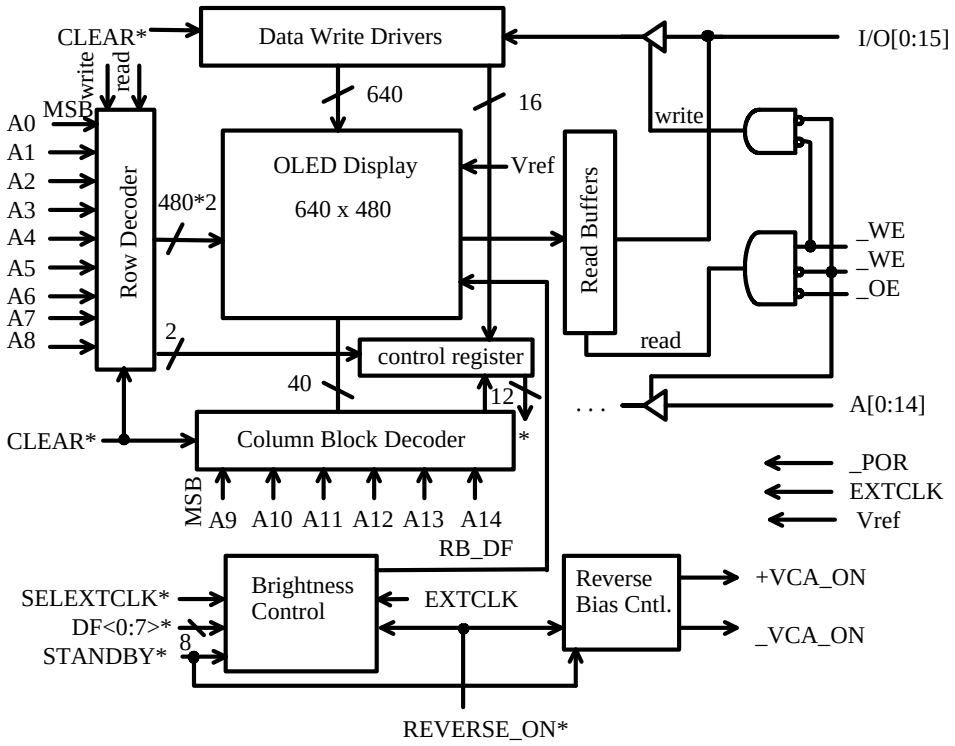

Figure 3 Display block diagram

n 3.9 cd/m^2 increments. The frequency of duty factor signal, RB_DF, is equal to or greater than 60 Hz.

With the REVERSE_ON* bit set high, all the pixel current sources are turned off and NMOS Q7 is turned on with a high state on the RB_DF signal line. The reverse bias control circuit produces the appropriately delayed signals, +VCA_ON and -VCA_ON, for switching the OLED common cathode to a positive power supply.

4. Fabrication

An IBM 0.35 micron 3.6 V rated silicon process is used to fabricate the silicon wafers. The wafers are tested with memory tester and a wafer map is produced.

eMagin Corporation carried out depositing and patterning the anode metal, providing and depositing the organic layers, depositing ITO for the cathode connection, attaching a cover glass and packaging the chip onto a printed circuit board [8].

A yellow colored OLED was chosen for high contrast and relatively high efficiency. eMagin selected the organic materials and optimized them for color and efficiency. Yellow is a high contrast color that is easier to read on a dark background than either blue or green.

5. Results

The electrical and optical measurements were made. At wafer testing, the display write and read operations were verified. In addition, the power supply currents were measured. With the internal clock switched off and all pixels in the off state, the +3 V current was a few microamps, resulting in a steady state power for the SRAM of ~ 10 microwatts. Using a 20 Mhz word addressing rate to write a single pixel checker board pattern down word columns, the worst case power dissipation condition, the measured +3 V current was 10 ma. Put into perspective for the wrist watch, the +3 V average power for writing this worst case pattern and its inverse every other second is ~ 40 microwatts. These measurements demonstrate the low power characteristics of the design.

The OLED current in the assembled display with Vref adjusted for 500 cd/m^2, the maximum desired luminance, was ~135 nanoamps which is close to the 150 nanoamp design target. PMOS Q3 source to gate voltage is 1.14 V. The luminance varies 0.3% with the -5 V power being changed by +0.5 V and -0.5 V indicating good constant current source operation. A nine spot luminance measurement shows that viewing area nonuniformity to be less than 3%.

The contrast is dependent upon the ambient illumination. The contrast of the display in sunlight was better than 4:1 which is sufficient for viewing. A circular polarizer or other contrast enhancement features are not required. The off state brightness in a laboratory illumination environment, having a white paper luminance of 150 cd/m^2, is about 8 cd/m^2. In this environment, the contrast is greater than 60 with OLED luminance at maximum.

Viewing area diagonal	1.08 inch
Format	VGA (640 x 480)
Pixel pitch	34.3 microns
Resolution	741 dots per inch
Structure	1 SRAM cell per pixel with a memory bus interface
OLED forward voltage	~6.75 V
OLED color	yellow; CIE(x=0.473, y=0.508)
OLED efficiency	~2 lumens/watt
Aperture ratio	90%
Luminance range	0 to 500 cd/m^2 in 4 cd/m^2 increments

Table 1 Summary of the OLED display characteristics

Photo 1 shows a scale size image of the display showing the time and icons in a computer wrist watch. The watch contains an ARM7 processor, 8 megabytes of dynamic random access memory and 8 megabytes of flash memory. A Linux operating system with X11 R6 graphics is incorporated [9]. A touch screen and a jog wheel are used for interaction. Also, included are a serial port and an IrDA port for communications.

For photo 2 shows a calendar, illustrating the ease with which the display can be read. Even though the display has only one bit per pixel, good gray scale images are obtained using spatial dithering.

Photo 1 OLED display in a computer wrist watch

6. Conclusion

A direct view active matrix OLED on crystalline silicon VGA display has been developed for low power personal information appliances. Low power operation using a SRAM to store data at each pixel has been demonstrated. Since the display is easily read in any ambient condition, the design objectives have been achieved.

Photo 2 Close up of OLED display

7. Acknowledgments

We are indebted to the management and technical staff at eMagin for the great working relationship and the excellent results. We would like to acknowledge the management and technical staff at Micrus for wafer fabrication and testing. We also would like to thank our management and coworkers at IBM.

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