RC 22031 (98910) 11 April 2001 **Electrical Engineering**

IBM Research Report

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The effect of thermal processing on strain relaxation and interdiffusion in Si/SiGe heterostructures studied using Raman spectroscopy

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ABSTRACT

The effect of thermal annealing on Si/SiGe heterostructures is studied using Raman spectroscopy. The structures consisted of Si on relaxed $Si_{0.8}Ge_{0.2}$ where the top Si thickness was 20-30 nm. MicroRaman spectroscopy with 488 nm incident radiation revealed no significant shift in the strained Si peak position with thermal annealing at temperatures up to 1100°C for 30 seconds. However, the intensity of the Si peak was systematically reduced with increasing thermal processing, a result which is attributed interdiffusion at the Si/SiGe interface resulting in an apparent thinning of the Si cap layer.

Si/SiGe strained-layer heterostructures are of potential value for future scaled CMOS technology.[1,2] In particular, relaxed SiGe layers capped with a thin (10-30nm) strained Si channel are particularly promising since both n- and p-MOSFET performance enhancement can be achieved.[3-6] However, it is not clear whether or not these layers can withstand the thermal processing necessary for high-performance scaled CMOS technology. For instance, a typical CMOS process involves processing temperatures on the order of 1000 °C, and these high temperatures can lead to relaxation of the strained Si layer. The reduced strain can decrease the potential performance benefit of the strained layer structure, and the formation of strain-relieving defects can lead to yield and reliability problems. Despite these potential difficulties, only a few studies on the effect of annealing in Si/SiGe bilayer structures have been reported. One such study was performed by Samavedam *et al.*[7] who concluded that the strained Si layer relaxes mostly elastically as a result of thermal processing, but that a small number of misfit dislocations can form even in very thin strained Si layers. However, that study did not account for any interdiffusion occurring as a result of thermal processing. Sugii[8] showed that interdiffusion occurs at the Si/SiGe interface but could not quantiatively asses the degree of strain relaxation and interdiffusion using Raman alone. In this paper, we study the effect of thermal annealing on both strain and interdiffusion in Si/SiGe bilayer structures using Raman spectroscopy. We find that, surprisingly, even in Si on SiGe layers with thickness well past the thermodynamically stable critical thickness,[9] that interdiffusion at the Si/SiGe interface occurs before the onset of significant strain relaxation, and it is the former process that appears to limit the practical thermal processing that these layers can withstand.

The basic layer structure used in the present work is shown in Fig. 1. The entire structure was grown by UHV-CVD on a p-type doped Si wafer, and consisted of a 500 nm step-graded $Si_{1-x}Ge_x$ buffer layer, a 400 nm constant-composition $Si_{0.8}Ge_{0.2}$ layer, a 50 nm $Si_{0.75}Ge_{0.25}$ layer, a 350 nm $Si_{0.8}Ge_{0.2}$ layer, and finally a strained Si capping layer. Two structures were grown with different strained Si cap layer thicknesses of 20 nm and 30 nm. X-ray diffraction analysis of the as-grown layer structure revealed an actual Ge concentration of 21% for the nominally $Si_{0.8}Ge_{0.2}$

layers, with 12% residual strain for both samples. Here, the residual strain is defined as the ratio of the strain in the layer to that of a fully strained (pseudomorphic) layer grown on Si with the same Ge concentration. The Raman spectrum from the as-grown layer structure with the 30 nm Si cap is shown in Fig. 2. The wavelength of the incident radiation was 488 nm. The curve shown in Fig. 2 was fit using a double Lorentzian line shape in order to the determine the peak position and intensity of the Raman scattered light arising from the Si-Si vibrational modes in the SiGe buffer layer and the strained Si cap layer. The "apparent" Ge concentration of the SiGe buffer layer, P_{SiGe}, can be determined from the difference between the position of the SiGe peak and the position of a reference bulk Si peak. We also introduce a term called the "net strain," *NS*, which is proportional to the difference between the strained Si and bulk Si peak positions divided by P_{SiGe}. The respective formulas[10] are as follows:

$$P_{SiGe} = 1.50\,(k_{Si} - k_{SiGe}), \quad (1)$$

$$NS = 3.31\,(k_{Si} - k_{SS}) / P_{SiGe} \quad (2)$$

where k_{Si}, k_{SiGe} and k_{SS} are the wavenumber positions of the Si-Si vibrational mode arising from the bulk Si reference sample, the SiGe buffer layer and the strained Si layer, respectively.

Fig. 3(a) shows the Raman spectra of the sample with the 20 nm Si cap with no anneal, and after RTAs of 1000 °C for 5 sec, 30 sec, and 5 min in a nitrogen ambient. The curves are offset along the *y*-axis for clarity. In each case, the experimental data was fit using the procedure described previously, and the results were normalized such that the integrated area of the double Lorentzian fit was constant. The figure shows several trends. First of all, the position of the SiGe peak shifts slightly to the left with increasing anneal time. X-ray diffraction of the annealed samples revealed that this is due to relaxation of some residual strain in the thick SiGe buffer layer. Secondly, the intensity of the strained Si peak decreases with increasing annealing time. In order to ascertain more clearly the effect of the annealing on the strained Si layer, we have plotted the Si peak separately in Fig. 3(b). The figure clearly shows a decrease in the strained Si peak intensity, but shows no evidence of a rightward shift in the Si peak position. In

fact, the peak shifts slightly to the left, indicating that annealing slightly *increases* the strain in the Si layer, once again, a likely result of the increased relaxation in the SiGe layer.

In order to better quantify the results in Fig. 3, *NS* was determined for various annealing conditions and plotted in Figs. 4(a) and (b). Results were obtained for both strained Si cap thicknesses of 20 nm and 30 nm. In Fig. 4(a), *NS* is plotted vs anneal time for constant temperature, and in Fig. 4(b), *NS* is plotted vs temperature for constant anneal time. A decrease in NS with increased annealing time or temperature would indicate the relaxation of strain in the Si surface layer. However, the plots show no such trend, and withing experiemntal error, the annealing has no definitive effect on the strain state of the Si layer. Figs. 4(c) and (d) show plots of A_{ss} after annealing under the same conditions. Here, A_{ss} is the ratio of the strained Si peak area to the total area of the double Lorentzian fit, and to first order, is proportional to the thickness of the strained Si layer. These plots clearly show that the strained Si peak area, and therefore layer thickness, decreases with increasing anneal time and temperature. Furthermore, the *slopes* of the plots for 20 nm and 30 nm Si layers are approximately equal. This result strongly suggests that the strained Si layer is thinned by a similar amount in both samples, which suggests that the thinning is due to interdiffusion at the Si/SiGe interface. The degree of thinning of the Si cap layer is consistent with experimentally determined diffusion coefficients reported by Griglione *et al.*[11] for SiGe layers grown on Si. For instance, in ref. 11, the diffusion length of Ge in Si for a 1000 °C / 5 min anneal was determined to be 5.2 nm, while our data shows a thinning of the 20 nm (30 nm) Si cap by 6.6 nm (6.3 nm) for the same conditions.

In conclusion, the effect of thermal annealing on strained Si on SiGe heterostructures has been studied using Raman spectroscopy. Annealing at 1000 °C for as long as 5 minutes caused no significant relaxation of the strained Si layer, but did reduced the intensity of the Si peak. We attribute the latter result to interdiffusion at the Si/SiGe interface, which effectively thins the Si cap layer. This interpretation is supported quantitatively by previous studies of Ge outdiffusion from SiGe strained layers on Si. This work suggests that Si/SiGe interdiffusion, not strain relxation, sets the upper limit on the practical thermal budget that these layers can withstand.

The authors would like to acknowledge Dr. Andre' J. Sommer at the Miami University Microspectroscopy lab for performing the Raman measurements, and Jean-Jordan Sweet for performing the X-ray diffraction measurements.

References

[1] K. Rim, J. L. Hoyt and J. F. Gibbons, *IEEE Trans. Elect. Dev.* **47**, 1406 (2000).

[2] T. Mizuno, S. Takagi, N. Sugiyama, H. Satake, A. Kurobe, A. Toriumi, *IEEE Elect. Dev. Lett.* **21**, 230 (2000).

[3] J. Welser, J. L. Hoyt, S. Takagi, and J. F. Gibbons, *IEDM Tech. Digest*, 947 (1994).

[4] K. Rim, J. L. Hoyt, and J. F. Gibbons, *IEDM Tech. Digest*, 707 (1998).

[5] K. Rim, J. Welser, J. L. Hoyt, and J. F. Gibbons, *IEDM Tech. Digest*, 1026 (1995).

[6] D. K. Nayak, K. Goto, A. Yutani, J. Murota, and Y. Shiraki, *IEEE Trans. Elect. Dev.* **43**, 1709 (1996).

[7] S. B. Samavedam, W. J. Taylor, J. M. Grant, J. A. Smith, P. J. Tobin, A. Dip, A. M. Phillips, and R. Liu, *J. Vac. Sci. Technol.* **B 17**, 1424 (1999).

[8] N. Sugii, Proc. of New Group IV (Si-Ge-C) Semiconductors Workshop, Sendai, Japan, Jan. 21-23, 2001.

[9] J. W. Matthews and A. E. Blakeslee, *J. Cryst. Growth* **32**, 265 (1976).

[10] B. Eietrich, E. Bugiel, H. J. Osten, and P. Azumseil, *J. Appl. Phys.* **74**, 7223 (1993).

[11] M. Griglione, T. J. Anderson, Y. M. Haddara, M. E. Law, K. S. Jones, A. van den Bogaard, *J. Appl. Phys.* **88**, 1366 (2000).

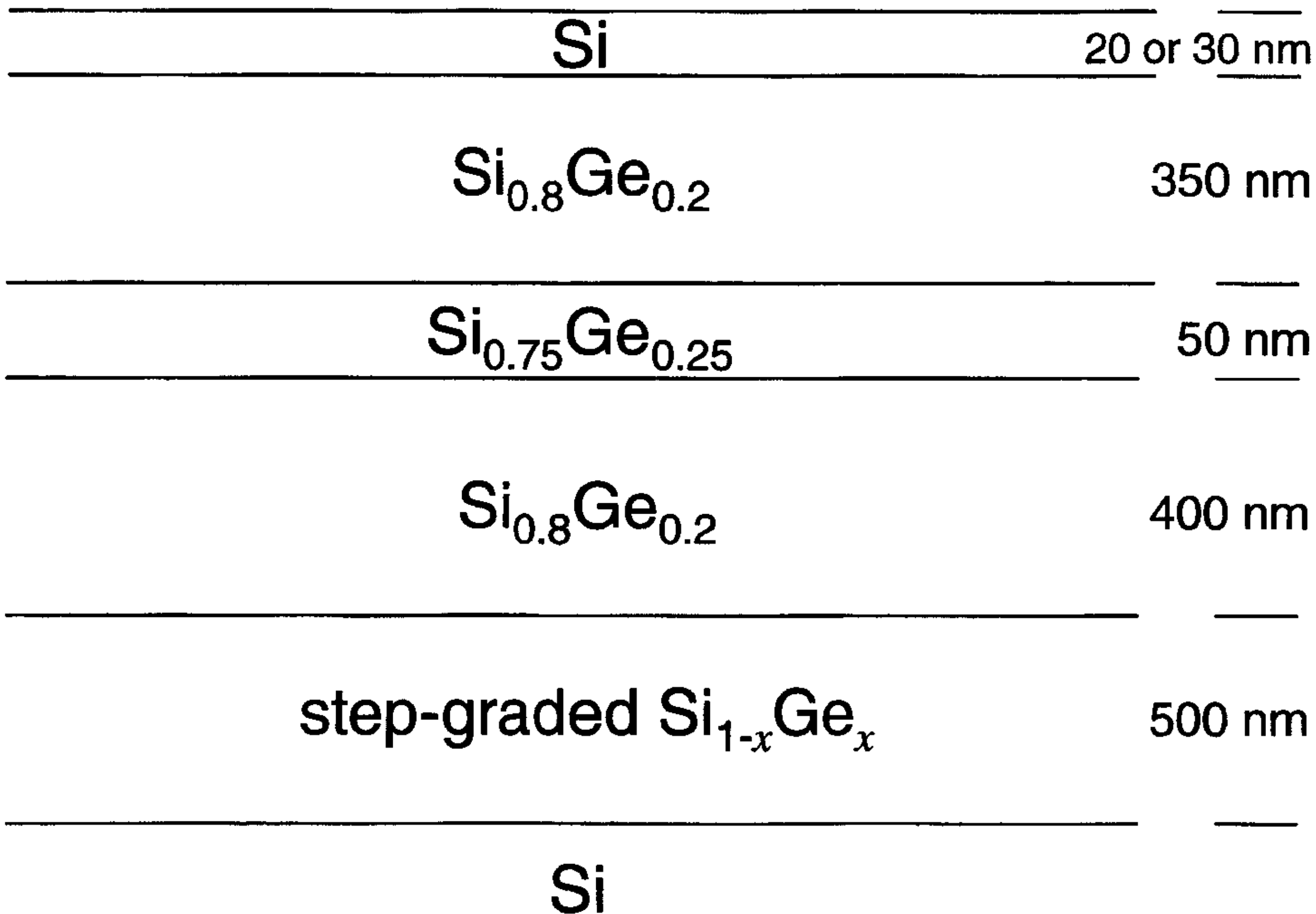

Fig. 1. Cross-sectional diagram of the Si/SiGe layer structure.

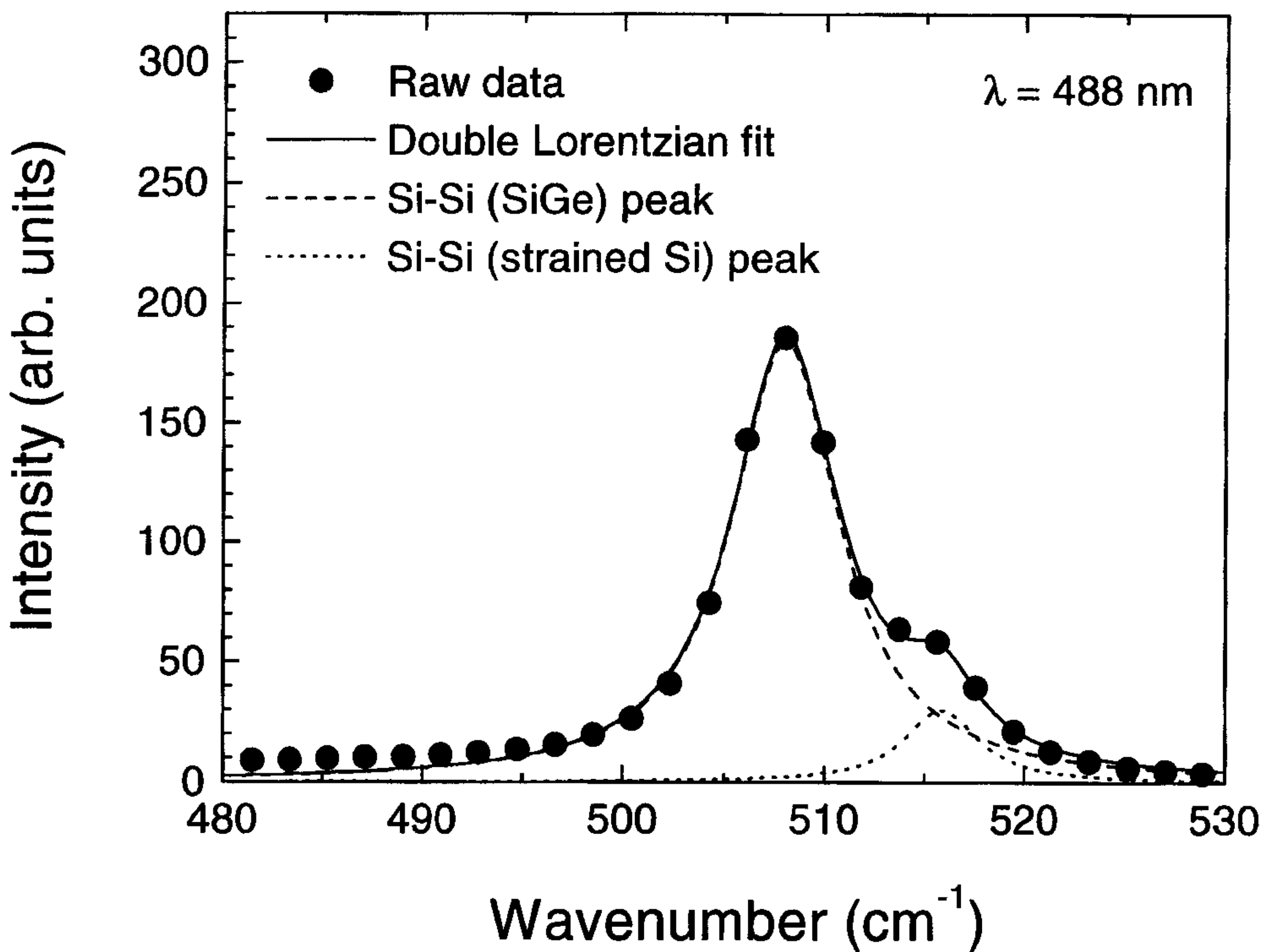

Fig. 2. Raman spectra from the as grown Si/SiGe layer structure with 30 nm Si capping layer. The solid line is the double Lorentzian fit, indicating excellent fit with the measured data. The plot also shows the separate Lorentzian lineshapes associated with the SiGe buffer layer and the Si cap layer.

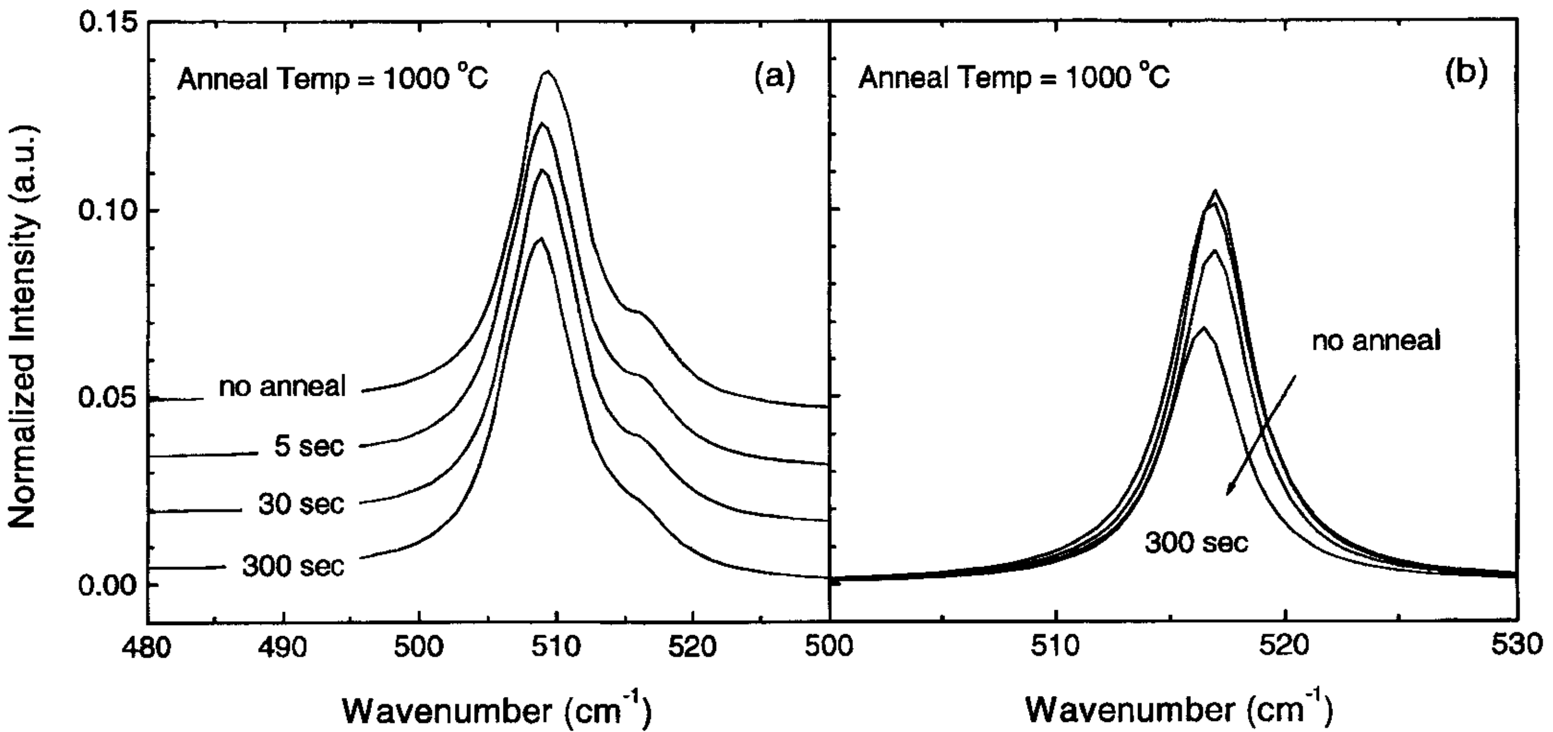

Fig. 3. (a) Intensity vs Raman shift for Si/SiGe layers with 20 nm Si capping layer, for no anneal, and for anneals at 1000 °C, 5 sec, 30 sec, and 5 min. The plots are offset in the *y*-axis for clarity. (b) Plot of the strained Si peak extracted from the raw data for the same annealing conditions as in (a).

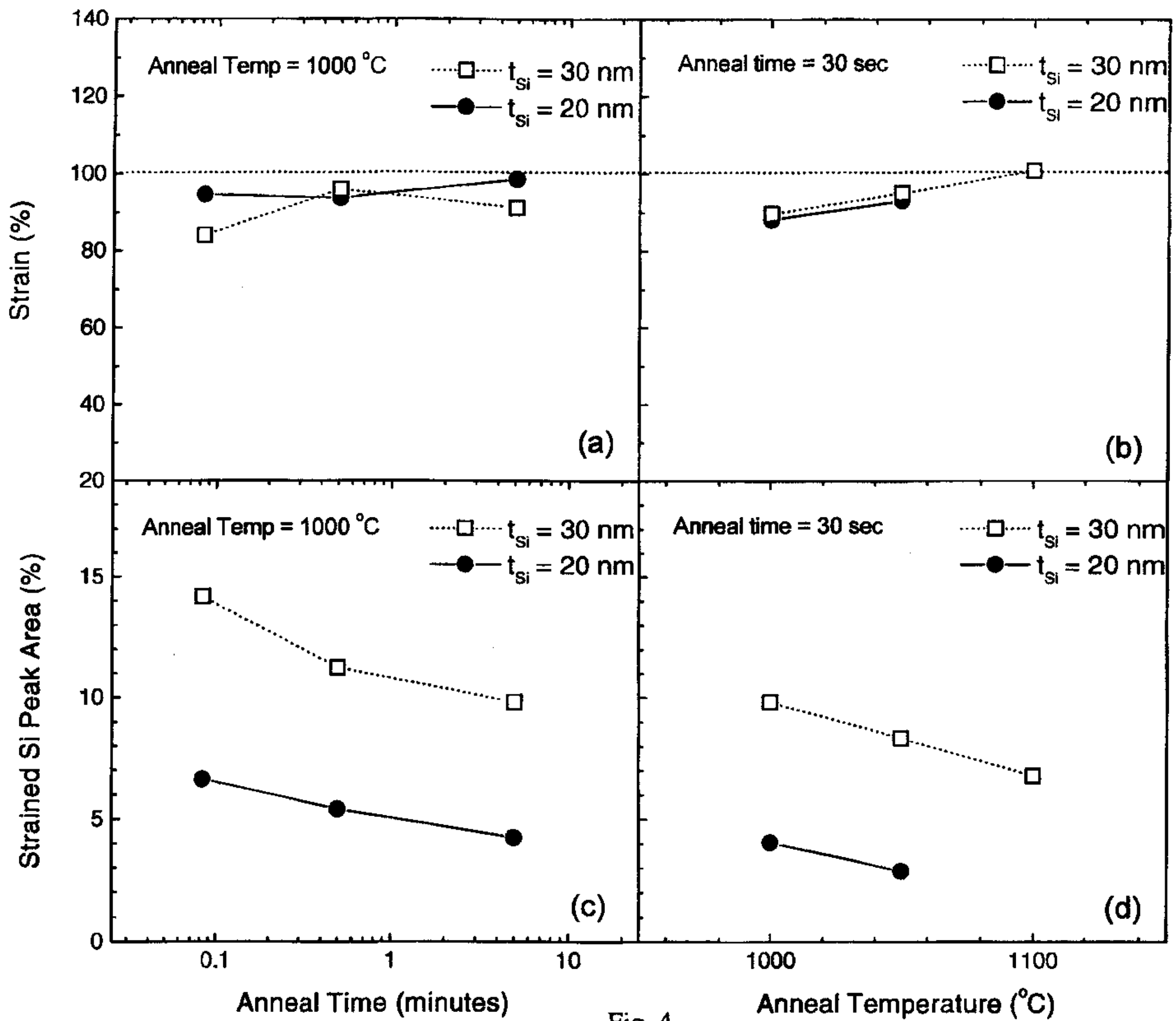

Fig. 4.

(a) Net strain in strained Si layer plotted vs. annealing time for constant temperature.

(b) Net strain in strained Si layer plotted vs. annealing temperature for constant time.

(c) Normalized strained Si peak area plotted vs. annealing time for constant temperature.

(d) Normalized strained Si peak area plotted vs annealing temperature for constant time.