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Research Report

Investigations of UHV/CVD Deposition of SiGe Alloys on Silicon-on-Sapphire Substrates for Application to Device Fabrication Technology

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Investigations of UHV/CVD Deposition of SiGe Alloys on Silicon-on-Sapphire

Substrates for Application to Device Fabrication Technology

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Circuit Fabrication

During this quarter, work continued on processing frequency-divider circuits on the GOV31 wafer, which is a pMODFET heterostructure grown on bulk Si. The device and circuit fabrication has progressed to the point of the M1 level, which is the fifth of seven total lithography levels in the fabrication process. Excellent T-gate yield was achieved on this run; however, subsequent processing seems to have degraded the process yield, with many of the T-gates detaching from the surface or breaking apart. Difficulties in obtaining acceptable Ohmic contact and M1 lithographic exposures contributed to the degradation of the T-gates. Due to the degradation of the T-gates, it is unlikely than any operational divider circuits will result from this fabrication run. Nevertheless, the M1 level was patterned and deposited on this wafer, despite significant misalignment, so that the discrete devices could be characterized.

Both dc and ac measurements were performed on nominally 0.1 μm gate-length devices after lift off of the M1 metallization. Fig. 1(a) shows the dc output characteristic from the best device, while Fig. 1(b) shows the dc transconductance plots from several nominally identical devices, indicating that significant variations in the device properties exist. Furthermore, many discrete devices were either dead shorts or showed no modulation. The best device had a maximum transconductance of 275 mS/mm, and a maximum dc gain >10. These values, along with the threshold voltages and overall current levels are consistent with those from previous runs, indicating that the devices are similar to those used in the circuit design models. The devices do however have somewhat higher gate leakage current than our previous runs, which is probably due to deterioration of the gate electrode as a result of over processing.

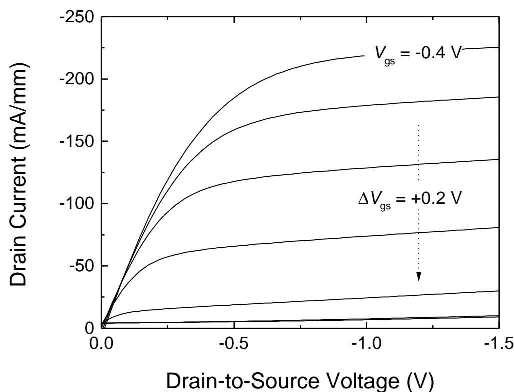

Fig. 1(a). Output characteristic for a 0.1 μm gate-length pMODFET.

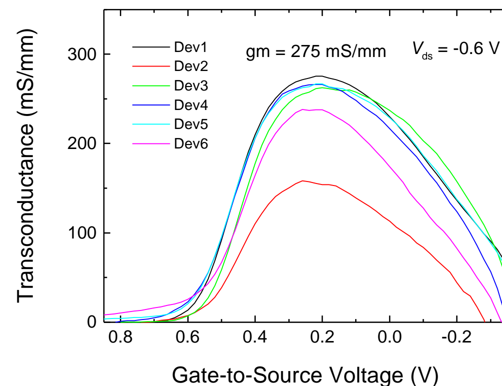

Fig. 1(b). Transconductance vs gate voltage plots for nominally identical 0.1 μm gate-length pMODFETs.

High-frequency *s*-parameter measurements were also performed on these devices, and the results are shown in Fig. 2. Maximum f_T and f_{max} values of 34 GHz and 68 GHz were obtained, values which fall well short of the 50 GHz and 116 GHz obtained on previous device runs. It is unclear at this point why the new devices show such degraded performance. However, it should be pointed out that our previous results were from devices on sapphire wafers, while these devices utilize bulk Si substrates. In addition, a slightly longer gate-length device was used for this run, in order to insure good T-gate lift-off yield for the divider circuits.

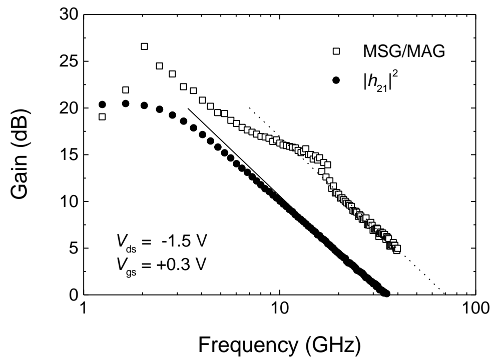

Fig. 2(a). Gain vs. frequency plot for a 0.1 x 50 μm^2 gate-length pMODFET.

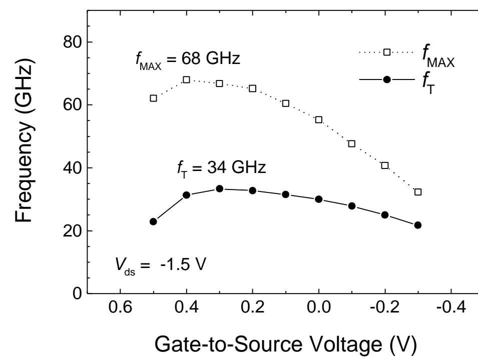

Fig. 2(b). f_T and f_{max} plotted vs gate voltage for same pMODFET as in Fig. 2(a).

The near-term strategy for fabrication of the pMODFET circuits is to start a new fabrication run from the beginning, using modified process conditions to improve device yield and performance. Such changes will include using a wafer stepper instead of contact aligner for all optical lithography steps and processing full 4" wafers instead of pieces. The current run will be continued through the final two lithography steps to act as a "send-ahead" run for the process development. Further characterization of the discrete devices will then be performed after completion of the run.

SiGe wafers for Wafer Bonding Experiments

4” wafers with relaxed SiGe (x=0.3) buffer layers were grown by UHV/CVD. The run (Gov44) included three SOI substrates as required for experiments at the University of Wisconsin (UW) on wafer bonding of SiGe to sapphire. In order for these wafers to be suitable for wafer bonding, the cross hatch surface roughness which accompanies strain relaxation by dislocation multiplication must be removed by chemical-mechanical polishing (CMP) and subsequently brush cleaned to remove the polishing materials. IBM’s tooling for CMP and brush cleaning is for 8” wafers. A 4” wafer holder was purchased for the CMP tool for this project, but the polishing paramteres required are at the edge of the ranges available with this tool. A special polymer adapter is used to hold the 4” wafers for brush cleaning in the tool designed for cleaning 8” wafers. Since the 4” wafer sits in this special wafer holder, the back side of the wafer is not cleaned. Instead, the holder is cleaned without the 4” wafer and then with the 4” wafer

and this sequence is repeated 3 times. This cleaning procedure has worked well in the past, giving typical values for the RMS roughness of less <0.5 nm, as measured by atomic force microscopy (AFM) with no debris left on the wafer surface (see previous quarterly reports). This time, however, AFM measurements after polishing and cleaning showed that some wafers had residual debris as shown in Fig. 3. Unfortunately these particles are too small to be observed by optical inspection of the wafer while it is still wet. A repeat brush cleaning did not remove this debris. Wafers with debris were therefore re-polished and the debris was removed. As shown in Fig. 4, the debris left fine scratches on the wafer surface during the second polish. These scratches are not expected to be a problem for the wafer bonding experiments since the RMS surface roughness is 0.18 nm. Three polished wafers (SOI substrates) were sent to Prof. Tom Kuech at UW for his experiments; two had a single CMP polish but one had to be polished a second time.

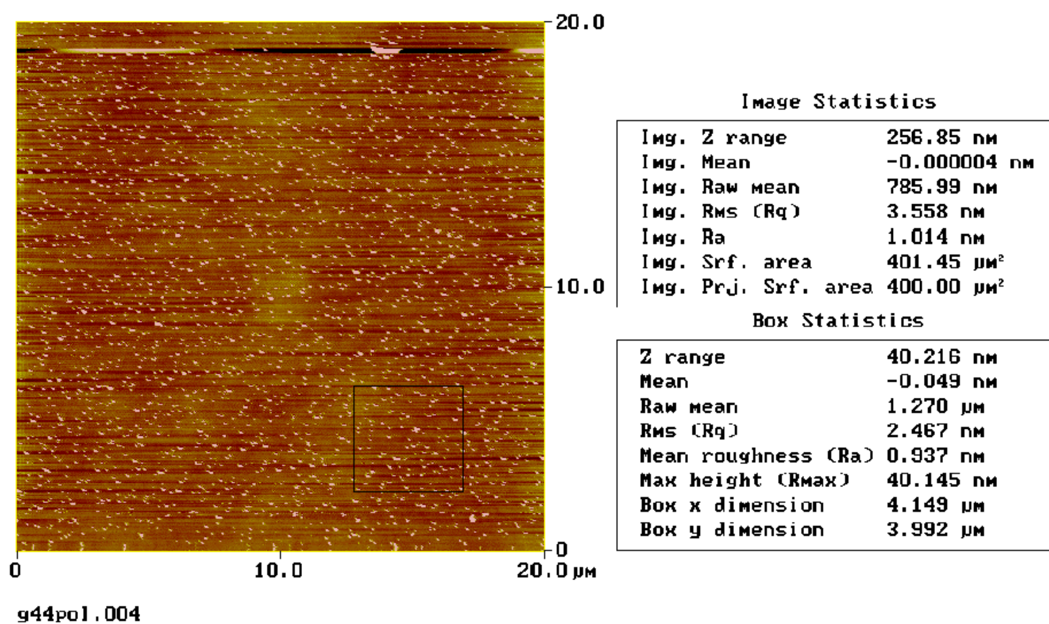

Fig. 3 AFM image of a Gov44 wafer showing debris left after CMP polishing and brush cleaning.

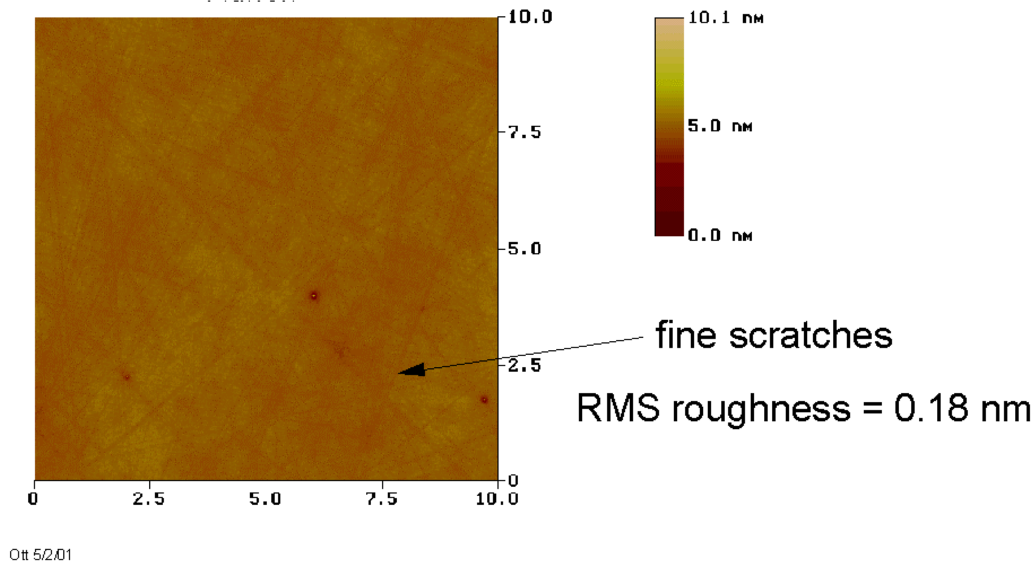

Fig. 4. AFM image of a Gov44 wafer after re-polishing and cleaning. The fine scratches are not expected to interfere with wafer bonding.

UHV/CVD growth of pMODFET Device Structures

Due to technical problems with our 5” UHV/CVD reactor, growth of a p-MODFET device structure on the 4” bonded SOS wafer received from UW has been delayed. The reactor has been repaired and SiGe calibration structures have been grown and are being evaluated. Once a test structure with mobility within the range of acceptable values has been grown, the same structure will be grown on the bonded SOS substrate. We anticipate that this will be done during the next quarter.

Publications

“SiGe pMODFETs on Silicon-Sapphire Substrates with 116 GHz f_{max}”, S.J. Koester, R. Hammond, J.O. Chu, P.M. Mooney, J.A. Ott, L. Perraud and K.A. Jenkins, IEEE Elect. Dev. Lett. 22, 92 (2001).