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ULTRATHIN HIGH-K DIELECTRICS GROWN BY ATOMIC LAYER DEPOSITION: A COMPARATIVE STUDY OF ZrO_2, HfO_2, Y_2O_3 AND Al_2O_3

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We summarize our recent work on atomic layer deposition (ALD) of metal oxides for advanced gate dielectrics applications. We present data on ultrathin (<10 nm) ZrO_2, HfO_2, Y_2O_3 and Al_2O_3 deposited on silicon. Both physical and electrical properties, as well as the effects of pre- and post-deposition treatments will be discussed.

INTRODUCTION

As the thickness of conventional SiO_2-based gate dielectrics in MOS devices shrinks below ~2 nm, large leakage current and reliability concerns dictate the search for new dielectric materials for the gate stack with permittivity (dielectric constant) higher than that of SiO_2, that are often referred to as "high-K" gate dielectrics.[1-3] Recent research on high-K dielectrics was focused mostly on binary metal oxides, such as Ta_2O_5, TiO_2, ZrO_2, HfO_2, Y_2O_3, La_2O_3, Al_2O_3, etc., and their silicates. In most of the reports published so far (with few exceptions), high-K dielectric layers were deposited on silicon by sputtering.[3] However chemical vapor deposition techniques are more attractive from a device manufacturing viewpoint.

In this paper, we demonstrate the use of ALD for ultrathin high-K gate dielectrics. This technique [4-7] offers excellent uniformity across 200 mm (and larger) wafers, process control, step coverage/conformality, and low thermal budget. We present a comparative analysis of physical and electrical properties of ZrO_2, HfO_2, Y_2O_3 and Al_2O_3. These materials are predicted to be thermodynamically stable on Si [8] and have reasonably high band gap (barrier height) [9] that make them promising high-K candidates for logic and memory applications. We found all four materials exhibited gate leakage much lower than that of conventional SiO_2 of the same equivalent electrical thickness (capacitance) and good interface quality (after post-deposition anneals). We further discuss some integration issues, in particular thermal stability.

EXPERIMENTAL

ALD is deposition technique based on *sequential* saturating surface reactions. [4-7] Typically, the process is performed by sequential pulsing of precursor A and B, Me-containing

molecules and oxidizer (such as H_2O, O_2, O_3, N_2O, etc. in our particular case). Surface saturation after each pulse (A or B) is important for reaction completeness and hence a monolayer-by-monolayer growth mode. This is achieved by setting the length of the pulse corresponding to the saturation of the surface by precursor molecules (Fig.1) typically on the order of 0.1 – few seconds. The surface saturation mechanism is an important feature of ALD. In particular, it enables excellent uniformity over large areas and good conformality on non-planar structures, such as deep trenches. Reactive precursors forming a chemical bond (chemisorption) with the surface at low deposition temperatures are ideal for ALD. ALD is a low thermal budget process with deposition temperatures in the 200-500^oC range. Deposition temperature should be lower than decomposition temperature of the precursors. In contrast to conventional CVD, the process is relatively insensitive to the temperature (within the ALD process window) implying that temperature uniformity in the ALD reactor is not a major design factor. To avoid gas phase (bulk CVD-type) reactions and consequently detrimental effects of particle formation and film non-uniformity, the pulses of precursors A and B are separated by a longer purge pulse of an inert gas. Film thickness in ALD is controlled by number of pulses, as show in Fig. 2 (summarized for different materials and reactions). For a "classical" ALD reaction [6, 10], Al_2O_3 deposition from TMA ($Al(CH_3)_3$) and water, deposition rate is ~ 0.1 nm/cycle.(Fig.3) Since ALD utilizes the concept of surface termination, initial condition of the surface (surface termination) is an important factor. As an example, Fig. 3 shows Al_2O_3 deposition on Si wafers prepared in four different ways: (i) H-terminated surface after an HF-last process; (ii) ultrathin silicon nitride; (iii) ultrathin silicon oxide; (iv) and ultrathin silicon oxynitride. One can see there is an incubation time of approximately 5 pulses (i.e. ~ 5 sec.) in the case of hydrogen terminated surface. This result confirms a known fact that OH or NH_2 surface terminations provide good reaction sites for subsequent ALD depositions. More technical details about ALD processes and applications can be found elsewhere. [4-7]

The films studied in this work were deposited using the following chemistries $ZrCl_4$ + H_2O; $HfCl_4$ + H_2O; $Y(thd)_3$ + O_3; and $Al(CH_3)_3$ + H_2O respectively. Physical thickness of the high-K layer was in the 1.5 – 10 nm range. The films were deposited on bare silicon (after HF last chemical pre-clean) or ultrathin thermally grown interlayer. In some cases, the low temperature (300-400^oC) ALD deposition step was followed by oxygen, nitrogen and/or forming gas anneals.

Capacitor structures were then fabricated on both n- and p-type Si wafers with Al gate electrode for electrical measurements. Capacitance-voltage (C-V) measurements were used to obtain equivalent electrical thickness of the high-K gate stack, flatband voltage, interface quality(interface defects) and hysterisis. Electrical thickness (Tqm) was calculated from capacitance in the accumulation using quantum-mechanical corrections as discussed in Refs. [1, 11, 12] Current-voltage (I-V) characteristics were taken to understand leakage current properties of the insulators studied. Electrical measurements were complimented by physical analysis with the help of cross-sectional electron microscopy (HRTEM), medium energy (100-200 keV) ion scattering (MEIS), photoemission spectroscopy (XPS), atomic force microscopy (AFM), nuclear reaction analysis (NRA), ellipsometry and other analytical tools.

RESULTS AND DISCUSSION

a) ZrO_2 and HfO_2 results

High-frequency CV characteristics of ZrO_2 films of different thickness on both n- and p-type substrates are shown on Fig. 4. Good interface quality can be seen. By plotting electrical (quantum-mechanical) thickness versus physical thickness (Fig. 5), the dielectric thickness of ~ 20-24 was obtained (the two dotted lines show the $20<k<24$ margins). The intercept with the Y-axis of the plot shows the electrical thickness of the interfacial oxide. The thickness varies from close to zero to as much as 1.5 nm depending on processing conditions. Most thickness increase comes from SiO_x growth at the interface after oxygen anneals. From CVs (Fig.4), a flatband shift of ~ 400-500 meV (with respect to the ideal Al gated MOS case) is observed that is summarized on Fig. 6. One can see the magnitude of the shift depends on the thickness of the bottom interlayer as well as on postdeposition anneal conditions. Leakage current of ZrO_2/SiO_2 gate stacks is found to be low, ~ 4 – 5 orders of magnitude lower than SiO_2 of equivalent electrical thickness (Fig. 7). However, films deposited on hydrogen terminated Si (after HF-last preclean) exhibit poor gate leakage characteristics. We attribute this to the nucleation problem observed in our recent MEIS and HRTEM experiments.[7, 13] More details on the physical analysis of the stoichiometric ZrO_2 ALD films can be found elsewhere.[7, 13]

HfO_2 films behave quite similar to ZrO_2 due to the similarities in the ALD chemistries and materials properties. We found that good quality HfO_2 gate stacks could be fabricated with significantly reduced leakage current. In analogy to ZrO_2, poor nucleation of HfO_2 on hydrogen terminated surface was observed by MEIS, HRTEM and also supported by electrical measurements. We discuss more results on HfO_2 in a forthcoming paper.[14] In both the HfO_2 and ZrO_2 cases we found uniform continuous ultrathin high-K layers can be deposited on thin SiO_2 oxide.

b) Y_2O_3 results

Due to a different ALD chemistry used for Y_2O_3 depositions, specifically the high reactivity of the ozone oxidizer and carbon-containing metal precursor, we found the films to be oxygen-rich (Fig. 9) with some (up to ~ 6%) residual carbon. Comparing MEIS spectra in the oxygen region (the lower energy peak) for deposited yttrium oxide and stoichiometric ZrO_2, one can see excess oxygen in the case of the yttrium oxide. No significant difference in depositions on HF-last treated Si surface and SiO_2 interlayers was observed. In fact, in both cases ~ 1.1- 1.4 nm of interfacial oxide was deduced from HRTEM (Fig. 8) MEIS (Fig. 9), and XPS (Fig. 10) experiments. Si2p core-level spectra for Y_2O_3 films deposited on HF-last; thin SiO_2 and annealed at 600^{o}C in oxygen are shown in Fig. 10. The two peaks correspond to elemential Si (in the Si substrate) and SiO_2 (the higher binding energy peak). The presence of SiO_2 in the case of Y_2O_3 deposited on HF last is clearly seen. One should also point out the increase of the intensity of the SiO_2 peak after oxygen anneal. This is indicative of SiO_2 growth at the interface due to oxygen diffusion through the high-K layer and reaction with Si at the interface. The HRTEM cross-section (Fig. 8) suggests that as-deposited Y_2O_3 film is microcrystalline. Electrically the

films show low leakage (Fig. 11). When compared to SiO_2 (solid bench line on the Fig), gate leakage is reduced by approximately four to five decades. However, scalability of Y_2O_3 grown by ALD to below 1 nm (EOT) may be problematic due to the interfacial oxide issue caused by the ozone reactivity.

c) Al_2O_3 results

As discussed above, a thin interlayer of SiO_x is often present between high-K layer(s) and the Si substrate, either as a results of deposition reaction or as a necessary "template" to achieve uniform depositions. Minimizing the thickness of the interlayer is important to reduce a parasitic effect of series capacitance in the gate stack. Recently, we demonstrated [15] Al_2O_3 can be deposited uniformly directly on Si without an interlayer (see also Fig. 13). By comparing high-frequency and quasi-static CVs for Al_2O_3 stacks after oxygen and forming gas anneals (Fig. 12), one can conclude the interface quality is quite good. The leakage current is lower than that of SiO_2 (Fig. 14), though not as by much as in the case of ZrO_2, HfO_2, and Y_2O_3 (because of the lower dielectric constant, approximately 10). Another difference between Al_2O_3 and ZrO_2, HfO_2, Y_2O_3 depositions is that as-deposited Al_2O_3 films are amorphous (Fig. 13) whereas the other three films show microcrystalline structure. Upon annealing at high temperatures, Al_2O_3 film undergoes a structural transformation too. More details on materials and electrical properties of ultrathin ALD Al_2O_3 films can be found in our other recent publications. [15, 16]

d) Thermal stability on silicon

Thermal stability of high-K gate dielectrics (especially in the contact with Si) is an important issue since high temperature (>1000 C) activation anneals are required for conventional (poly-Si) CMOS process flow. Our studies show that not all the materials satisfy these requirements. For example, ZrO_2 films react with the Si substrate forming zirconium silicide. Of the four materials studied, Al_2O_3 exhibits best thermal "robustness". In fact, we fabricated short-channel poly-Si gated transistors with Al_2O_3 gate stack using conventional process flow. [16] Lower thermal budget process schemes (e.g. replacement gate) are under investigation for materials with lower thermal stability.

In summary, an analysis of basic physical and electrical properties of ultrathin ZrO_2, HfO_2, Y_2O_3, and Al_2O_3, gate has been performed. Important properties of the materials are summarized in Table 1. Thermal stability data were obtained with the help MEIS on uncapped (i.e. vacuum/high-K/Si) structures.

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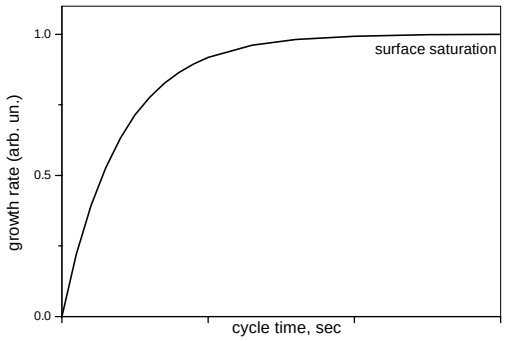

Fig. 1 Typical deposition rate vs. ALD pulse length curve.

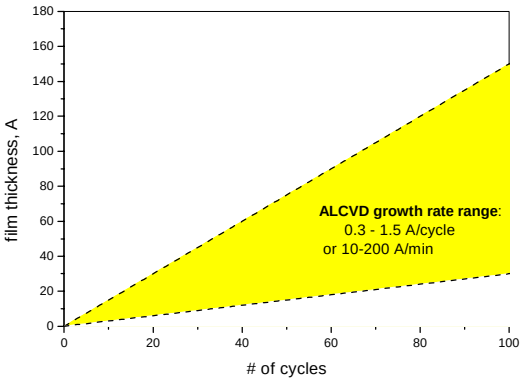

Fig. 2 Schematic illustration of ALD growth rate

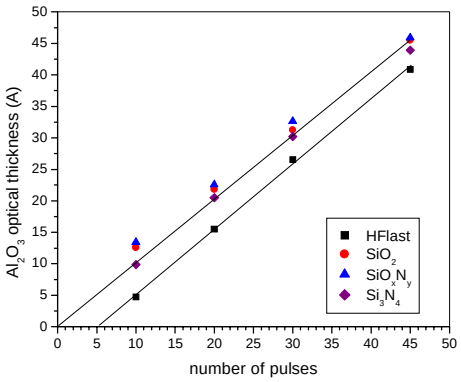

Fig. 3 Data on Al_2O_3 depositions on different initial surfaces

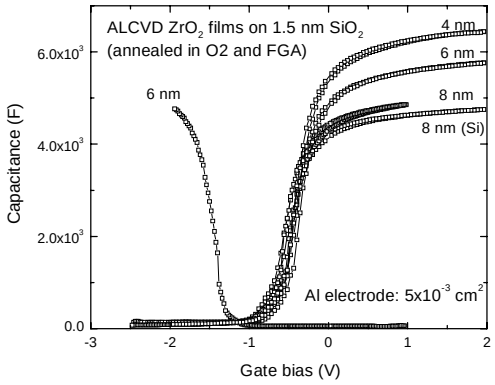

Fig. 4 CV characteristics for ZrO_2

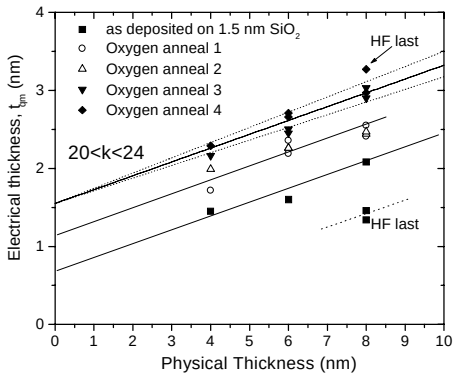

Fig. 5 Electrical (Tqm) vs. optical thickness for ZrO_2

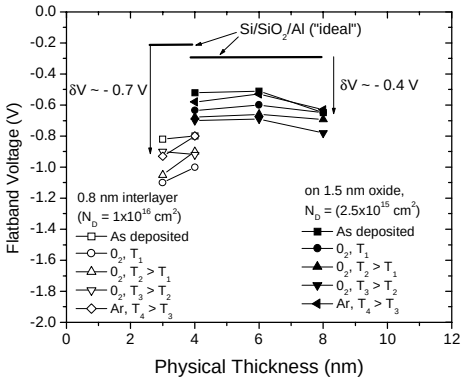

Fig. 6 Flatband voltage shifts for ZrO_2 stacks for various postdeposition treatments.

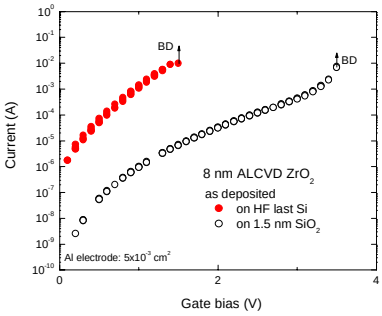

Fig. 7 Leakage current vs.Vg for ZrO_2 films deposited on SiO_2 and hydrogen terminated surface.

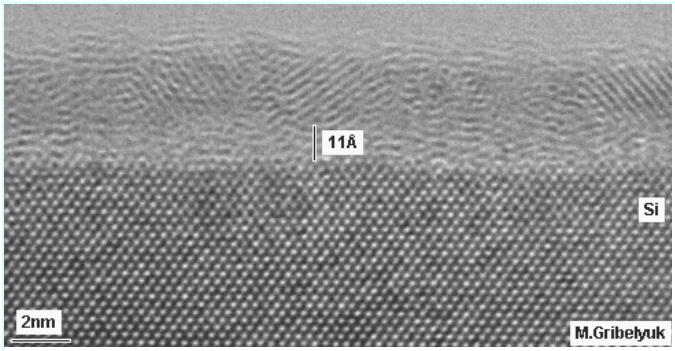

Fig. 8 HRTEM on Y_2O_3 deposited on HF-treated Si.

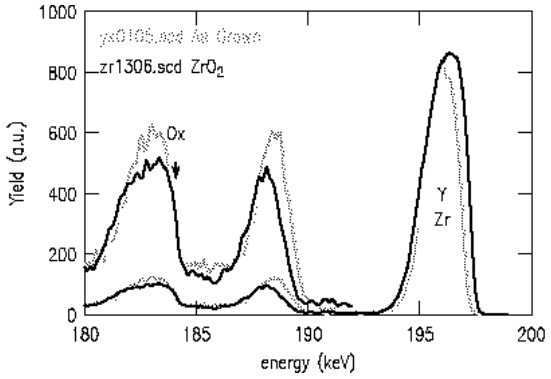

Fig. 9 MEIS spectra for thin Y_2O_3 and ZrO_2 films

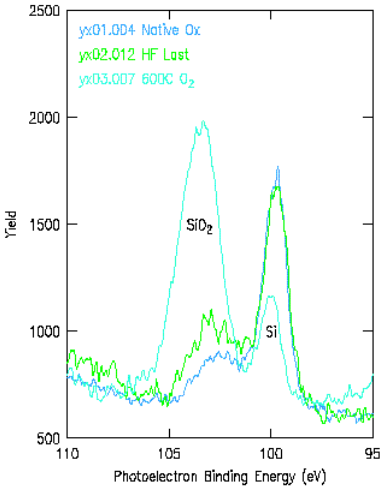

Fig. 10 Si 2p core-level XPS on Y_2O_3 films: (i) deposited on HF-last surface; (ii) thin SiO_2; and (iii) after 600°C anneal in oxygen.

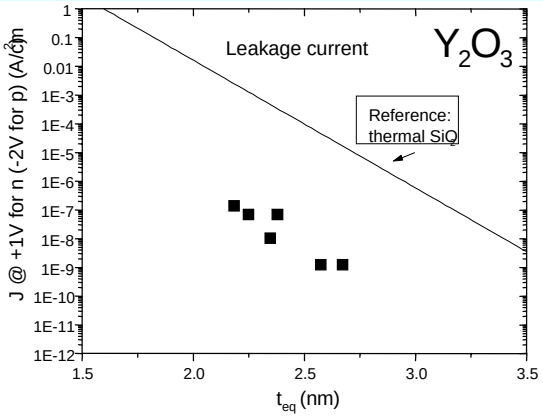

Fig. 11 Leakage current density for Y_2O_3

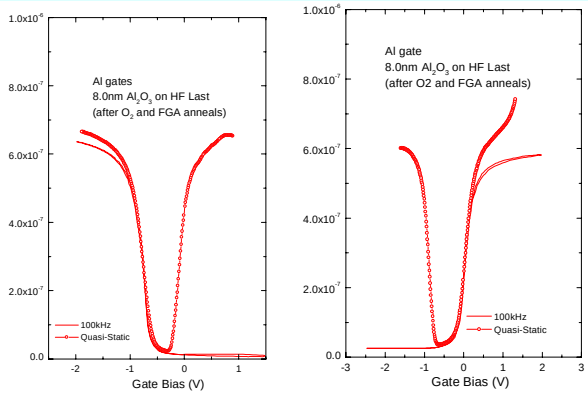

Fig. 12 HF and QS CVs for Al gated Al_2O_3 on p- and n- Si

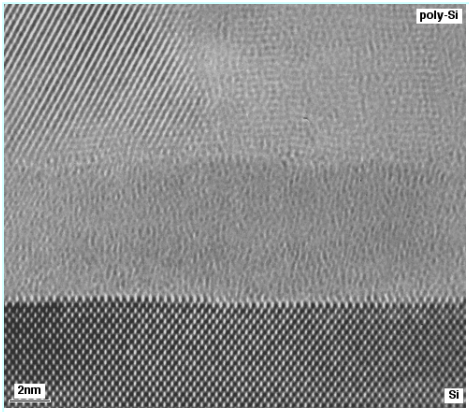

Fig. 13 HRTEM of the poly-Si/Al_2O_3/Si system.

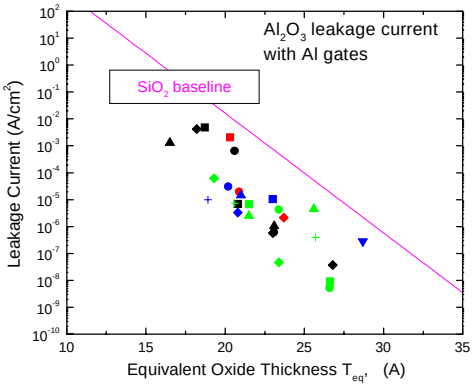

Fig. 14 Leakage current for Al_2O_3 capacitors with Al gates

Table 1.

High-K Material	**Dielectric Constant**	**Leakage Current reduction (wrt SiO_2)**	**Thermal Stability, T_{max}, C (MEIS data)**
ZrO_2	~ 23	x 10^4 - 10^5	~ 900
HfO_2	~ 20	x 10^4 - 10^5	~ 950
Y_2O_3	~ 15	x 10^4 - 10^5	silicate formation
Al_2O_3	~ 10	x 10^2 - 10^3	~ 1000

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