Patterning Pentacene Organic Thin Film Transistors

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Abstract:

Organic semiconductors have demonstrated excellent electrical performance in some cases rivaling inorganic systems in use today. These materials, which are processed at or near room temperature, have attracted considerable interest because they would enable the creation of active circuitry on organic substrates leading to a new generation of displays, radiofrequency identification systems, and smartcards. Many of these materials are intolerant to wet processing, however. This has led to a major processing limitation: the lack of a subtractive photolithographic patterning process to define active regions of the semiconductor. This paper presents a process which uses a dry organic encapsulant (parylene) as a boundary layer between an organic semiconductor (pentacene) and photolithographic chemicals. Traditional photolithography may then be performed to use a dry etch to pattern the material stack. This process, which is fully subtractive, opens the path to the use of these materials in a wide range of applications.

Introduction

Organic semiconductors have evolved considerably in the last decade from a laboratory curiosity into a class of materials close to commercialization. High performance p-type materials are now commonly encountered in the literature, and n-type materials with rapidly improving performance have also been developed. Processing still remains a challenge, however. Patterning

organic semiconductors has in general been detrimental to their performance. This paper will present a simple technique for overcoming these limitations in pentacene and permitting a direct subtractive etch process for the organic layer.

Most known organic semiconductors are p-type. These materials, despite exhibiting much lower mobility at room temperature than crystalline inorganic semiconductors, behave very much like p-type inorganic semiconductors (albeit ones with low performance). Correspondingly, field effect transistors fabricated with organic active layers are typically modeled and measured using the same metrological parameters and figures of merit encountered in the literature of inorganic devices, such as mobility and on/off ratio. High performance organic thin film transistors (OTFTs) made using the organic semiconductor pentacene (currently the best organic semiconductor) show mobilities of the order of 1 $cm^2 V^{-1} s^{-1}$ and on/off ratios of about 7-8 orders of magnitude [1]. Progress continues to be made in improving the performance of these devices by optimizing deposition processes and device design.

Most deposition processes for high-performance organic semiconductors occur with the substrate at or near room temperature. This permits deposition on a wider variety of substrates, including plastic materials, which can be stronger and less expensive than glass [2]. Several product applications could benefit from the use of flexible, inexpensive, easily integrated active components such as flexible, active-matrix flat panel displays (AMFPD), radiofrequency identification tags, large area sensors, and low-end smartcards. While inorganic semiconductors already serve in many of these systems, all of these applications can benefit from the cost reduction and simpler integration organic devices offer.

The largest potential market for organic semiconductors is in displays, an area where single crystal silicon has not been very successful. Amorphous silicon and polysilicon have led

the market for AMFPDs despite the relatively high cost of processing and substrates (which is much lower than single crystal silicon, however). Performance and high areal density is not critical in this market; instead compatibility with large area circuitry and processability have determined design choices. Organic semiconductors enable the use of substrates, interconnects, and light modulation layers, which cannot be considered in inorganic systems processed at high temperature, leading both to less expensive and also new types of displays, including flexible displays.

Two basic approaches have been taken in the development of new organic semiconductors. One has been to try to develop soluble materials with high packing density. These materials are generally long chain polymers with high solubility in nonpolar solvents. The use of regioregular materials has advanced performance in this area considerably; regioregular polythiophene is a typical material of this class.[3],[4] These materials are typically drop-cast or spin-coated onto substrates. The other approach, which has produced materials with about an order of magnitude better performance, has been to use self-assembling short chain oligomers, such as hexathiophene[5], or fused-aromatic molecules such as pentacene [5],[6]. These materials are generally insoluble and must be vacuum deposited by molecular beam deposition methods. The material is vaporized from a heated effusion cell in ultra-high vacuum conditions onto substrates at or near room temperature. While this class of materials requires a vacuum step which complicates processing, intermolecular packing is significantly better. Performance is directly related to the degree of intermolecular packing and highly ordered structures produce transistors with the best performance [6],[7]

For both classes of materials patterning the semiconductor is difficult. The structure of the materials is generally optimal at deposition and most treatments degrade the material's

properties. The problem is most acute for short chain oligomers and small molecules. These materials have good packing due to their weak interaction with the substrate and high intermolecular interaction [6]. The deposition conditions used in a high performance process force the oligomers to pack into a continuous sheet of high order. Exposure to liquid solvents reduces the interaction between the semiconductor and the substrate leading to a strain relaxation of the film, which destroys its charge transport properties [8]. In some cases it can even lift off (delaminate) the organic film. This occurs even through the material may be insoluble in the solvent used. Most types of wet processing are therefore not an option for patterning short-chain oligomers.

Several approaches have been proposed in the literature for patterning organic semiconductors. None, however, is satisfactory for all applications. The most common laboratory technique is the use of shadow masking through metal, silicon membrane, or organic masks of varying sophistication. This technique, while well suited for the laboratory, is unable to produce features of high areal density and is unsuitable for manufacturing since the masks need to be cleaned and high resolution masks are fragile. Another technique commonly used is depositing the material onto reentrant or deep-gap photoresist profiles [9]. This technique has proven useful for the creation of logic circuitry, but is undesirable for many types of diplays since it leaves semiconducting material over the entire inactive area.

Benefits of patterning

In any discussion of patterning the a question often arises: is patterning even necessary? Many all-organic and mostly-organic circuits have been presented in the literature which have used a continuous layer of semiconducting material as the active layer (see, for example, [10]). There are three benefits to patterning the semiconductor, each varying in importance for different

applications and geometries: reduction of cross-talk, improvement of the on/off ratio, and removal of material from the optical path, in the case of a backlit display. Because p-n junctions may not be used to isolate transistors, lateral electrical cross-talk is a severe issue for OTFTs. In patterned gate applications (although this also holds to a lesser degree for unpatterned gates) nongated current carrying pathways contribute a constant leakage while gated pathways change in conductance. Removal of these peripheral paths decreases the off current while making no significant change in the on current. Finally, in shutter-based displays (such as TN-LCDs) the backplane should be as clear as possible for maximum brightness.

Experimental procedure

To demonstrate this process transistors were fabricated using the organic semiconductor pentacene. Details of the deposition setup and conditions may be found in reference [11]. Bottom-electrode inverted TFTs were fabricated on heavily doped silicon substrates with a thermally grown oxide. The highly conductive substrate serves as a common gate and the oxide as the gate dielectric. Electrodes were then vacuum deposited using a shadow mask to define their geometry (although nothing prevents the use of photolithographically defined electrodes). This process is not specific to bottom or top electrode geometries but the bottom contact geometry (Fig. 1) is the only one compatible with a fully lithographic process. The materials were then encapsulated with approximately 1 micron of parylene, a dry deposited polymer which forms an excellent conformal coating. Regular photolithography without post-bake and a dry oxygen reactive ion etch was used to complete the patterning process [12]. Figure 1 shows the resulting stack.

In the best performing samples the photoresist was not removed from the patterned semiconductor. The use of solvent agents to remove the resist in other devices reduced the

performance of the transistors, typically halving the mobility measured before solvent exposure. While the complete device destruction which occurs in unprotected devices is not seen, once the parylene barrier is breached immersion of the devices in solvents degrades the device performance. If photoresist removal is needed it can be accomplished by overetching the samples down to the parylene layer. The parylene layer does not have to be removed. It may actually have a positive effect since it can be a surface barrier that prevents environmental contaminants, such as water, from reaching the pentacene layer.

Results

The current-voltage curve of a device etched using this technique is shown in figure 2. The device has a mobility of 0.08 $cm^2 V^{-1} s^{-1}$. This performance is typical of devices produced under these conditions (bottom contact devices have lower performance than top contact devices [13], and the substrate was held at room temperature) but have the pentacene layer patterned with a shadow mask during deposition. Thus we have demonstrated that this protection mechanism produces working devices. Parylene coatings are very well suited to this type of encapsulation. The material is deposited onto the substrates at room temperature and polymerizes during the deposition process into a solvent-resistant, chemically inert film. This barrier is key to the patterning process; it protects pentacene against any contact with the solvents used for the photolithographic process. A micrograph of an etched device is shown in figure 3.

Both parylene and pentacene are easily etched in a reactive ion plasma process. While further studies are needed to determine if there is radiation damage which might deteriorate semiconductor performance, there is no indication at this stage that any such damage occurs. The test devices used exhibit performance comparable with control devices patterned by shadow masking. This good performance is proof that the parylene protects pentacene fully; control

devices patterned without a protective layer were completely destroyed by their contact with photolithographic processing chemicals.

To demonstrate compatibility with transparent organic substrates, care was taken to not heat the samples above 100 C. The photoresist was soft-baked at 90 C and used directly in the soft-baked stage. Certainly, problems using this process with organic substrates may remain to be solved (such as substrate shrinkage), but the path is clear for a fully subtractive pentacene process. Heating in air after encapsulation with parylene appears to have no effect on pentacene performance.

The wider applicability of this process is also clear. The extension to other short chain oligomers is straightforward, but this process may also be used to simplify the processing of soluble organic materials. This may also be extended to non-transistor applications, such as organic LEDs.

Conclusion

Processing pentacene and other organic semiconductors has traditionally been difficult. The simple test vehicles developed in laboratories to study the material's properties have proven to be inadequate for scaling up the use of the material in large circuits. The use of shadow masking, in particular, has been extremely limiting. Progress in isolation has been made to date, but it has served only the electrical functions of isolation. A fully subtractive solvent- and water-free process is needed for display applications. This paper has presented a technique which patterns pentacene using such a process providing both electrical isolation and removal of the material from the substrate where it is unused. This permits the use of pentacene in displays, where having a semiconductor film in the optical path would be undesirable. This process may

also be applied in other applications where pentacene active circuits will be useful, such as in smart cards.

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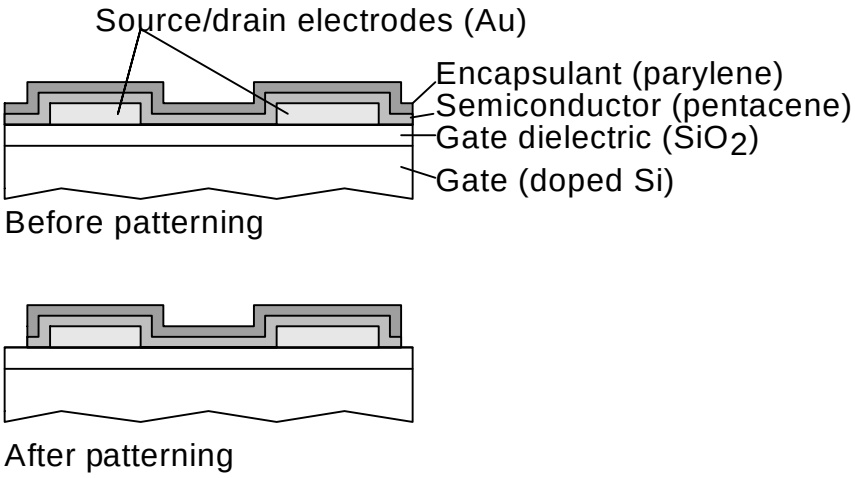

Fig.1. Schematic of deposition process and structure after patterning.

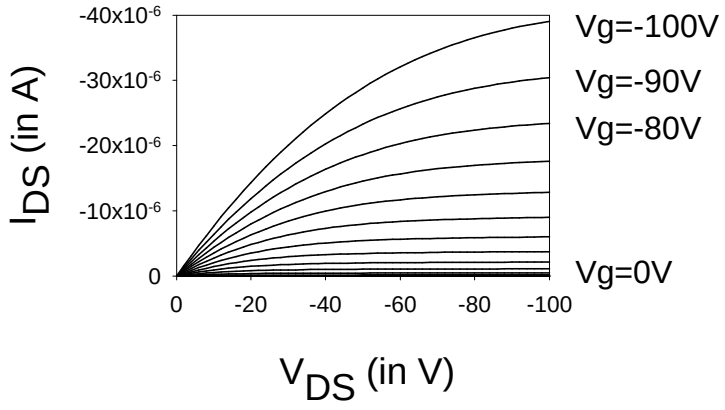

Fig. 2. Current-voltage characteristic of an OTFT produced using this process. The performance observed is what we had measured from shadow-masked, bottom-contact OTFTs. Channel width, W=1500 μm, channel length, L=70 μm

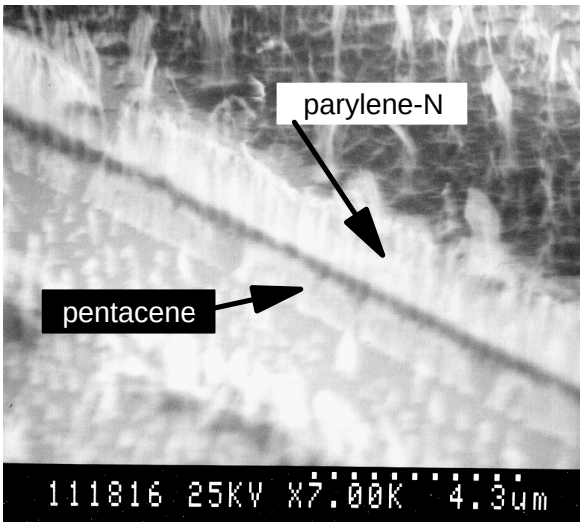

Fig. 3. A micrograph of a field effect transistor etched using this process. The edges of pentacene and parylene are clearly visible.