RC22177 (W0109-031) September 18, 2001
Electrical Engineering

IBM Research Report

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Sub-40nm SOI V-groove n-MOSFETs

J. Appenzeller, R. Martel, Ph. Avouris, J. Knoch, J. Scholvin, J. A. del Alamo, P. Rice, and P. Solomon

Abstract— **We present output and transfer characteristics of single-gated, 36nm, 46nm and 56nm channel length SOI MOSFETs with a V-groove design. For the shortest devices we find transconductances as high as 900μS/μm and drive currents of 490μA/μm at V_{gs}-V_{th} = 0.6V. The V-groove approach combines the advantages of a controlled, extremely abrupt doping profile between the highly doped source/drain and the undoped channel region with an excellent suppression of short-channel effects. In addition, our V-groove design has the potential of synthesizing devices in the 10nm range.**

Keywords— **V-groove MOSFET, single-gated device, SOI, ultra-short channel**

I. Introduction

IN PAST years opinions about the ultimate scaling limits of MOSFETs have often been revised. Experimentalists have proven that aggressive scaling results in high performance devices in the sub-50nm channel length regime [1], [2], [3], [4]. The question of how far can MOSFET size scale - while obtaining improved device characteristics - remains open.

To address this question we have recently proposed a concept based on a V-groove MOSFET that is capable of generating transistors with source/drain separations as small as 10nm [5]. The potential of our approach becomes obvious from the device cross-sectional view shown in Fig. 1 b).

In the V-groove MOSFET, raised thick highly n-doped silicon regions on top of an ultra-thin p^- body serve as low resistive source and drain. The ultra-thin body effectively suppresses short-channel effects due to electron confinement and a single-gate design is sufficient to fully control charge transport in the channel. An extremely abrupt transition in the doping profile between the source/drain and channel region of the device is ideal to precisely control the device dimensions. Obtaining this is not possible through any ion implantation technique but it can be achieved by epitaxial growth. In addition, thanks to the low doping level in the body, this design does not suffer from mobility degradation due to ionized impurity scattering that is prevalent in highly doped body designs. For this reason also, this design is rather immune to pn-leakage currents and dopant fluctuations which can cause non-reproducible device behavior in ultra-short channel MOSFETs. From all these arguments, excellent electrical performance is to be expected.

In this article we demonstrate sub-40nm high-performance V-groove n-MOSFETs. We also discuss that a reduction of channel length towards 10nm while still achieving improved device characteristics seems to be well feasible using our V-groove ansatz.

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II. Device Fabrication

The device fabrication is based on the combination of epitaxial silicon growth and its anisotropic wet chemical etching. First, molecular beam epitaxy (MBE) was em-

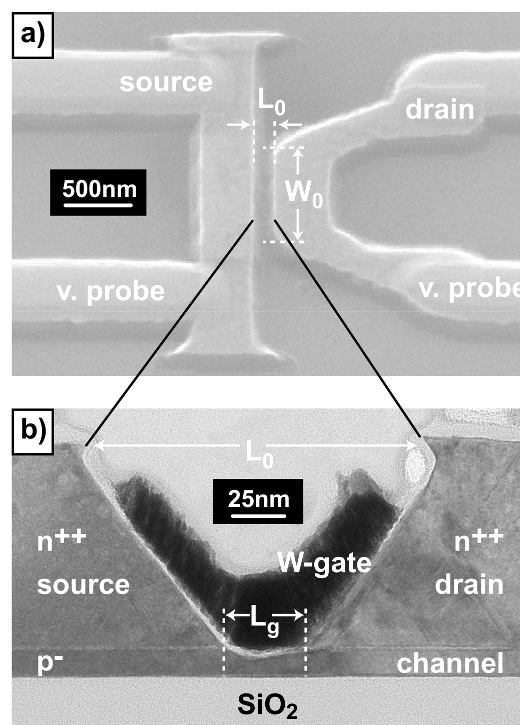

Fig. 1. a) SEM top view of a 36nm V-groove MOSFET before gate oxidation and gate metal deposition. L_0 is the V-groove opening, W_0 the transistor width of around 700nm. Two source and two drain contacts are connected to allow to perform four-terminal measurements. b) TEM image of the same MOSFET device. Tungsten (W) is used as a metal gate. Electron transport takes place in the channel of length L_g = 36nm in the p^- region.

ployed to grow an n^{++} layer of silicon with an antimony dopant concentration of $\sim 10^{20}\mathrm{cm}^{-3}$ on an SOI substrate with a 15nm nominally undoped silicon-(100) layer ($p^- \sim$

$5\times10^{14}cm^{-3}$). The high n^{++} doping level is essential in order to reduce series resistances as pointed out before and to minimize the depletion of the contact region. MBE growth ensures that an extremely abrupt interface is generated.

This stack was then patterned using electron beam lithography and an anisotropic silicon etch. By means of etching silicon in a KOH solution, a V-groove with flanks defined by the {111} silicon planes can be fabricated in a self-limiting way [6]. Cutting through the n^{++} layer, two isolated regions (source and drain) - only connected through the ultra-thin p^- body were created. (A detailed description of the process flow can be found elsewhere [7].)

The silicon pattern as defined after the V-groove formation is displayed in Fig. 1 a). In the particular case shown, the V-groove opening L_0 was 155nm and the transistor width was $W_0 = 700$nm. To perform four terminal measurement two contacts exist for both source and drain respectively. It is important to mention that because of the self-limiting nature of the anisotropic etch-approach not only the V-groove but also device-to-device isolation was accomplished through the etch step.

After the V-groove definition a 600°C gate oxidation process was employed to generate a 26Å dielectric film between the gate and the channel [8]. The low growth temperature during oxidation is essential to preserve the abrupt transition between source/drain and the channel. For these first devices we conservatively used a rather thick gate oxide. Device fabrication was finished defining a tungsten-gate within the V-groove (black area in Fig. 1 b)).

Interestingly, Fig. 1 b) clearly reveals that the tip region of the V-groove, thus the channel region of the transistor is rather flat. This behavior is a result of the ex-situ cleaning before epitaxial growth of the n^{++} film. Presumably the adsorption of carbon and oxygen at the interface between the channel and the source/drain layer slows down the etch rate between the n^{++} film and the p^- body [5]. Due to this etch stop layer we were able to fabricate 36nm (see Fig. 1 b)), 46nm and 56nm devices respectively by increasing L_0 stepwise. (Mention, that a V-groove opening of 155nm defines a channel of only $L_g = 36$nm in length.) For larger V-groove openings the channel layer gets fully consumed and no transistor action was found.

III. Experimental Results and discussion

Figure 2 shows the results on a typical 36nm V-groove MOSFET. The measurement was performed at room-temperature in a four-terminal configuration to exclude the impact of series resistances from source and drain as far as possible. However, our data still contain a 150 to $200\Omega\cdot\mu m$ extrinsic resistance contribution as confirmed by the analysis of the G_{ds} versus V_{gs} data for small V_{ds} values and in agreement with calculations of the spreading resistance contributions from the wedge-shaped n^{++} source/drain regions. We found a maximum transconductance of $g_m = 900\mu S/\mu m$ and a drive current of $I_d = 490\mu A/\mu m$ at $V_{gs} = V_{ds} = 1.1V$ ($V_{th} \approx 0.5V$). Both, g_m and I_d were *not* corrected to account for the aforementioned series resistance. These data are particularly impressive since our gate oxide is rather thick. For the devices with $L_g = 46$nm and 56nm, g_m was determined [1] to be $\approx 750\mu S/\mu m$ and $\approx 600\mu S/\mu m$ respectively. The clear trend of transconductance as a function of channel length seems to indicate that saturation velocity is not reached in our devices.

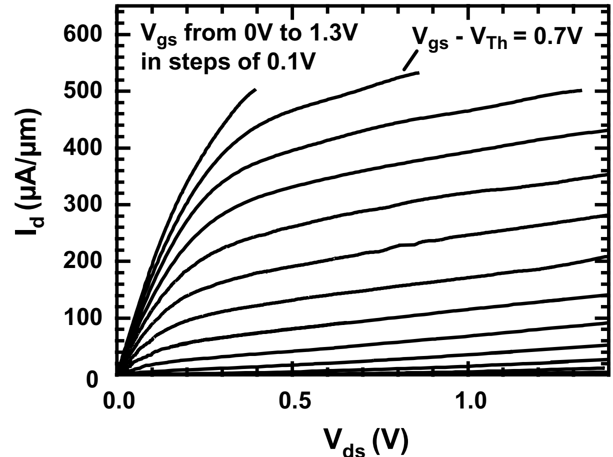

Fig. 2. Output characteristics of a 36nm ultra-short channel lengths MOSFETs.

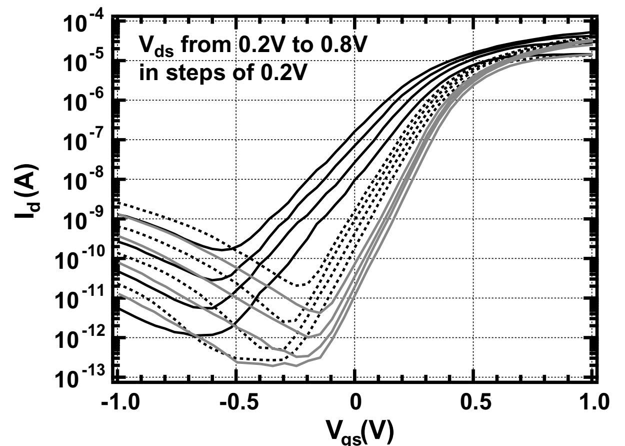

Fig. 3. Sub-threshold characteristics for devices with L_g equal to 36nm (straight black lines), 46nm (dotted black lines) and 56nm (straight gray lines) for V_{ds} ranging from 0.2V to 0.8V.

This is also consistent with a rather low mobility of approximately $\mu = 100cm^2/Vs$ extracted for the 36nm de-

[1] The effective channel width of the devices was found to decrease with increasing L_g. This is the case since the etch stop layer at the n^{++}/p^--interface is not perfectly uniform. The larger L_g the more likely that parts of the channel get consumed by the KOH-etch. To determine g_m correctly, the electrical channel width of the larger devices was determined from the G_{ds} vs. V_{gs} data for small V_{ds} values by comparison with the 36nm transistor data.

vices. Surface roughness may be responsible for the deviation of μ from the universal mobility behavior.

In Fig. 3 the subthreshold characteristics for the three device types under investigation are displayed for comparison. The subthreshold slopes are 160mV/dec, 90mV/dec and 80mV/dec for the 36nm, 46nm and 56nm transistors respectively. The corresponding DIBL is 314mV/V, 171mV/V and 128mV/V. The change in slope goes along with a monotonous decrease in the off-current and DIBL with increasing channel length. All these trends are symptomatic for an increased impact of short-channel effects for smaller transistors. This is the case when the channel length becomes comparable to the body thickness of the channel. Simulations of the impact of the body thickness in ultra-small MOSFETs [9], suggest that significant improvements in the 36nm devices can be expected for a body thickness in the range of 5nm.

Fig. 3 also shows an increase of current for negative gate voltages for all channel lengths. For large enough negative V_{gs}, gate induced band-to-band tunneling occurs and electrons can travel through the channel region via the raised valence band, resulting in an increase in I_d. As was experimentally verified, the increase in I_d does not originate in the gate.

TABLE I
COMPARISON BETWEEN DIFFERENT ULTRA-SHORT CHANNEL DEVICES

	Intel[a]	NEC[b]	Berkeley[c]	V-groove
L_g	30nm	24nm	15nm	36nm
g_m	1200 $\frac{\mu S}{\mu m}$	1000 $\frac{\mu S}{\mu m}$	400 $\frac{\mu S}{\mu m}$	900 $\frac{\mu S}{\mu m}$
t_{ox}	8Å	25Å	40Å	26Å
I_d[d]	514 $\frac{\mu A}{\mu m}$ at 0.55V	796 $\frac{\mu A}{\mu m}$ at 1.0V	190 $\frac{\mu A}{\mu m}$ at 1.2V	490 $\frac{\mu A}{\mu m}$ at 0.6V
S	100 $\frac{mV}{dec}$	140 $\frac{mV}{dec}$	150 $\frac{mV}{dec}$	160 $\frac{mV}{dec}$
I_{off}[e]	100 $\frac{nA}{\mu m}$	300 $\frac{nA}{\mu m}$	300 $\frac{nA}{\mu m}$	280 $\frac{nA}{\mu m}$

[a] see Ref. [2]
[b] see Ref. [3]
[c] see Ref. [4]
[d] at V_{gs}-V_{th}
[e] at $T = 300$K

Despite the fact that in the devices investigated so far the silicon body and the gate oxide thickness are not optimized, it is interesting to compare our results with recently published data on ultra-short channel n-MOSFETs. Table I displays a selected number of electrical characteristics for devices with channel lengths between 15nm and 36nm.

It is obvious from both, the transconductance data as well as the drive current values that our data compare well with state-of-the-art classical approaches [2], [3]. In contrast to the results from Kedzierski and co-workers [4] on thin body MOSFETs, our V-groove approach does not suffer from high source (or drain) to channel contact resistances. Subthreshold slope and off-current of our devices are very comparable to those published by Wakabayashi and co-workers [3]. However, as pointed out above, our device design has the freedom to reduce the body thickness for smaller source/drain separations which is expected to substantially improve S as well as I_{off}.

IV. Summary

We have presented excellent electrical data on ultra-short channel n-MOSFETs with channel lengths down to 36nm. Our results clearly indicate the potential of single-gated thin-body SOI structures for sub-50nm transistors. The particular V-groove design employed allows the fabrication of even smaller devices. From the experimental data obtained so far we expect that high performance devices with excellent device characteristics can be obtained for single-gate SOI V-groove MOSFETs with channel length down to 10nm. It is crucial in this context to use an extremely thin body to achieve a well defined off-state of the transistor.

V. Acknowledgement

Device fabrication took place in part at the Microsystems Technology Laboratories of MIT, with financial support from IBM and at the Technical University in Aachen, Germany.

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