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Technology Trends in Power-Grid-Induced Noise

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ABSTRACT

With technology scaling, the trend for high performance integrated circuits is towards higher power dissipation, higher operating frequency and lower power supply voltages. This causes a dramatic increase in power supply current being delivered through the on-chip power grid and is recognized in the International Technology Roadmap for Semiconductors as one of the difficult challenges. The design of appropriate power grids and the addition of decoupling capacitance has become crucially important in order to control power-grid-induced noise. In this paper, we show analytical relationships between noise and various technology parameters, and we show the resulting trends in noise based on current roadmap predictions.

Keywords

power grid noise

1. INTRODUCTION AND MOTIVATION

Noise margins have been greatly reduced in modern designs due to the lowering of supply voltages, the corresponding lowering of threshold voltages, and the presence of a larger number of potential noise generators that eat significantly into the noise margins built into a design. The power grid provides the power (denoted by V_{dd}) and ground signals throughout a chip and supply voltage variations can lead not to delay variations, which can in turn cause malfunction, or even to spurious transitions when dynamic logic is used [1]. Thus it is vitally important to model and predict power supply performance from a noise perspective.

Chip power supply models can be very large, in the range of millions of components and nodes, and the analysis of such large systems is challenging in itself [2]. In this paper, however, we focus on simple equivalent-circuit models for power grids which are amenable to analytical modeling. We then use these analytical models to understand the impact on power grid noise of the various parts of the power delivery system. We also study the trends in the values of the various component parts based on the ITRS [3] and other documents, and translate those into trends for noise.

2. CANONICAL POWER GRID CIRCUIT

Consider the circuit shown in Fig. 1, which can be thought of as a canonical model of a power grid and loading circuit. We make the following assumptions:

- The V_{dd} and Ground nets are largely symmetric and so it suffices to consider the V_{dd} net alone, i.e. with an ideal ground.
- The package is predominantly inductive, and is modeled by the series inductance L.
- The power grid is predominantly resistive, and is modeled by the resistance R_g.
- The circuit using the power grid is modeled by two components. First, switching circuits are represented by a time-varying current source (I_{load}) modeled using a simple triangular waveform with period T:

$$I_{load} = \begin{cases} 0 & : \quad t < 0 \\ \mu t & : \quad t < t_p \\ \mu(2t_p - t) & : \quad t < 2t_p \\ 0 & : \quad 2t_p < t < T \end{cases} \tag{1}$$

  Second, non-switching circuits are represented by the resulting decoupling capacitance, C_d. The power grid components *between* the switching and non-switching circuits are modeled by the resistance R_d.
- Any additional decoupling capacitance added to the circuit is modeled using C_d and R_d as well.

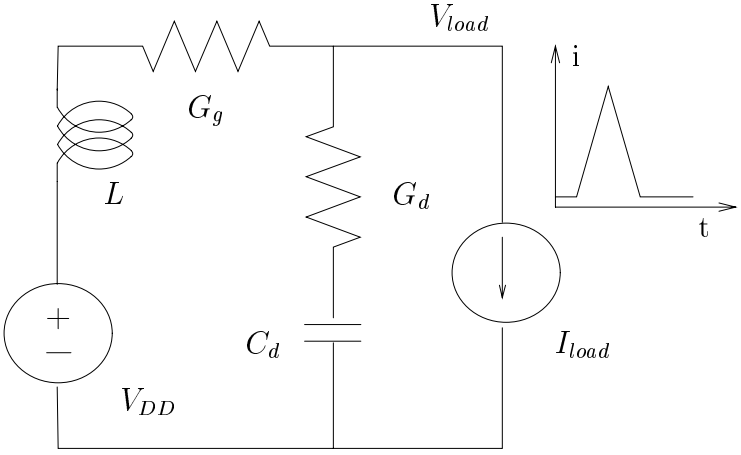

Figure 1: A canonical representation of a power network.

3. ANALYTICAL MODEL FOR POWER GRID NOISE

The circuit in Fig. 1 is simple enough that we can solve for the analytical form of the voltage delivered to the active circuitry, denoted by V_{load}, then determine the minimum such voltage and therefore the maximum power grid noise. We will do this for two cases:

1. The inductance L is set to zero, since this results in a far simpler result from which analytical insight is somewhat easier to gain.
2. The inductance L is included, but the resulting expressions are complicated and the insight is gained by making some simplifying assumptions.

3.1 Noise Model When $L = 0$

For the circuit shown in Fig. 1, we observe that V_{load} over the time interval from $t = 0$ to $t = t_p$ can be expressed as:

$$V_{load} = V_{dd} - \mu R_g \left(t - C_d R_g (1 - e^{-t/\tau}) \right) \tag{2}$$

where

$$\tau = (R_g + R_d) C_d \tag{3}$$

The minimum V_{load}, or maximum normalized power-supply-induced noise occurs at $t = t_p$ and the magnitude of the noise is:

$$V_{max} = \mu R_g \left(t_p - C_d R_g (1 - e^{-t_p/\tau}) \right) \tag{4}$$

It is interesting to take the Taylor expansion of Eq. 4):

$$V_{max} = \mu R_g \left(t_p - \frac{t_p R_g}{R_g + R_d} + \frac{{t_p}^2 R_g}{(R_g + R_d)^2 C_d} - \ldots \right) \tag{5}$$

We claim that terms in the Taylor expansion of order greater than one can be ignored, an approximation made increasingly more valid as C_d is increased. Thus for large $C_d >> t_p$, the behavior of V_{max} is dominated by the term:

$$\mu R_g \left(t_p - \frac{t_p R_g}{R_g + R_d} \right) \tag{6}$$

Continually increasing the decoupling capacitance C_d has little effect on the noise in the system. Instead, one ought to decrease the resistance associated with the decoupling capacitance R_d, pointing to the need to carefully control the *placement* of the decoupling capacitance in order to maintain control on R_d.

3.2 Noise Model With $L \neq 0$

When the inductance is included, the solution for V_{load} for the time interval from $t = 0$ to $t = t_p$ can be expressed as:

$$V_{load} = V_{dd} - \mu(L + R_g t - C_d R_g^2) + \psi_1 + \psi_2 \tag{7}$$

where

$$\psi_1 = (e_1 + e_2) \frac{\mu(L - C_d R_g^2)}{2} \tag{8}$$

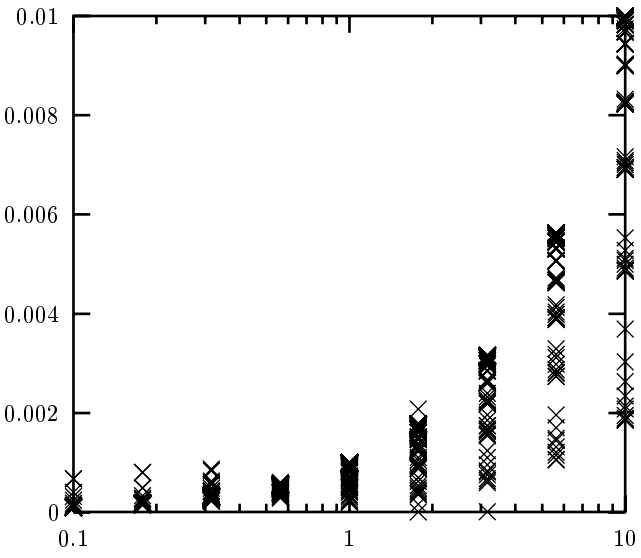

Figure 2: Eq. 13 vs. R_g

$$\psi_2 = (e_1 - e_2) \frac{\mu C_d}{2\beta} (\tau R_g^2 - L(3R_g - R_d)) \tag{9}$$

$$e_1 = \exp \frac{-(\tau + \beta)t}{2C_d L} \tag{10}$$

$$e_2 = \exp \frac{-(\tau - \beta)t}{2C_d L} \tag{11}$$

$$\beta = \sqrt{\tau^2 - 4LC_d} \tag{12}$$

In the case where the system is over-damped (i.e. β is *real*), we expect the minimum V_{load}, or maximum normalized power-supply-induced noise occurs at $t = t_p$ and the magnitude of the noise is:

$$V_{max}^L = \mu(L + R_g t_p - C_d R_g^2) - \psi_1 - \psi_2 \tag{13}$$

Note that if the system is not over-damped, the resulting overshoot and oscillations represent a far greater problem to the designer than the type of power grid noise we are tackling here. In such cases, treating the grid in the lumped-element manner implied by Fig. 1 might not be appropriate.

Again, we wish to examine this equation to gain insight. Due to the complexity of the equation, We start by calculating the maximum noise of a range of values of R_g, R_d, C_d, and L. Figures 2, 3, 4 and 5 show plots of the noise with respect to these parameters. The plots show that R_g is the dominant factor in determining the noise value. It turns out, however, that an approximation based on Eq. 4 suffices for most case:

$$V_{max}^L \approx V_{max} + \mu L \tag{14}$$

Fig. 6 shows a plot of the results of evaluating Eq. 13 and 14 for a range of values of R_d, R_g, C_d and L. We see that Eq. 14 is usually within a few percent of Eq., 13, especially

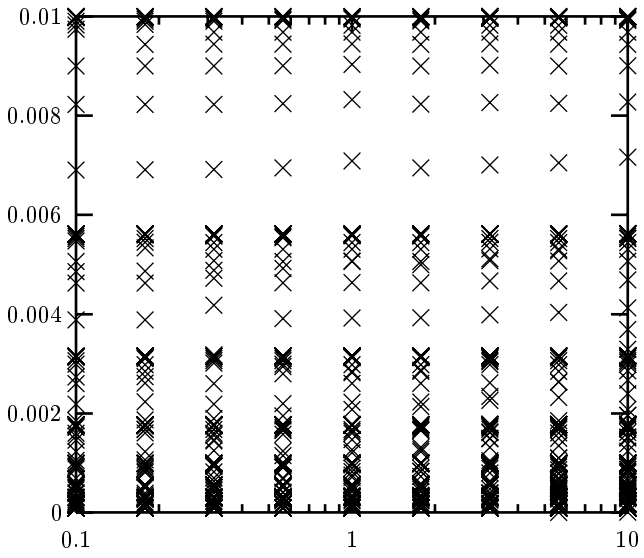

Figure 3: Eq. 13 vs. R_d

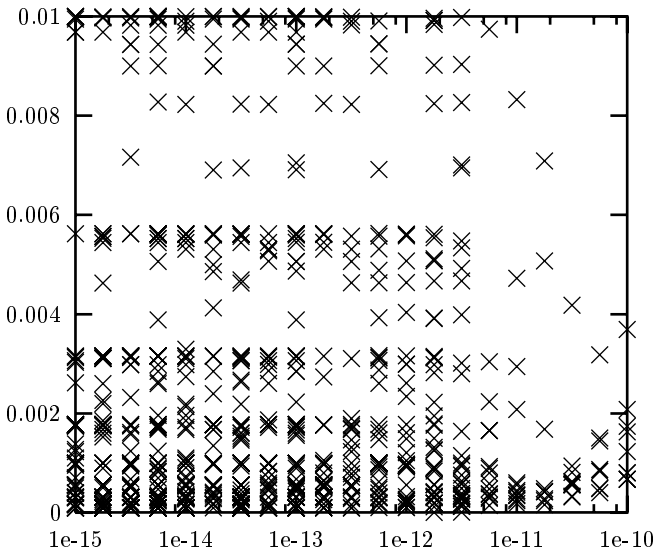

Figure 5: Eq. 13 vs. L

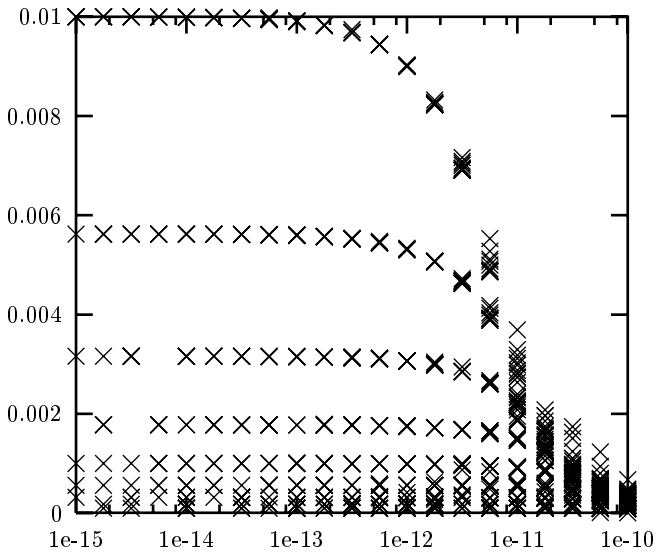

Figure 4: Eq. 13 vs. C_d

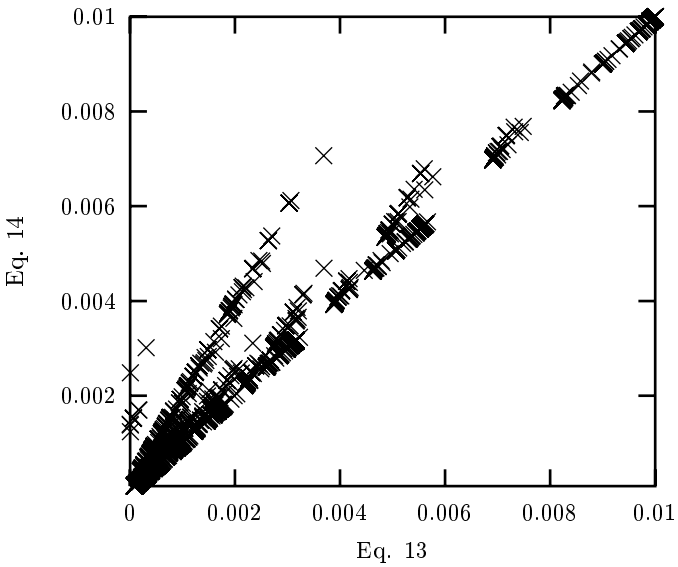

Figure 6: Comparison of Eq. 13 and 14

Year	L_{eff} nm	f MHz	V_{dd} V	Size mm^2	Power W	Density W/mm^2
1999	140	1200	1.8	450	90	*0.2*
2000	120	1321	1.8	450	100	*0.22*
2001	100	1454	1.5	450	115	*0.26*
2002	85	1600	1.5	509	130	*0.26*
2003	80	1724	1.5	567	140	*0.25*
2004	70	1857	1.2	595	150	*0.25*
2005	65	2000	1.2	622	160	*0.26*

Table 1: Trends in IC technology parameters.

when the noise magnitude is high, and that the estimate provided is pessimistic, making it safe to use in worst-case analysis.

4. TECHNOLOGY TRENDS

We will use data from the International Technology Roadmap for Semiconductors [3], summarized in Table 1, to predict the dependence of the load voltage V_{load} on the various circuit parameters in order to predict trends in power-grid-induced noise with technology scaling. The table shows the projected yearly trends for the effective length L_{eff}, of a transistor, the circuit frequency, f, the supply voltage level, V_{dd}, the chip size, the power dissipation and the density of power dissipation per unit area.

In analyzing the roadmap data for trends, we make the following first order approximation:

- The characteristic time for the load current source $t_p \propto f^{-1}$. This assumes that the same circuit family is pushed to a higher frequency, resulting in a general compression of relevant voltage and current waveforms at a rate proportional to operating frequency.
- The power per unit area, i.e. power density, $P_{\square} \propto V_{dd}\mu t_p$ since the maximum current is μt_p. From this we can infer that the slope of the current $\mu \propto P_{\square} f / V_{dd}$.

Based on the trends in Table 1, t_p decreases by about 0.6X across the table, while μ increases by about 3.25X.

A harder problem is the analysis of trends in the power supply parameters themselves since such trends are a function of design particulars such as number of metal layers, pitch and width of power grid wires, and the relative among of wiring resources (area) allocated to the power grid. We make the following observations:

- Power grid wires are rarely minimum width, so the dependence of power grid performance on overall back-end lithography capabilities is nil.
- Once a power grid spans more than 4 layers of metal, the benefit of additional layers of metal becomes progressively smaller. Thus the dependence of power grid performance on the number of layers of metal is a relatively weak function.
- With no change in the relative amount of area allocated to decoupling capacitance, the ratio of C_d to the maximum current μt_p should remain fairly constant since -to first order- the maximum device current can be expressed as:

$$I_{ds} = C_{ox} K \left(V_{dd} - V_T\right)^2 \qquad (15)$$

  where C_{ox} is the gate oxide capacitance which is directly proportional to the decoupling capacitance.
- The package inductance L is a strong function of package *cost*. It is not likely that current packaging technology will result in packages of significantly reduced inductance without cost increases. Thus a safe assumption is that L stays approximately the same.

Keeping the comments above in mind, we re-examine the equation for maximum noise relative to the power supply V_{dd}:

$$V_{noise} = \frac{\mu}{V_{dd}} \left(L + R_g t_p - C_d R_g^2 (1 - e^{-t_p/\tau}) \right) \qquad (16)$$

Based on the trends in Table 1 we observe that over the interval from 1999 to 2005:

- V_{dd} decreases by about 0.6X.
- t_p decreases by about 0.6X.
- μ increases by about 3.25X.
- C_d increases by about 1.95X.
- L, R_g and R_d stays approximately constant.

We see that the major source of concern is the fact the μ/V_{dd} is increasing by about 5.4X. Given that L is constant and that t_p is changing relatively modestly, the situation demands radical improvement of the decoupling term $C_d R_g^2 ...$ in Eq. 16 in order to keep noise constant.

5. CONCLUSIONS

This paper has presented an analytical formulation for power grid noise as a function of key technology and design parameters. The results show that recent trends to lower power supply voltages, faster frequencies and increased power dissipation result in dramatically increased power grid noise which can be controlled by careful decoupling capacitance placement and sizing. This points to the need to do early power estimation, power grid design, and decoupling capacitance sizing in order to avoid costly re-design.

6. REFERENCES

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