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PHYSICAL MODELS OF ULTRA THIN OXIDE RELIABILITY IN CMOS DEVICES AND IMPLICATIONS FOR CIRCUIT RELIABILITY

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ABSTRACT

An extensive review article on the physics of oxide breakdown has recently been published (1, 2). This manuscript gives a brief summary and an update with some further comments on the subject.

DEFECT GENERATION BY ELECTRONS, HOLES, OR HYDROGEN?

The idea that oxide breakdown from electrical stress is ultimately caused by the gradual build-up of defects is now widely accepted. This is illustrated schematically in Figure 1. The rate of defect generation (P_g) is strongly voltage dependent below 5 V (3). The critical defect density (N^{BD}), which determines the breakdown point, is strongly thickness dependent between 3-6 nm (3). This has been explained quantitatively by a percolation model (4).

Still not agreed upon, in spite of decades of research, is the microscopic nature of the defects and the mechanisms by which they are generated. However, two major models for the generation mechanism have come to the forefront of recent debates. These are the hydrogen release model (5-7) and the anode hole injection (AHI) model (8-10). (The third well-known model, the electrochemical or "E" model, (11) will not be discussed in this brief paper.)

The evidence for hydrogen involvement in defect generation and breakdown is circumstantial but strong, notably the observation of substrate dopant passivation (12) and hydrogen redistribution (13) during hot electron stress, the enhanced degradation rate of hydrogen-soaked films, (14) and experiments showing that exposure of bare SiO_2 films to atomic hydrogen radicals, in the absence of any electric field, produces electrically active defects essentially identical to those produced by electrical stress or radiation (6, 7, 15-26). The purported mechanism is shown schematically in Figure 2.

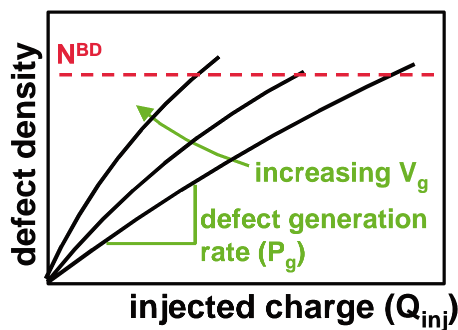

Figure 1. Mechanism of defect generation to breakdown in ultra thin SiO_2.

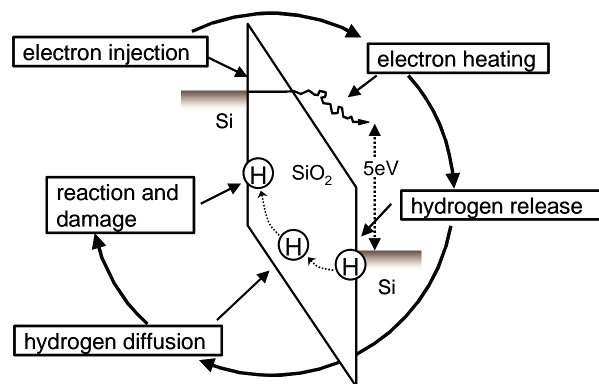

Figure 2. Hot electron induced hydrogen release mechanism of defect generation.

The 5 eV threshold is in reasonable agreement with electron beam desorption of hydrogen from Si surfaces (27). Once released from the anode, the hydrogen (mostly in the form of protons) (28, 29) may react to form defects in the SiO_2, as explored in recent calculations (30, 31).

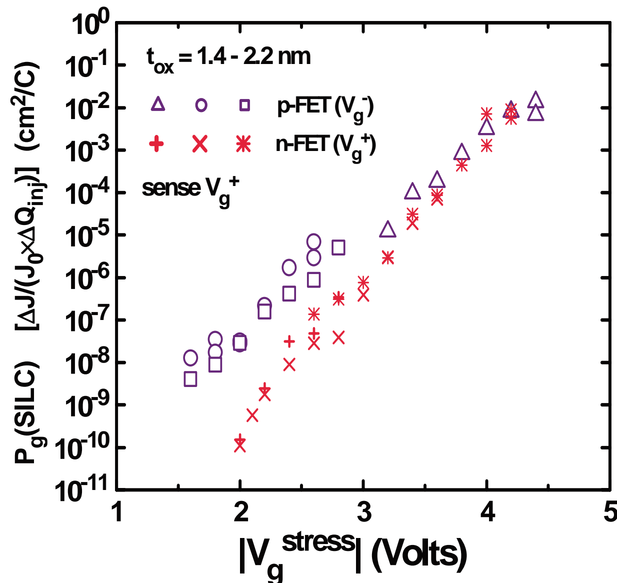

Figure 3. Defect generation probability for holes (p-FET) or electrons (n-FET).

In (1, 2) we pointed out that the AHI model does not correctly predict the magnitude of the defect generation rate. According to (9), at low gate voltage (*e.g.* 2-3 V) the hole current is at least 12 orders of magnitude lower than the primary electron current. Therefore, the defect generation probability per hole (P_g^h) should be very much greater than the probability per injected electron (P_g^e). In contrast, experimental data (Figure 3) show that the defect generation probability is similar (within a factor 10^2) for holes or electrons (29).

On the other hand, the AHI model supposes that only the hot holes with energy ~5 eV below the Si valence band are responsible for the damage leading to breakdown. Therefore, one should compare the value of P_g^h for hot holes at this energy to the value of P_g^e for the primary electron current at ~2-3 eV. According to Figure 3, these quantities differ by a factor of 7-10 orders of magnitude at most, which is still not enough to prove that the hot hole current can cause more damage than the primary electron current.

Given uncertainties in both experiment and theory, numerical arguments such as this may not be conclusive. There are other experiments, however, which are problematic for the AHI model. The AHI model of (9, 10) asserts that the energy of the hole in the oxide band gap (or at the anode Si/SiO_2 interface) controls the defect generation rate. This has been examined in detail by DiMaria (29). It was shown that, for ultra-thin oxides, P_g^h is the same for cold holes (tunnelling from a hole inversion layer) as for hot holes (injected from a *p* substrate into the *n*-well of a pFET), when P_g^h is expressed as a function of the energy of the holes at the p^+ gate, i.e. the cathode. This energy is $|V_g|$ for cold holes or $|V_{well}+\phi_{p/n}-V_g|$ for hot holes, where $\phi_{p/n}$ is the contact potential difference of 1.1eV between the hole inversion layer and the *n*-well, for near-ballistic transport. Therefore, the defect generation depends mostly on the energy carried by the holes when they strike the cathode, not on their energy in the anode. When the oxide is made thicker (>2-3 nm), few hot holes are able to tunnel through the oxide, and only then does the

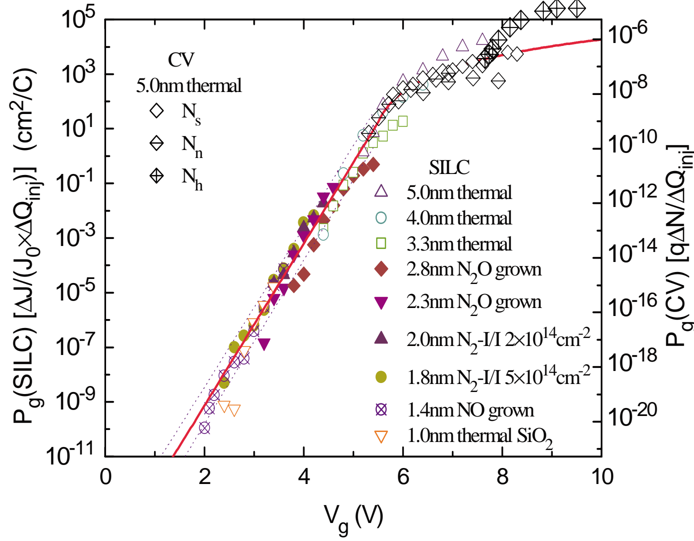

Figure 4. Defect generation probability measured from SILC (P_g(SILC)) and CV stretch-out (P_g (CV) and N_s), and electron and hole trapping rates (N_n and N_h, respectively), as a function of stress voltage for various oxides.

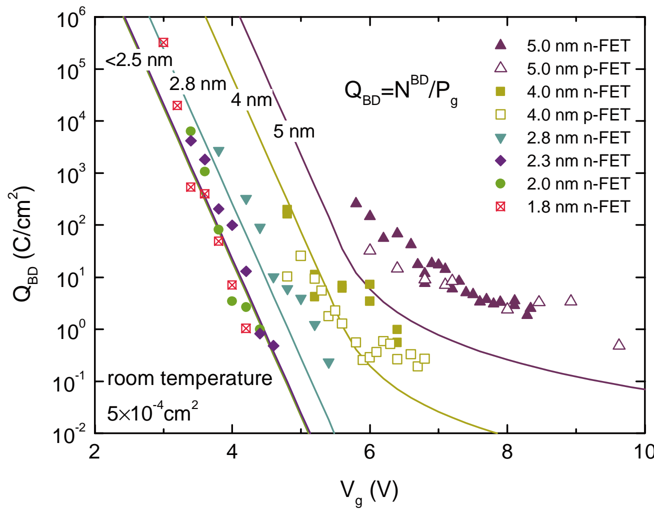

Figure 5. Charge-to- breakdown as a function of stress voltage for various oxides. The lines are calculated from $Q_{BD}=N^{BD}/P_g$ using the P_g data of Figure 4, and a thickness dependent N^{BD}. There is no feature corresponding to the hole trapping threshold in Figure 4.

defect generation become controlled by the energy of holes impinging on the Si/SiO_2 interface (29).

Measurements of hole trapping probabilities as a function of gate voltage (32, 33) show no correlation between anode hole generation and oxide breakdown. This is shown in Figures 4 and 5.

Figure 4 shows the hole trapping probability (N_h) with a hole injection threshold at ~7.5 V (32), in addition to the interface state (N_s) and bulk electron trap (N_n and SILC) generation. The offset between the hole trapping threshold and the trap generation threshold clearly establishes the sub-threshold tail as being related to the trap creation (hydrogen release) process and not anode hole injection. Figure 5 shows charge-to-breakdown (Q_{BD}) data as a function of voltage for various oxides. The feature in Figure 4 corresponding to the onset of hole trapping is not seen in the Q_{BD} data.

OXIDE LIFETIME VS. PRODUCT LIFETIME

The practical implications of any quantitative model of oxide wearout and breakdown are significant, because oxide reliability is one of the major considerations in device scaling. The difficulty faced by engineers has always been to extrapolate oxide lifetime data from the accelerated stress conditions (high voltage), where data can be collected within a reasonable time, to the lower operating voltage, where the failure rate should be very low. The oxide wearout and breakdown mechanisms change as a function of voltage and oxide thickness (34) so that earlier extrapolations, before this was understood, were easily in error. A controversy still exists over the proper extrapolation from data taken near 2-3 V, to the operating condition at 1 V, (10, 35-37) and this has major implications for reliability projection. This controversy will be reviewed in a forthcoming paper (38). Moreover, for the ultra thin oxides at lower voltages now being employed, a potentially non-destructive "soft" breakdown mode is frequently observed. Thus, the true implications of oxide breakdown for the reliability of integrated circuit products is still unclear. Indeed, microprocessors are already successfully manufactured with sub-2 nm gate oxide (39, 40) without any immediate catastrophic result.

CIRCUIT RELIABILITY

In most circuits, the gate oxides are not connected directly to the power supply. The *n*-FET gates are connected via *p*-FETs, and the *p*-FET gates via *n*-FETs. Figure 6 shows the typical case for an SRAM cell. An increase in gate current after oxide breakdown will cause a voltage drop across the transistor which is driving the gate, diminishing the noise margin of the circuit. The voltage drop will increase as transistors are made narrower, *e.g.* in dense SRAM (cache memory) (41). Rather than focussing on the effect of soft breakdown on individual transistors, it is important therefore to investigate the interaction within a circuit (42, 43). Cache memory occupies a large fraction of the area of many chips and therefore is a useful place to begin an investigation of circuit reliability (44).

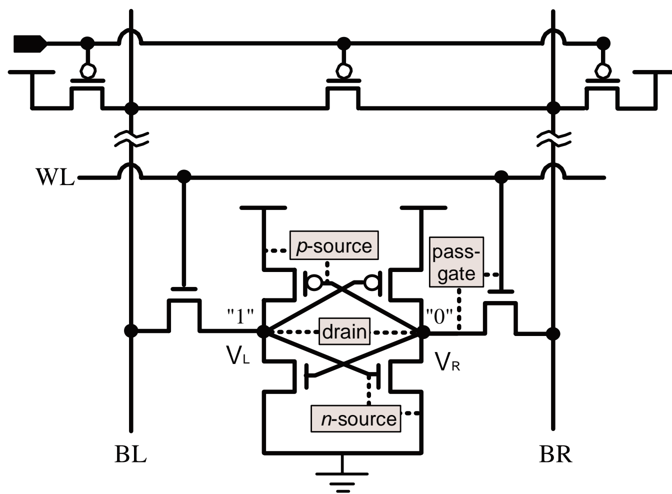

Figure 6. 6-T SRAM cell with possible BD leakage paths corresponding to the cell state shown.

Different circuits may have various degrees of sensitivity to the erosion of noise and voltage margins resulting from oxide breakdown, so more research is needed in order to develop a quantitative methodology for predicting the reliability of circuits. The present oxide reliability methodology will need to evolve from characterizing oxide degradation and breakdown, to the more complex problem of characterizing the response of circuits to oxide breakdown.

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