RC22335 (W0202-031) February 12, 2002
Electrical Engineering

IBM Research Report

The Impact of Gate Oxide Breakdown on SRAM Stability

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ABSTRACT

We have investigated the effects of oxide soft breakdown (SBD) on the stability of CMOS 6T SRAM cells. Gate-to-diffusion leakage currents of 20-50μA at the *n*-FET source can result in a 50% reduction of noise margin. Breakdown at other locations in the cell may be less deleterious depending on n-FET width. This approach gives targets for tolerable values of leakage caused by gate oxide breakdown.

Index terms: Dielectric breakdown, oxide reliability, leakage currents, soft breakdown, hard breakdown, MOS devices, SRAM.

I. INTRODUCTION

It has been argued that oxide breakdown (BD) may limit CMOS scaling [1]. As the thickness of the oxide becomes thinner the Soft Breakdown (SBD) failure mechanism acquires a greater importance in the study of the reliability of the oxide. Until now, the effect of the SBD on the reliability of the oxide has been commonly analyzed on simple capacitors or transistors but very few studies have been done on circuits. However, the necessity to improve the reliability of circuits becomes more and more important and consequently an analysis of the impact of SBD on circuit functionality is required. Oxide reliability models assume that a single BD on a chip will cause circuit failure, but it has been reported that even Hard Breakdown (HBD) does not cause complete failure of some circuits [2].

SRAM was chosen for this investigation because it is a generic circuit (compared to custom logic), and because cache memory may occupy a significant fraction of the chip area. Therefore, by demonstrating that SRAM arrays are relatively insensitive to gate oxide BD, we may realize a significant reliability margin for some chips. Previous work has considered only HBD (ohmic) using 5V technology [3]. In that case, breakdown resistance $\lesssim$1-10kΩ was necessary to degrade cell operation.

In this paper, the effect of SBD on the SRAM functionality is analyzed. One characteristic generally used to evaluate the performance of the SRAM is the cell stability, that is, the ability of the cell to maintain a stable state, and this has been used in this work to study the impact of SBD on the cell operation.

II. DETAILS

Two different CMOS 6T SRAM cells were investigated, using a 0.18μm/1.5V bulk technology [4] and a 0.13μm/1.2V SOI technology [5]. Cell transfer ratios (width ratio of *n*-fet/pass-gate) are approximately 2-2.4. Oxide SBD was modeled as a power law [6] of the form $I=KV^5$ where K reflects the 'size' of the breakdown spot. Fig. 1 shows experimental results supporting this relation. For comparison we also considered ohmic conduction, I=(1/R)V. Only gate-to-diffusion (source or drain) breakdown was considered, since these represent the worst-case situations. Breakdown to the channel can be modeled as a superposition of two gate-diffusion events. For SOI technology, increased gate-body current will affect dynamic operation [7], but was not considered here for static behavior. In order to quantify the cell stability the static noise margin (SNM) was obtained, which is defined as the minimum DC noise voltage necessary to flip the state of the cell. A graphical technique to obtain the SNM consists of drawing and mirroring the transfer curve of the inverters of the cell. The side of the smaller of the two maximum nested squares is a measure of the stability of the cell [8,9]. The higher this value, the better is the stability of the cell. This sort of representation is called the 'butterfly' plot (Fig. 3) and was used in this work to evaluate the cell stability in the presence of BD at various locations in the cell.

III. RESULTS

There are only three topologically distinct breakdown locations in an SRAM cell, denoted drain, *p*-source, and *n*-source in Fig. 2. Breakdown at *p*- or *n*-source is also equivalent to increased source-to-drain leakage (I_{off}) in the opposite *p*- or *n*-FET. Fig. 3 illustrates schematically the effect of HBD at each of these locations. A *p*-source or an *n*-source BD as defined in figure 2 does not affect the transfer curve at the inverter with the *p*-(*n*-)source BD (dotted line in Fig. 3.b and continuous line in

Fig. 3.d respectively). However, the *p*-(*n*-)source BD raises (lowers) the voltage at the output of the opposite inverter (continuous line in Fig. 3.b and dotted line in Fig. 3.d), fighting the channel resistance of the *n*-(*p*-)FET of the inverters without the BD. Consequently, the SNM and therefore the stability of the cell is modified. For fixed R, breakdown at *p*-source has less effect than *n*-source on minimum SNM, because the opposing *n*-FET is stronger (relative to the *p*-FET). Breakdown at drain (equivalent to input-output short) reduces output swing, with the largest effect being to reduce the 'high' state, again because of the weaker *p*-FET.

A cell is most sensitive to noise during a "read" operation. The worst-case scenario occurs in the half-selected state [9], where the word line is pulled high while the bitlines are pre-charged high before the "read" operation. In this case, breakdown at *p*-source is indistinguishable from breakdown at the inverter side of a pass gate. Figs. 4-6 show the SNM in the half-selected state, normalized to the SNM of the cell without BD. For HBD (Fig. 4) the dependence of SNM on R is similar for both technologies. However, for SBD (Fig. 5) there is a significant difference between the two technology generations when compared at the same value of breakdown size K. This is because the somewhat larger V_{dd} for 0.18μm technology results in much greater leakage for the same breakdown spot size. However, when normalized to V_{dd} using an effective SBD resistance $R_{eff} \equiv V_{dd}/(KV_{dd}^5)$, both technologies show essentially identical behavior (Fig. 6). We find that all the BD data can be well described by the relation $SNM=SNM_\infty \times (1-\exp(-[(R_{(eff)}-R_0)/\rho]^\alpha))$ where R_0 is a critical value of the breakdown resistance where SNM=0, and ρ describes the sensitivity to variations in $R_{(eff)}$. For the various cases considered, the parameter α is in the range 0.3-0.6. The physical significance of this stretched exponential form is unknown.

For a fixed value of R for HBD and for a fixed K for SBD it is shown that the worst cell stability has been obtained for the *n*-source BD in both cases (Figs.4-6). However there are differences

between HBD and SBD position for the best cell stability. The higher values of SNM are shown for *p*-source HBD (Fig. 4) while the drain SBD produces the best stability results (Figs. 5 and 6).

For the cells considered in this paper, a 50% degradation in SNM results from oxide BD when the current through the BD spot reaches ~20-50μA at V_{dd} for the worst-case *n*-source breakdown. Pass-gate or *p*-source breakdown may tolerate higher leakage, up to ~500μA, however this value will decrease with *n*-FET width. These values give targets for tolerable values of leakage caused by gate oxide breakdown.

IV. CONCLUSIONS

The effect of gate oxide breakdown on the stability of SRAM cells has been analyzed. Two different technologies (bulk and SOI) have been compared showing similar results. The worst cell stability has been obtained for gate oxide breakdown between gate and source of an NFET of the cell. In this case BD leakage currents of ~20-50μA at V_{dd} produce a reduction of 50% of the SNM. Oxide breakdowns in other positions of the cell of the cell are less significant. These results are indicative of the BD leakage currents that can be allowed for a correct operation of the cells.

ACKNOWLEDGEMENTS

We are grateful for helpful discussions with M. Ketchen, R. Dennard, T. Ning, D. Frank, U. Srinivasan, and D. Plass. R.Rodriguez is funded by a Fulbright Grant and the Ministry of Education, Culture and Sports, Spain.

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FIGURE CAPTIONS

Fig. 1. Experimental SBD curves. Indicated compliance level is breakdown current at stress voltage. Solid lines are power law fits with exponent ranging from 4.6 to 6.1. The current is independent of device area because the BD is a localized spot.

Fig. 2. 6-T SRAM cell with possible BD leakage paths corresponding to the cell state shown. The precharge devices were not present in the cells studied.

Fig. 3. Typical butterfly plots illustrating the effect of breakdown at each location in the cell. HBD, R=40kΩ. SNM is the noise voltage across the cell which causes the transfer characteristics of the inverters to intersect at only one point. Graphically, it is the side of smaller of the two maximum nested squares.

Fig. 4. Normalized SNM for HBD as a function of ohmic breakdown resistance R at various locations in cell. Fitted curves are $SNM=1-\exp(-[(R-R_0)/\rho]^{\alpha})$.

Fig. 5. Normalized SNM for SBD as a function of breakdown size K, at various locations in cell, for two different technologies.

Fig. 6. Normalized SNM for SBD as a function of the effective resistance of the breakdown spot at V_{dd} for two different technologies.

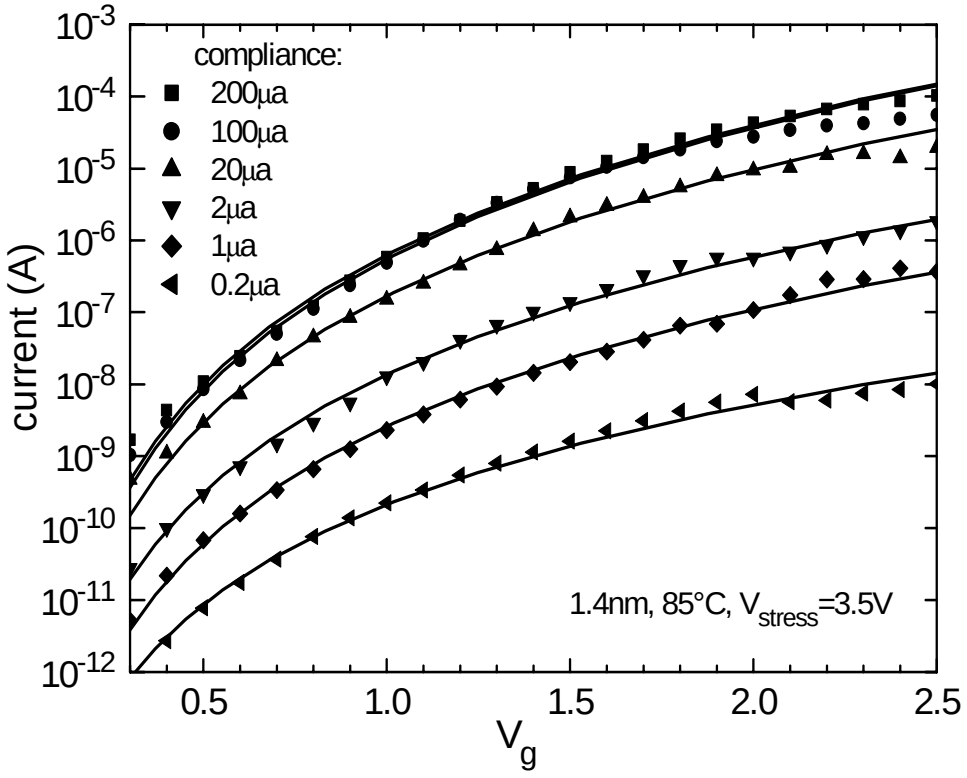

Figure 1

Fig. 1. Experimental SBD curves. Indicated compliance level is breakdown current at stress voltage. Solid lines are power law fits with exponent ranging from 4.6 to 6.1. The current is independent of device area because the BD is a localized spot.

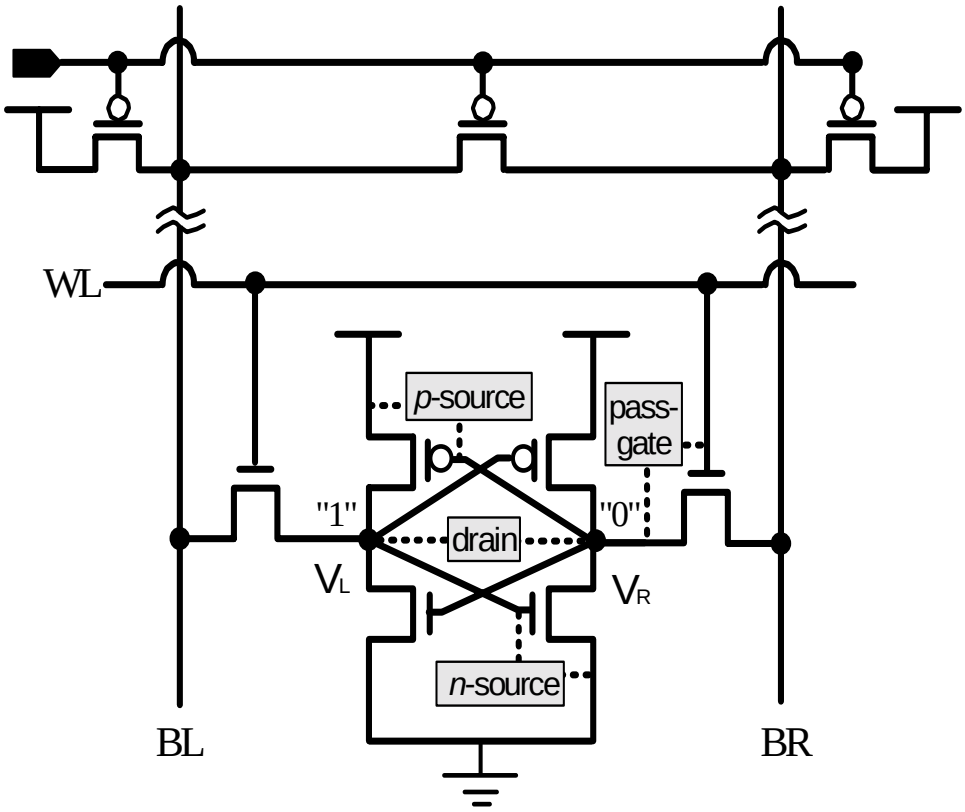

Figure 2

Fig. 2. 6-T SRAM cell with possible BD leakage paths corresponding to the cell state shown. The precharge devices were not present in the cells studied .

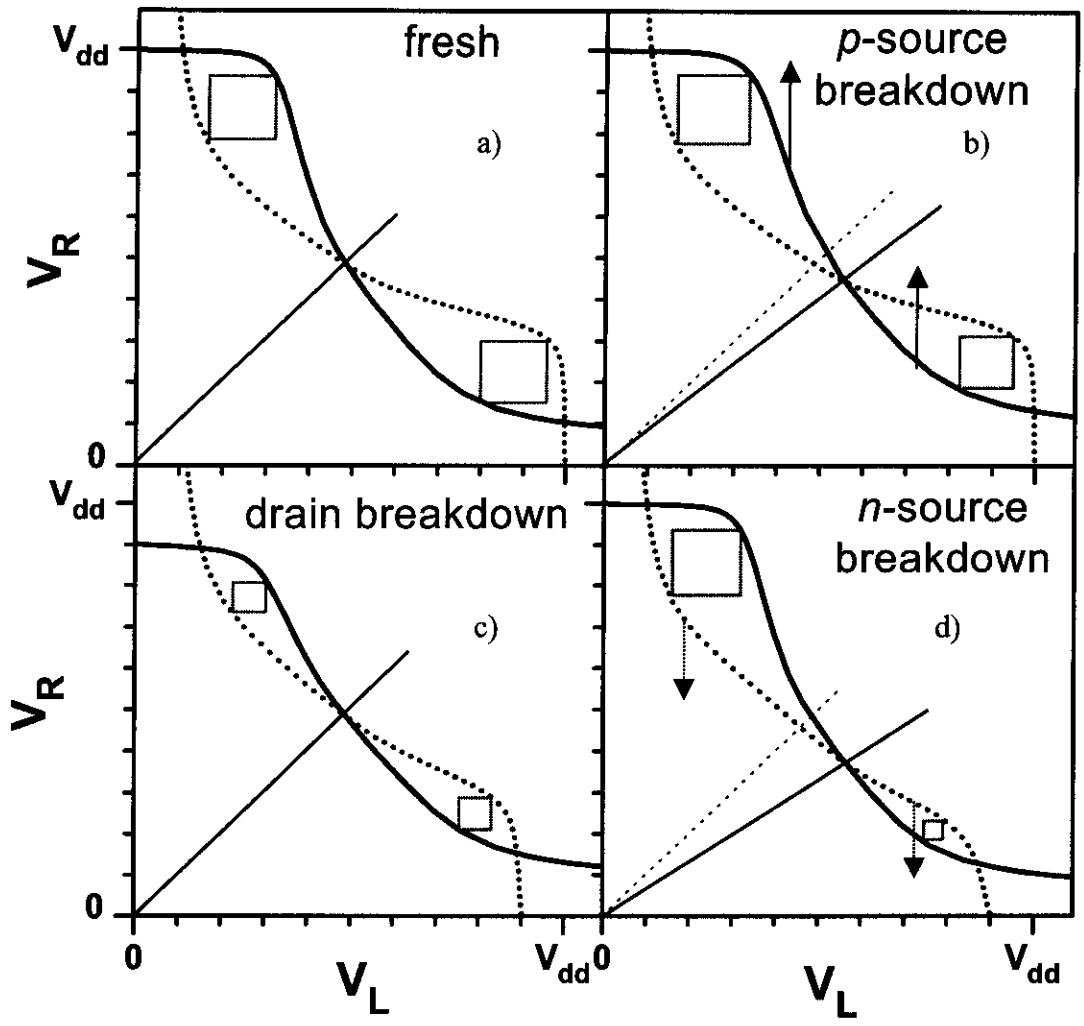

Figure 3

Fig. 3. Typical butterfly plots illustrating the effect of breakdown at each location in the cell. HBD, R=40kΩ. SNM is the noise voltage across the cell which causes the transfer characteristics of the inverters to intersect at only one point. Graphically, it is the side of smaller of the two maximum nested squares.

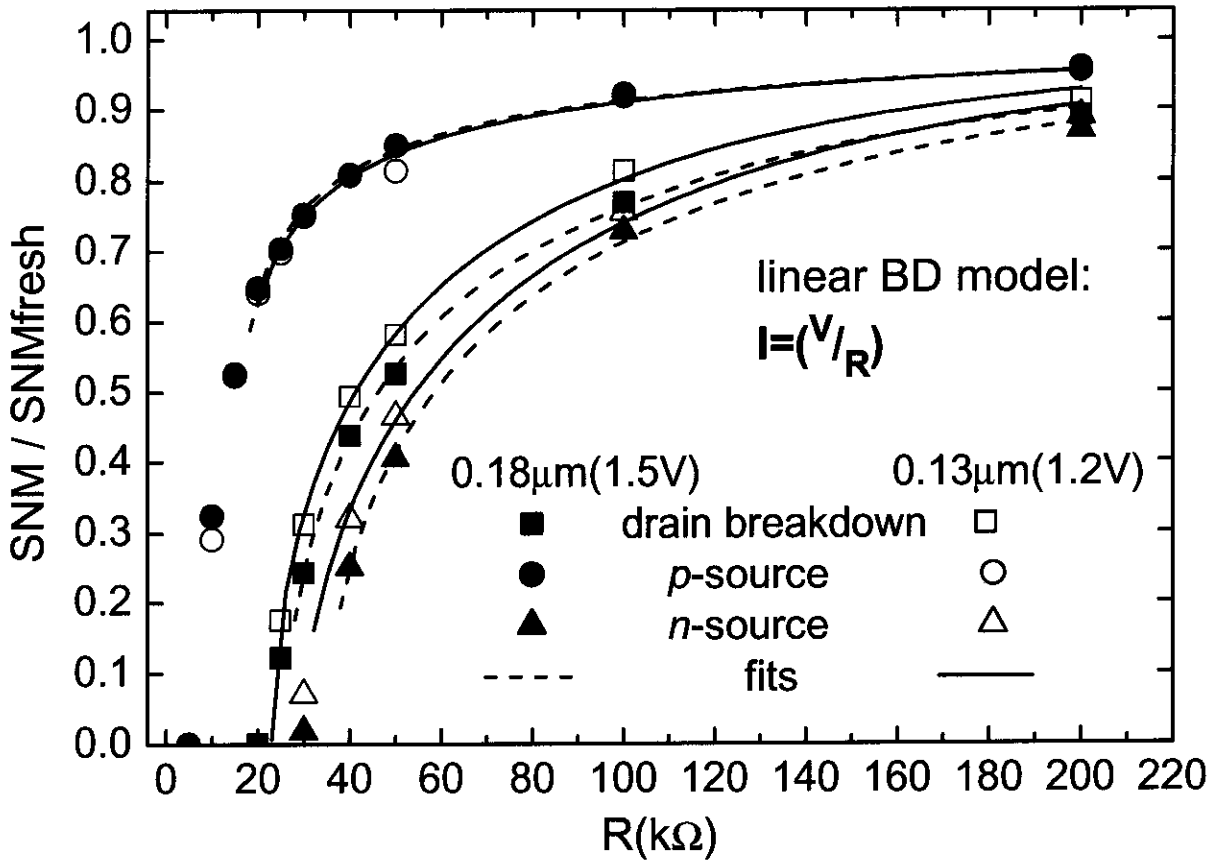

Figure 4

Fig. 4. Normalized SNM for HBD as a function of ohmic breakdown resistance R at various locations in cell. Fitted curves are $SNM=1-\exp(-[(R-R_0)/\rho]^{\alpha})$.

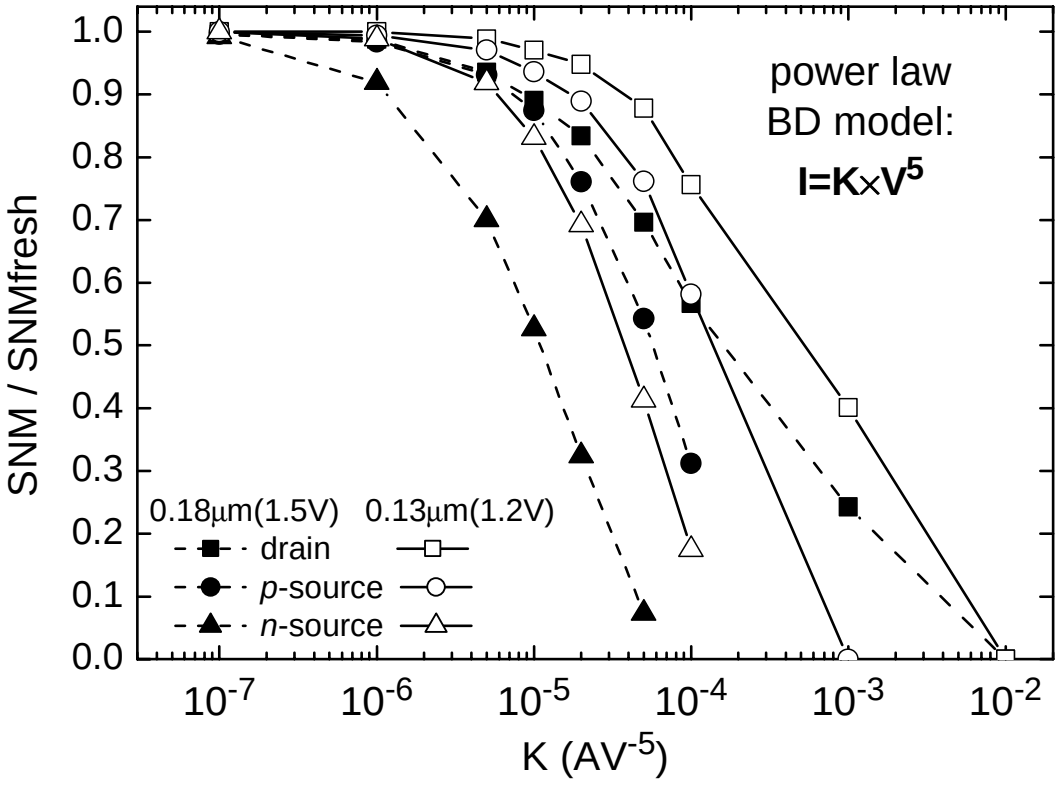

Figure 5

Fig. 5. Normalized SNM for SBD as a function of breakdown size K, at various locations in cell, for two different technologies.

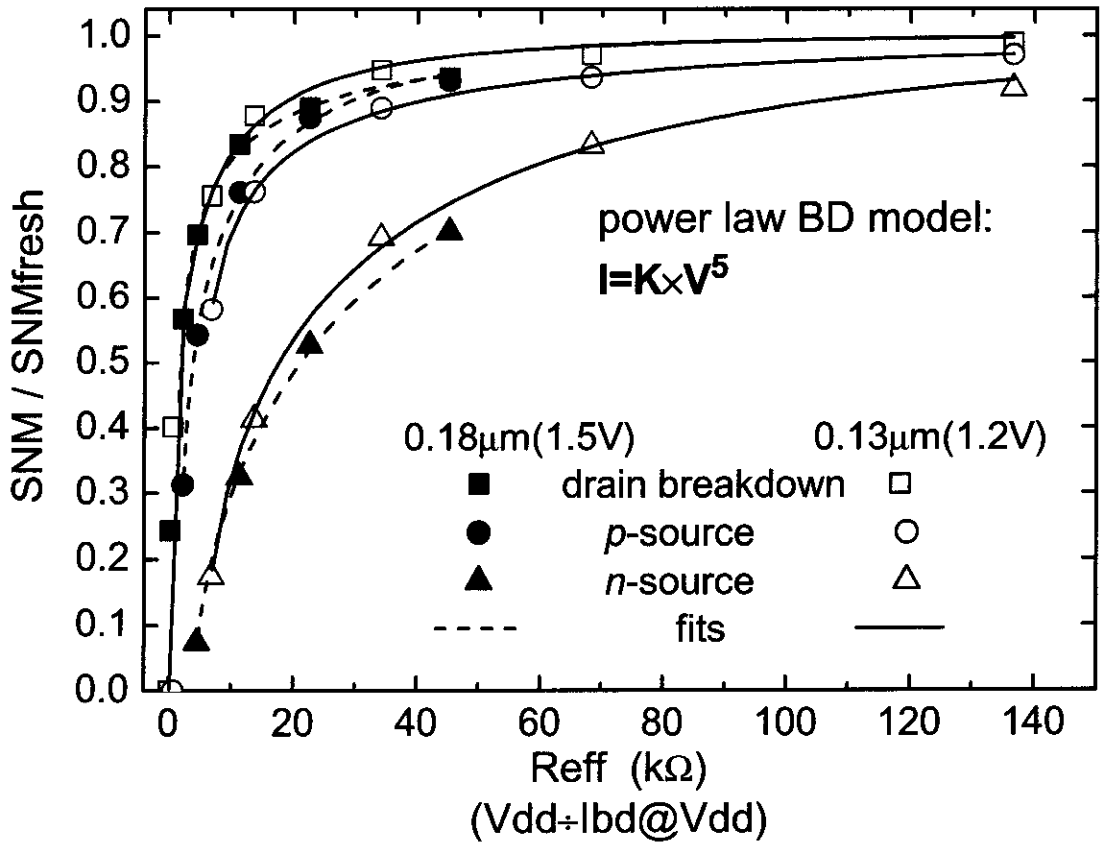

Figure 6

Fig. 6. Normalized SNM for SBD as a function of the effective resistance of the breakdown spot at V_{dd} for two different technologies.