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## Methods for Comparing Contact Hole Shrinking Techniques with 248 nm Single Layer and Bilayer Photoresists

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## Abstract

Several contact hole shrinking techniques have been discussed in the literature recently. Two notable techniques; Resolution Enhancement Lithography Assisted by Chemical Shrink (RELACS™) and Resist Flow Process (RFP) were investigated in conjunction with several commercially available high activation energy chemically amplified materials and one bilayer material. During the course of this study the unique set of advantages along with the inconveniences associated with each technique were explored. It was not only the lithographic attributes of each technique that were of interest, but also characteristics that would effect manufacturability. To that end, experiments were designed so that standard statistical techniques could be employed at the data analysis stage. The attributes of interest were the amount and control of shrinkage, nested and isolated feature bias, process window comparisons, and line edge roughness. It will be shown how several of theses attributes are directly related to manufacturing issues such as lot-to-lot repeatability and linewidth variations across the wafer.

## 1. Introduction

The International Technology Roadmap for Semiconductors[1] indicates that contact sizes in photoresist will be in the 130 to 160 nm range in 2002. To meet these ground rules, there are two potential optical lithography tooling options under consideration. One potential solution is to use 193 nm lithography. Another solution uses 248 nm lithography in conjunction with phase shift masks (PSM) requires imaging below the resolution limit. Several contact hole shrinking techniques[2-5] have come into existence; RELACS™, RFP, CARL™, and Water-Soluble Organic Over-coating Material (WASOOM) to address this need. The basic notion behind all of these techniques is to pattern contact holes at a relatively large dimension where a reasonable process window exists, and then shrink the contacts to a smaller dimension while maintaining the prior exposure latitude and depth of focus. While enabling sub-resolution patterning of contact holes, these techniques come at a cost of increased process complexity, reduced tooling throughput, and increased cost of ownership. Some of these techniques require additional chemical treatments, hence waste disposal issues and chemical compatibility concerns in the process chamber. Related to process quality, the ability to pattern both isolated and nested contacts with a usable common process window is another issue that can be affected by shrinking techniques. On a more positive note, Jeong et al[6] found that line edge roughness in Bilayer resists is reduced by thermal

curing techniques, and data will be presented indicating the same phenomenon using RELACS and RFP.

## 2. Experimental

### 2.1 Materials and Tooling:

All of the photoresists used in this study are commercially available. The single layer resists include Shipley's UV82, UVIIHS, UV110, JSR's M20G and M22G. The Bilayer formulation, EIRIS, used in conjunction with RFP and RELACS can obtained from JSR. The DUV exposures were done on an ASML PAS 5500 stepper with a variable NA from 0.57 to 0.63. Both conventional illumination and annular illumination were available on this tool. Coating took place on a TEL Mark 8 track where the Bilayer materials and single layer materials were plumbed in and automatically dispensed. The R200 Coat material for RELACS was hand dispensed, while the R2 developer was automatically dispensed in the develop bowl. Top down CD-SEM measurements were done on the Applied Materials VeraSEM A, and cross-sectional SEM micrographs were done on a Hitachi S-4000.

### 2.2 Process Conditions:

The RELACS process involves overcoating a completely developed photoresist image with a polymeric solution containing an acid sensitive crosslinking agent. A series of bake steps follow to diffuse acid from the developed photoresist into the overcoat initiating a crosslinking reaction along the resist sidewalls. The uncrosslinked material is then removed during a develop step, and a final bake is performed. The initial RELACS process used in this study was the vendor recommended process, as seen in table 1. An optimized version of this process was developed and evaluated as well.

The RFP technique is less intensive then RELACS with respect to the number of processing steps, additional chemical usage, and to the number of track modules necessary to perform the process. RFP involves adding an extra bake and chill step after the final images are developed. Some experimentation is necessary to find the optimal bake temperature for each photoresist of interest. The optimal bake temperature is a user determined parameter which is based on the desired amount of shrinkage, the bake latitude in that temperature range, the bake time which directly impacts track throughput, the nested to isolated contact shrinkage, and the photoresist profile. In this study 40 nm of shrinkage and a one minute bake time were the desired process attributes.

## 3. Results and Discussion

### 3.1 Evaluation of Shrinkage: Amount, Control, and Change in Profile

While there is a considerable documentation in the literature suggesting that 100 nm of shrinkage is typical for the RELACS process used in conjunction with low activation energy acetal type resists, the areas of interest for this study are high activation energy resists and a Bilayer resist. Previously reported results [7] for several such resists indicating a typical shrinkage range of 35 - 65 nm can be found in table 3. It is known from the literature that the mixing bake is the most

important step in controlling the shrinkage in the RELACS process. In an effort to quantify the effects of the mixing bake on CD, experiments were set up to evaluate the influence of both the time and temperature. The results found in figure 1 for resist A indicate a 2.7 nm/ºC change in shrinkage with temperatures in the 90 to 120ºC range, and a 0.14nm/sec change with time in the area of interest from 30 to 90 seconds. These values are in the same range as the amount of CD change per degree C that most chemically amplified resists exhibit during the post exposure bake step, and are considered acceptable when used in conjunction with state of the art bake plates.

Considering the number of steps in the RELACS process and the shrinkage range of the various resists seen in table 2, an effort was made to simplify the process while increasing shrinkage. In order to optimize the process to maximize shrinkage, the contributions of the remaining process steps were examined and can be seen in table 3. Resist C was chosen for this work because it had shrinkage values that were on the lower end of the range. It was found that resist C shrinkage increased by 2 nm when the soft bakes was eliminated. The 2 nm is probably well within the noise of the measurement technique, but it does indicate that the soft bake is not contributing to shrinkage. Shrinkage was observed to increase by 10 nm when the post develop bake was eliminated. By increasing the mixing bake time from 60 to 90 seconds, eliminating both the mixing bake and the post develop bake, the shrinkage is increased by 14 nm.

The RFP was evaluated using resist F from table 2. The effect of flow bake temperature on CD seen in Figure 2 indicates a 20 nm/ºC change in shrinkage with temperatures in the 164 - 170ºC range and a 1.5 nm/sec change with time at 166ºC from 30 to 90 seconds. Efforts to lower the temperature and increase the time to 90 or 120 seconds while maintaining 40 nm of shrinkage did not improve the bake latitude.

Resist profile changes are inherent in both the RELACS and RFP process. In table 2, the resist profile before and after RELACS processing for both the vendor recommended and optimized process can be seen. Some rounding at the top of the profile takes place during processing, but as shown in a previous study[7], the resist profile doesn't effect the etched contact. For the RFP there are also profile changes upon shrinking. These can be seen for the Bilayer resist in figure 3**,** where the profile of the imaging layer becomes rounded, but the profile after the etch into the underlayer remains vertical.

### 3.2 Contact Hole Process Window and Optical Proximity Effects

An anticipated benefit of contact hole shrinking processes is that one could pattern contacts at a large dimension and shrink them to a much smaller dimension while maintaining the same exposure latitude and depth of focus. To test this hypothesis resist C was patterned to obtain 240 nm nested contacts, using the standard RELACS process the contact size was decreased to 200 nm. The resulting process windows can be seen in figure 4. When analyzing the data a +/- 24 nm specification was used for both samples in order to have a consistent comparison. The results show that the 200 nm process window using RELACS is almost as large as the 240 nm process window from the control as hypothesized. In the case of RFP using resist F patterned to obtain 250 and 210 nm contacts with a +/- 25 nm specification, the process window for the control and the RFP experiment were reasonably similar. The RFP sample had a larger exposure tolerance

but a smaller depth of focus then the control. The smaller depth of focus may be due to profile changes as the focal limits are approached causing the RFP contacts to close up sooner then the control. The larger exposure latitude for nested contacts is consistent with the proximity behavior of the RFP process. As there is less resist between the contacts in the overexposed region compared the underexposed area, the amount of flow decreases enhancing the exposure latitude.

One consideration in the use of any contact hole shrinking process is the effect of processing on the nested to isolated bias, and this was evaluated for both techniques. For the RELACS process, the nested to isolated bias remains unchanged by the shrinking technique. If you have a 45 nm difference between the nested and isolated contacts in your resist, after RELACS processing the CD difference will still be 45 nm which enables one to use the same optical proximity corrections on the single layer resist as with the RELACS processed wafers. This is shown in Figure 5 using resist A. For the RFP process the average shrinkage of nested contacts is 10.8 nm while the isolated contacts had an average shrinkage of 21.5 nm using resist A at a flow temperature of 152 ºC. This trend indicates that optical proximity corrections will need to be reoptimized for wafers processed using RFP.

### 3.3 Line Edge Roughness

Line edge roughness is a concern at the contact hole and via levels because it consumes much of the CD error budget. The ITRS indicates that the CD control requirement post etch for 130 nm contacts is 11 nm. Although it is difficult to measure line edge roughness on contacts, the roughness on 150 nm resist lines is typically in the 5 - 6 nm range. Trends indicate that line edge roughness increases as dimensions decrease. If we estimate that this 5 - 6 nm of roughness found on 150 nm lines is equal to the roughness found in 130 nm contacts, and that roughness transfers from the resist to the etched image, half of the CD error budget will have been used. Jeong [6] indicated that thermal curing after development decreased line edge roughness. In agreement with Jeong's results, it can be seen in figure 6 using resist F, both REF and RELACS are effective in decreasing line edge roughness.

Looking at the images in figure 6 it appears that the RFP and RELACS process significantly decrease line edge roughness. In order to determine if this effect is statistically significant, the line edge roughness was measured along 3 - 5 lines on each sample. The standard deviation of the linewidth is used as the metric for roughness. The data is compared statistically by doing a one-way analysis of variance (ANOVA) for Control Vs RELACS and for control Vs RFP. Results from that analysis indicate that with 99.7% certainty that the RFP line edge roughness is different then the control, and 96.2% confident that the RELACS line edge roughness is different then the control. Results from the two one-way ANOVAs can be found in table 4.

### 3.4 Process Quality Tests

Several tests were performed in order to compare overall process quality before and after the contact shrinking techniques were carried out. One of the initial concerns was that of lot-to-lot repeatability, and this was tested by evaluating at the amount of shrinkage on three separate lots. Each lot consisted of 4 control wafers and 4 wafers processed through the contact shrinking

technique. CD measurements were taken on 13 sites per wafer encompassing areas from the center to the edge of the wafer. A one-way ANOVA was performed on each shrinking technique to determine if the 3 lots had statistically significant amounts of shrinkage variation. The techniques that were evaluated were the RELACS process as defined by the vendor using resist C, the optimized RELACS process without the soft or post develop bake using resist C, and the RFP process using resist F. Results from the analysis can be seen in table 5. Results indicated that the 2 RELACS processes used in conjunction with resist C were repeatable from lot to lot, while the RFP process used in conjunction with resist F was not.

Another aspect of process quality is the CD variation within a wafer. Evaluating the 24 wafers described above, it can be shown that the CD variation of the control wafer and that of the RELACS and optimized RELACS processed wafers were not significantly different as determined through a statistical t-test. Using the same testing procedure the RFP wafers with resist F exhibited a significant difference between the 3 sigma values of the control Vs that of the RFP processed wafers. This can be seen graphically in Figure 7.

In an effort to understand the cause of the lot-to-lot inequalities and the CD variations of the RFP process using resist F, the plot of shrinkage Vs temperature needs to be examined. Figure 2 reveals a 20 nm/ºC change in shrinkage with temperatures in the 164 - 170ºC range. A plot of the average hot plate temperature as a function of time after a wafer has been placed on the plate reveals that the average temperature of the plate varies from 165.28 to 165.66 during a 25 wafer lot as shown in Figure 8. This translates into a 7.6 nm change in CD across the lot. The vendor across plate temperature uniformity specification on the bake station that was used for this work was 2ºC, this translates into a possible 40 nm CD variation across the wafer, and explains why the 3 sigma numbers for this process were higher then the control. To enhance lot-to-lot repeatability and decrease CD variations across the wafer, 1 of 2 things are needed. One is better temperature control on the hot plates, and the second to enhance the process to decrease shrinkage dependency on temperature. Adding small amounts of thermal crosslinkers to the photoresist has been mentioned[2] as a way to control the shrinkage process. If smaller amounts of shrinkage are desired, one can work on a more level part of the shrinkage Vs temperature curve enabling more repeatable results. Resist A where the thermal flow is done at 152 ºC is such an example. With this process the shrinkage on dense contacts is 20 nm, and the dependency of shrinkage on temperature in the 150 to 156 ºC range is approximately 4 nm/ºC.

## 4. Conclusion

As contact hole sizes diminish to 130 nm and below**,** contact shrinking techniques become attractive approaches to realize that requirement. To decide which of the numerous procedures best accomplishes the necessities, a comprehensive comparison is required. It should take into consideration not only the absolute lithographic requirements such as resolution and process window, but also evaluate aspects of the process that may effect manufacturability such as repeatability from lot-to-lot and CD control across the wafer. Even if manufacturing quality tools are not available for the study, simple tests on smaller sample sizes can be performed that are indicative of these attributes.

Results from this comparison indicate that both the RELACS and RFP techniques can be used in conjunction with high activation energy resists to decrease contact hole sizes from 10 to 60 nm. Process windows for the "shrunk" contacts were roughly equivalent to that of the preprocessed contacts. In some cases the nested to isolated contact bias was effected by the shrinking technique, and would need to be addressed through optical proximity corrections on the reticle. Both shrinking techniques reduced line edge roughness, aiding in lowering the total CD error budget for the processes. The RELACS process used in conjunction with resist C showed outstanding repeatability and CD variation control across the wafer. Using RFP that magnitude of control was not found using resist F due primarily to the bake latitude when trying to achieve a 40 nm shrink. Lower levels of shrinkage or tighter control on the bake plate are needed to achieve better process performance.

## 5. Acknowledgments

The authors would like to thank Marie Angelopoulos for management support on this project and Arpan Mahorowala for etch support. Bob Lang's support with Vera SEM measurements is greatly appreciated as was Kelly Garcia's and Rich Owen's work on the SEM cross-sections. Taylor Harris and Jim Brancaccio provided track support for the RELACS process, which was also greatly valued.

## 6. References

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| **Vendor Recommended Process** | **Optimized Process** |
|---|---|
| R200 Coating | R200 Coating |
| Soft Bake 85 C for 70 seconds | |
| Mixing Bake 110 C for 60 seconds | Mixing Bake 110 C for 90 sec |
| R2 Develop, 30 seconds single puddle | R2 Develop, 30 seconds single puddle |
| Post Develop Bake 110 C for 120 seconds | |

Table 1. The RELACS process was performed after the initial wafer patterning and development steps. Both a vendor recommended process and an optimized process were evaluated

| **Resist** | **RELACS Shrinkage** (nm) vendor recommended process | **RELACS Shrinkage** (nm) optimized process | **Resist Flow Process Shrinkage** (nm) |
|---|---|---|---|
| A | 58 | | 10 - 60 nm depending on temperature |
| B | 63 | | |
| C | 44 | 58 | |
| D | 42 | | |
| E | 36 | | |
| F | | 65 | Target was 40 |

Table 2. The amount of shrinkage for contacts using various resists with the vendor recommended RELACS process is compared to an optimized RELACS process and RFP.

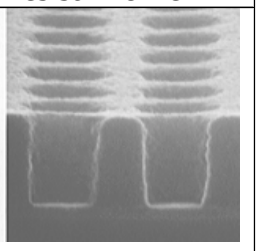
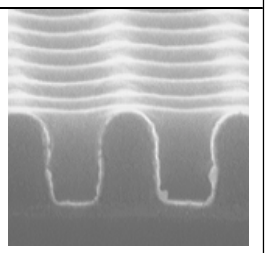
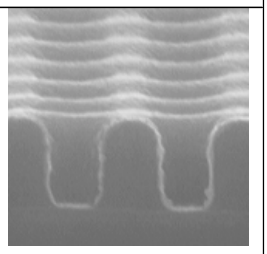
| Experiment | Shrinkage (nm) | Resist Profile |
|---|---|---|
| Control | 0 |  |
| RELACS, vendor recommended process | 43.5 |  |
| No soft bake | 46.5 | |
| No Post Develop Bake | 53.5 | |
| No Soft Bake, No Post Develop Bake, longer mixing bake | 58.7 |  |

Table 3. Optimization of the RELACS process to reduce process steps and increase shrinkage resulted in a 15 nm increase in shrinkage and the elimination of 2 bake steps.

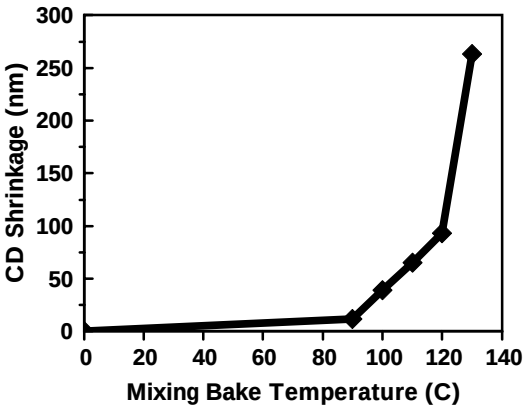
| Data | Mean | F (calculated) | F (critical) | P value |
|---|---|---|---|---|
| Control | 5.2 | | | |
| RELACS | 3.85 | 7.0418 | 5.9874 | 0.3785 |
| RFP | 3.5 | 27.3714 | 6.6079 | 0.0034 |

F (calculated) > F (critical): reject null hypothesis that means are equal
P = 0.3785, 96.2% confident that RELACS is different then the control
p = 0.0034, 99.7% confident that RFP is different then the control

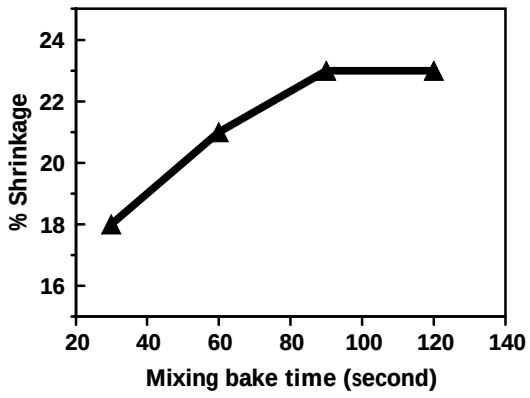
Table 4. A one way analysis of variance was performed to determine if the sample means for line edge roughness were statistically different, and results indicate that they are.

| Process | Lot 1<br><br>Average shrinkage (nm) | Lot 2<br><br>Average shrinkage (nm) | Lot 3<br><br>Average shrinkage (nm) | Means statistically different at 95% confidence level |
|---|---|---|---|---|
| RELACS (vendor process) | 44.55 | 45.05 | 43.8 | No |
| RELACS (optimized) | 58.07 | 58.03 | 61.13 | No |
| RFP | 35.2 | 32.27 | 40.5 | Yes |

Table 5. The RELACS process as defined by the vendor, the optimized RELACS process and the RFP process were tested for lot-to-lot repeatability using resist C. A one-way ANOVA was performed to determine if the amount of shrinkage between lots was statistically significant at the 95% confidence level.

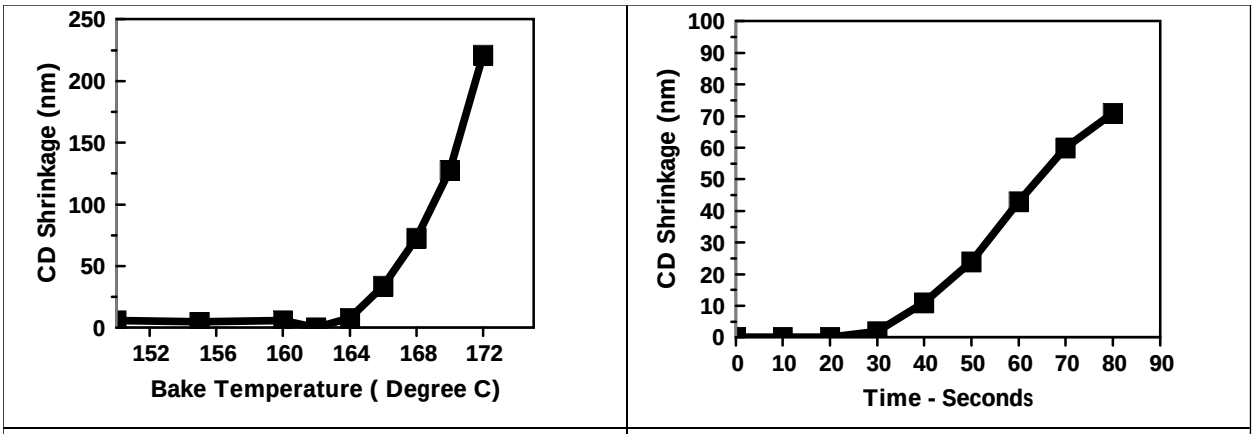



A. Effect of temperature on shrinkage



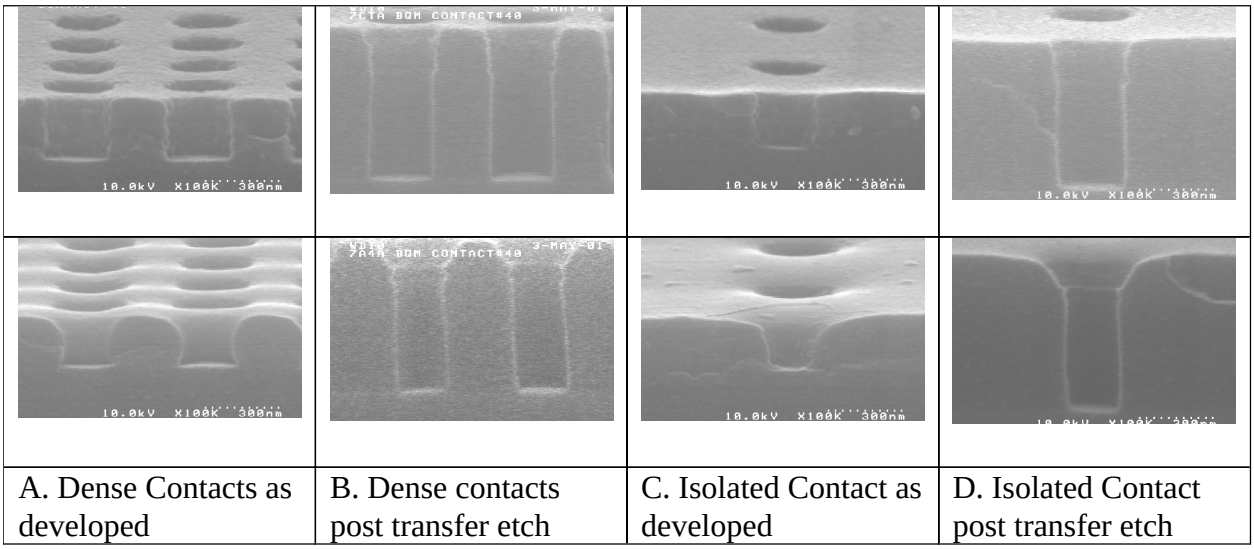

B. Effect of time on shrinkage

Figure 1. On the left is the effect of the RELACS mixing bake temperature on the amount of shrinkage for 250 nm contacts. On the right is the effect of time on the percent of shrinkage for resist B.



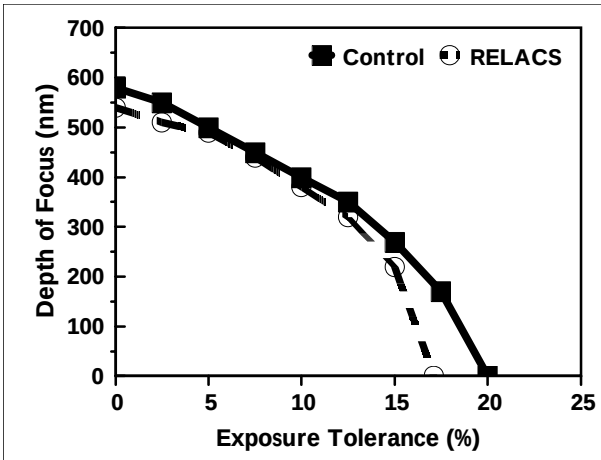

| A. Effect of temperature on shrinkage | B. Effect of time on shrinkage |
|---|---|

Figure 2. On the left is the effect of the RFP bake temperature on the amount of shrinkage for 250 nm contacts. On the right is the effect of time on the amount of shrinkage for resist F.

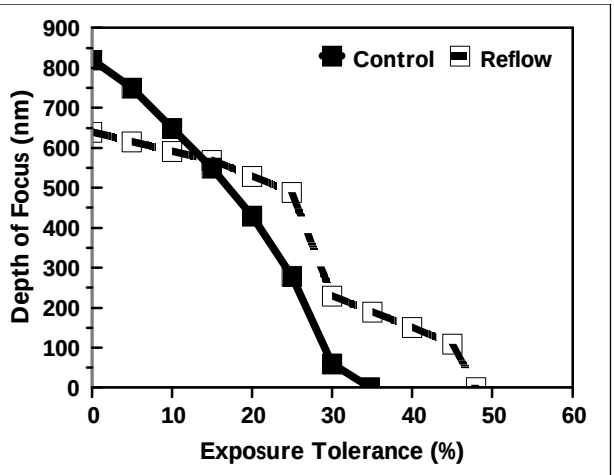


| A. Dense Contacts as developed | B. Dense contacts post transfer etch | C. Isolated Contact as developed | D. Isolated Contact post transfer etch |
|---|---|---|---|

Figure 3. Contact holes using the Bilayer process change profile after RFP, but the profile after the transfer etch into the underlayer remains unaffected.

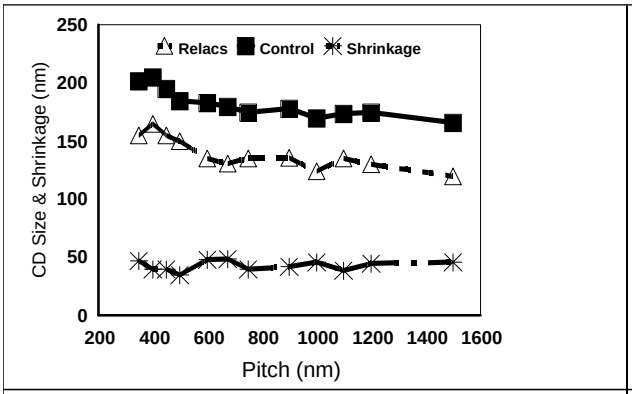



A. RELACS & control process window

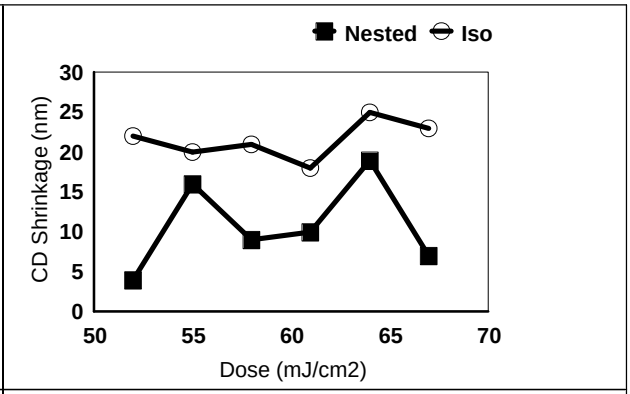



B. RFP and control process window

Figure 4. On the left is the process window for 240 nm contacts compared to the process window for the same contacts after shrinking to 200 nm using the RELACS process using resist C. On the right is a process window comparison using resist F for 250 nm contacts which have been reduced to 210 nm using the RFP.

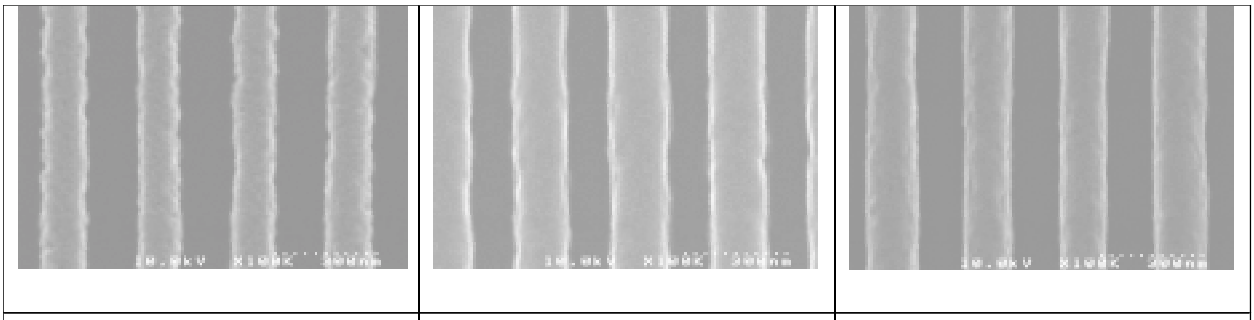



A. RELACS CD and shrinkage through pitch



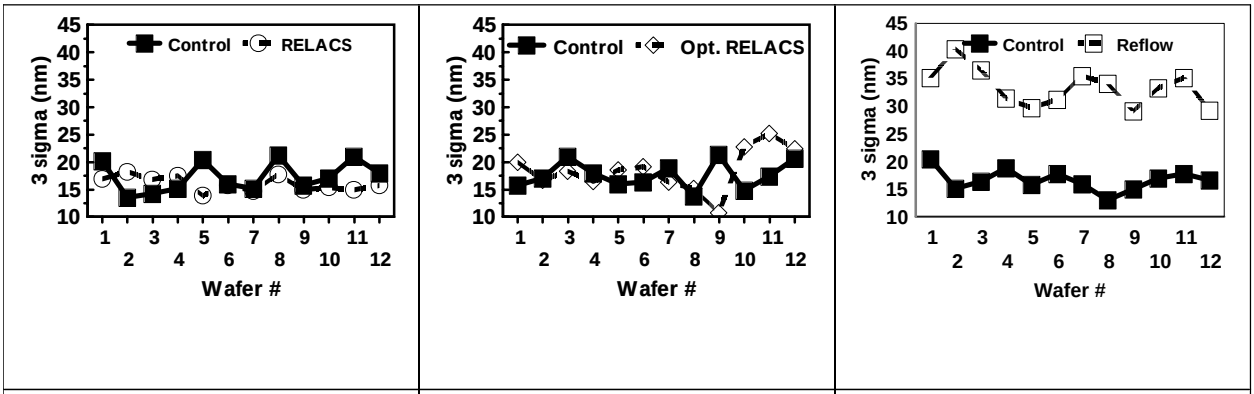

B. Nested & isolated contact CD through dose

Figure 5. The plot on the left compares the contact hole CD through pitch as patterned compared to the results after RELACS processing for resist A and the amount of shrinkage through pitch. The data on the right compares the difference in shrinkage between nested and isolated contacts through dose using resist A at 152 ºC and the RFP process.



| A. As printed: SD = 5.20 nm | B. RELACS: SD = 3.85 nm | C. RFP: SD = 3.50 nm |
|---|---|---|

Figure 6. Lines and spaces designed to be 150 nm were patterned using resist F and post processed using a contact shrinking technique. Figure 5A shows the as printed lines, B exhibits the features after RELACS processing using the vendor recommended process and a mixing bake temperature of 100C, and C demonstrates the effect of RFP at 166 ºC for 1 minute. The standard deviation (SD) is given for each of the 3 processes.




| A. RELACS with resist C | B. Optimized RELACS with resist C | C. RFP with resist F |
|---|---|---|

Figure 7. The 3 sigma CD variation was determined from measurements of 13 sites across each wafer. The amount of variation on the control wafers was compared to that of each shrinking technique. Statistical significance was determined using a t-test. Results indicated that the RELACS and modified RELACS processes did not vary significantly from the control, while those of the RFP process did at a 99% confidence level.

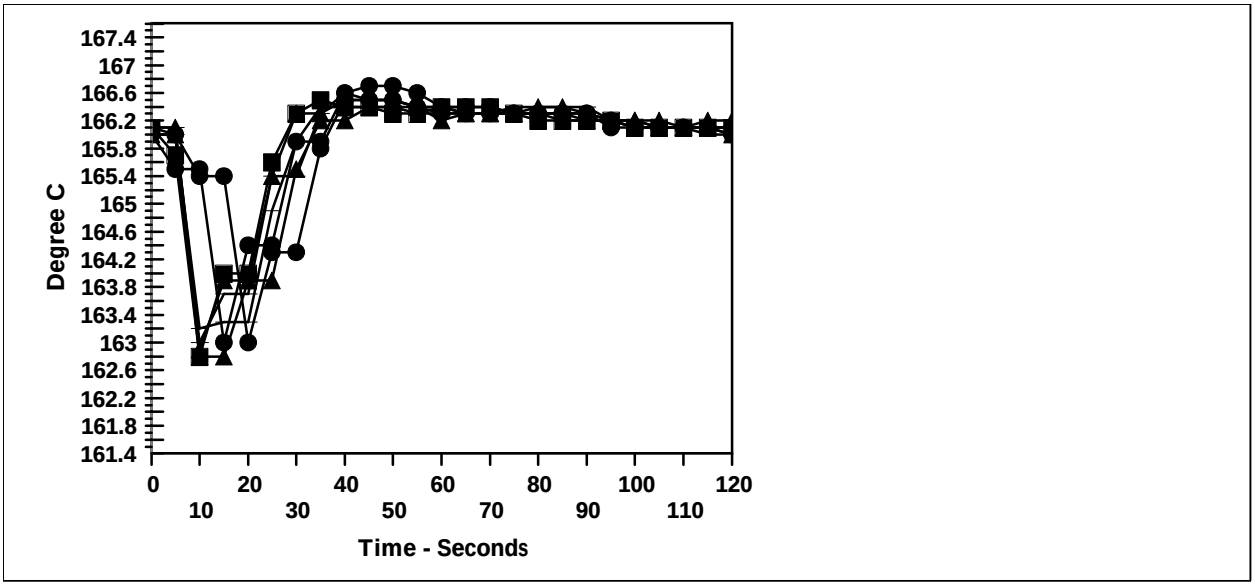



Figure 8. Temperature behavior of the hot plate during a 25 wafer lot. The various curves are from different wafers in the lot. Each data point is an average of 5 sites on the plate. The temperature range for the 25 wafers was 0.38 ºC, which would give a CD range of 7.6 nm. This is a partial explanation for the reproducibility problems using resist F and RFP at 166 ºC for 1 minute. Another aspect of the CD control problem is due to the temperature variation across the plate, which at 166 ºC is specified to be within 2 ºC. This could potentially add another 40 nm of variability.