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Enhanced mobility with an Al_2O_3 gate dielectric grown by MOCVD

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Aluminum oxide films deposited by metal organic chemical vapor deposition (MOCVD) were investigated as a possible high K dielectric for SiO_2 gate replacement in metal-oxide -semiconductor (MOS) devices. The best electrical performance for these devices was achieved when the thin oxide interlayer (< 10Å) on the Si substrate and the Al_2O_3 film were grown in-situ. Electrical measurements on self-aligned poly Si n-FETs show peak mobilities of about 140 cm^2/V-s which are significantly higher (2x) than those reported in previous work[1]. This improvement in mobility is attributed to reduced trapped charge in the gate stack. This charge reduction was also confirmed by capacitance-voltage measurements which shows the hysteric behavior to be reduced. This result is significant because it shows that growth methods have an impact on reducing charge trapping.

Aluminum oxide (Al_2O_3) has been proposed as gate dielectric[1,2,3] material to replace SiO_2 in MOS devices. Al_2O_3 has a dielectric constant K~10 which is about 2.5 times that of SiO_2. These Al_2O_3 films show lower leakage currents, and appear to withstand the high temperature annealing necessary for self-aligned CMOS processing[1,2]. However, self-aligned n-FETs using a poly- -Si/Al_2O_3/Si gate stack have been shown to have reduced performance when compared to SiO_2[1,2,3] . Electron channel peak mobilities were found to be as high as a factor 5 lower than is typically found with an SiO_2 gate stack[1]. In this case, the Al_2O_3 films were deposited by atomic layer deposition (ALD) at temperatures T~ 250-300 ºC on a thin (<10 Å) SiO_2 interlayer.

In this letter, a different approach is used. The Al_2O_3 films were deposited by metal organic chemical vapor deposition (MOCVD) on a thin SiO_2 interfacial layer grown by rapid thermal oxidation (RTO). Aluminum isopropoxide was used as a precursor during the MOCVD process[4]. The RTO/Al_2O_3 deposition sequence was performed in situ. By using this in-situ process sequence, electron peak mobilities were found to increase by a factor 2 when compared with an ALD/RTO or a MOCVD process which was done ex-situ.

This increase in peak mobility may be correlated to the high frequency CV measurement which showed reduced charge trapping when compared to previous processes. This is a significant result since it implies that the trapped charged in the Al_2O_3/RTO/Si stack can be reduced by controlling the process sequence.

Using a conventional self-aligned poly Si process n-FETs were fabricated. The source/drain implant anneal was done by rapid thermal annealing (RTA) at 1000 ºC. In general, device integration was similar to the one reported by Buchanan et. al.[1] but here the Al_2O_3 was deposited by MOCVD. The RTO and Al_2O_3 growth sequence was carried out in-situ. Al_2O_3 deposition rates were about 3A/min.

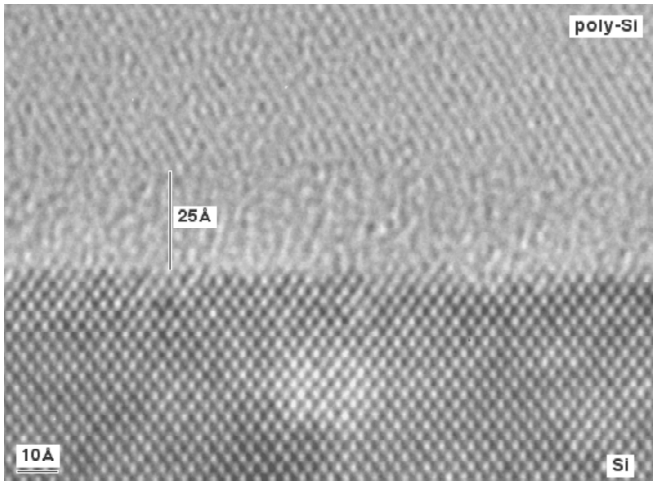

Fig. 1 High resolution TEM of the poly Si/RTO/Al2O3 gate stack.

High resolution transmission electron micrscopy (TEM) at 200kV was used to analyze the interfacial microstructure of Al_2O_3 gate stack. The lattice image in Fig. 1 was taken along [110] zone axis of Si. The dark spots in the image correspond to dumbbells of Si atoms in (110) projection. Figure 1 also shows a thickness of ~ 25Å for the RTO/Al_2O_3 layer which appears uniform along Si surface. The RTO and Al_2O_3 layers can not be resolved in the image due to the fact that both materials have similar electron scattering factors limiting the contrast.

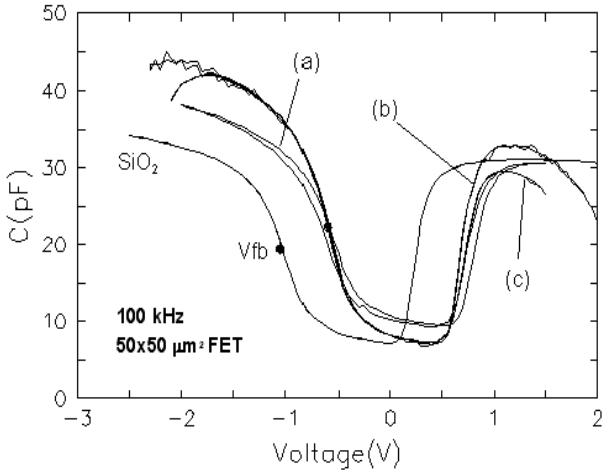

Fig. 2 High frequency CV of 50x50 μm² n-FETs. (a) RTO and Al_2O_3 grown in-situ, (b) RTO and Al_2O_3 grown ex-situ (5 min deposition), (c) same as (b) but 3 min Al_2O_3 deposition.

The 100KHz high- frequency capacitance-voltage (CV) characteristics of 50x50 μm² FETs for different gate stack processes are shown in Fig. 2. Curve (a) is the standard process where the RTO and the MOCVD Al_2O_3 are grown ex-situ. Note that a large hysterisis, of ~ 70mV, is present on both the accumulation and the inversion side. This large hysterisis is also found in FETs fabricated using ALD Al_2O_3[1].

On the contrary, when the RTO and MOCVD Al_2O_3 stack was grown in-situ, the high frequency CV shows a much reduced hysterisis of ~5mV on the inversion side and 12mV on the accumulation side (curve (b) and (c)). The devices were driven to a high voltage to induce charge in the oxide, From the accumulation side an equivalent oxide thickness *Tqm~13Å* was obtained by using a quantum mechanical simulator reported in Ref. 5.

Deposition time for curve (b) was 5 min which should yield an Al_2O_3 thickness of about 15*Å*. Curve (c) shows that by decreasing the Al_2O_3 thickness to 9*Å* using a 3 min deposition time there is no reduction in *Tqm* or *Tinv*. On the inversion side a significant poly depletion is seen which is more pronounced for the thinner film. Using a classical approximation, inversion thickness are found to be *Tinv~26Å* for curve (b) and *~29Å* for curve (c). It appears that the poly/Al_2O_3 interface is still key for obtaining lower *Tinv*. By modifing the poly silicon deposition process, a more stable interface may be achieved which could produce a lower *Tinv*[6].

Flat band voltages V_b ~ *-1.6V* for the Al_2O_3 capacitors are also indicated in Fig. 2. For a polysilicon process flat band voltage shifts should be ~ *-1V* as shown by the SiO_2 control wafer. Since both the in-situ and ex-situ RTO/Al_2O_3 processes give the same shift, it is likely that the poly interface may play a role in pinning the flat band voltage since the poly process was the same for both samples. This significant shift also is responsible for the large V_t shift of the FETs.

By plotting the drain current I_{ds} vs the gate voltage V_g, the threshold voltage was *~0.63V* for the Al_2O_3 and *0.21V* for the SiO_2 FETs, respectively, as shown in Fig. 3b. This is consistent with the large shift (~ 400 mV) observed on high frequency characteristics on the inversion side between the SiO_2 control and the Al_2O_3 gated FET of Fig. 2. Figure 3a shows the source drain current I_{ds} as a function of the gate voltage V_g on a log scale. Field effect transistor dimensions are 0.4x20 μm². The subthreshold slopes are about 75 mV/dec for both the SiO_2 and Al_2O_3 FETs.

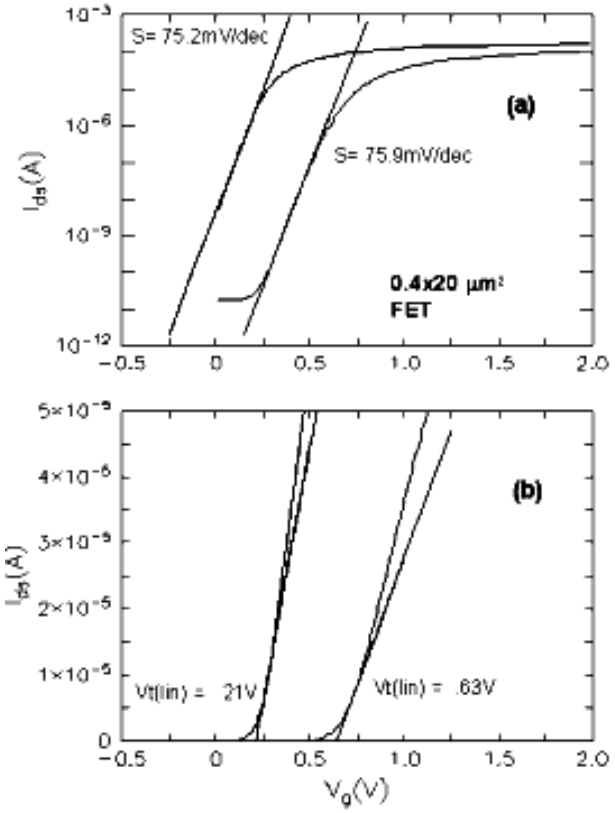

Fig. 3 Comparison between I_{ds} vs V_g for n-FET using MOCVD Al_2O_3 and SiO_2. (a) log scale, (b) linear scale.

Mobilities as a function of effective field for the processes shown in Fig. 2 and described earlier, are shown in Fig. 4. The peak mobility for the ex-situ process is about *70 cm²/V-s* which agrees with previous work with ALD Al_2O_3 films[1]. A significant improvement in mobility ~ 2X is obtained when the in-situ processing is performed. This data is consistent with the reduced trapped charged found from the high frequency CV characteristics.

Fig. 5 shows the flat band voltage shift (ΔVfb) as a function of stressing time at a stress voltage of 1.5 V. In order to measure the ΔVfb a series of voltage pulses were applied at the gate. Between each stress pulse, capacitance versus voltage curve was measured to estimate the flat band voltage shift. To ensure that ΔVfb occurs only due to the stress

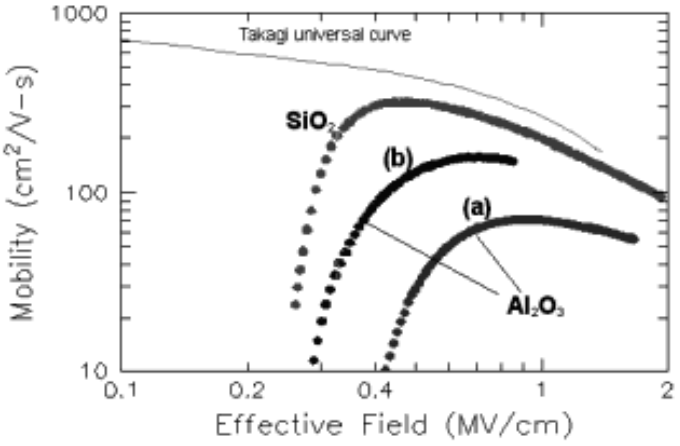

Fig . 4 Mobility of MOCVD Al_2O_3 gated n-FET. (a) substrate allowed to cool between RTO andAl_2O_3 growth, (b) no cooling between RTO and Al_2O_3 growth. SiO_2 control and Takagi universal curve are also plotted.

voltage pulse, C-V was performed over a limited voltage range. As the gate dielectric films were stressed, some of the injected electrons were trapped in the gate dielectric films thereby causing a shift in the ΔVfb. The shift in the flat band voltage is linearly dependent on the trapped charge density (Nt) : $Nt = (\Delta Vfb^* d) / k\varepsilon_o$, where eo is the permittivity of the free space, k is the dielectric constant and d is the centroid of trapped charge density. In Fig. 5 , the in-situ film shows

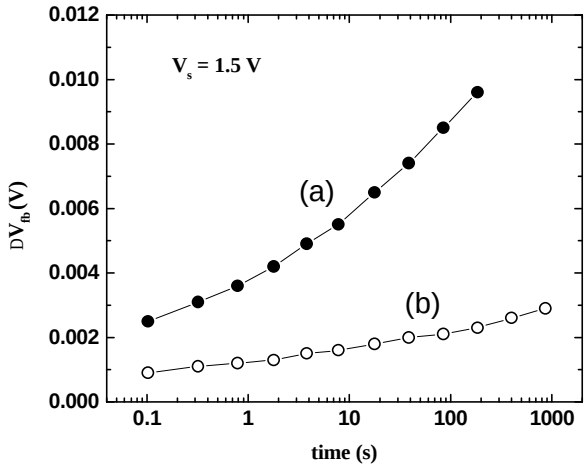

Fig. 5. Flatband voltage vs time using a stress voltage of 1.5V. (a) RTO and Al_2O_3 grown ex-situ, (b) grown in situ .

smaller flat band shift in comparison to ex-situ films thereby indicating that charge trapping is reduced significantly in in-situ films.

Still, these mobilities are far below the SiO_2 values of about *400 cm^2/V-s*. Reducing trapped charges to the level of SiO_2 is still a big challenge. However, this work demonstrates that by using a different approach to processing some improvement can be achieved. Still, the top interface poly/high-K appears to be the most crucial due to the large poly depletion. To form stable poly/high-K interfaces alternative poly processing needs to be investigated.

In summary, Al_2O_3 films deposited by MOCVD produced lower trapped charges than films deposited by ALD. This was achieved by using an in-situ process between the RTO and the Al_2O_3 depositions. Higher mobilities in Al_2O_3 FETs were observed when this process was used. When an ex-situ process was performed lower mobilities were measured. However, the reduction in trapped charge did not affect the flat band voltage which appear to be pinned around *-0.6V* for both processes. Also, a large poly depletion was observed for both in- and ex-situ processing. This may indicate that the poly Si/Al2O3 interface is partly responsible for the reduced electrical performance.

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