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Integration of self-assembled diblock copolymers for applications in microelectronics

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Integration of self-assembled diblock copolymers for applications in microelectronics

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Integration of new materials into semiconductor technology has become ever more important in the quest for continued performance improvements in microelectronics. For example, the introduction of copper wiring and low-k dielectric materials into back-end silicon processing has enabled microprocessors which operate above gigahertz frequencies. New giant magnetoresistive (GMR) materials for magnetic disc read-heads are pushing storage densities above 100 Gb/in^2. Chemically-amplified polymer resists have aided in improving photolithographic resolutions to 100 nanometer (nm) dimensions. Introducing each of these materials into "conventional" silicon processing has involved both large efforts to ensure compatibility with the established technology, and also development of reproducible processes for building with the new materials.

Nanometer-scale self assembly has become a popular concept for structuring materials and devices on sub-lithographic (i.e., sub-100 nm) length scales. Of the many different ideas for utilizing self-assembly, only a fraction are suitable for application in microelectronics because of stringent material restrictions for integration with semiconductor manufacturing. Any self-assembly process should add functionality to silicon-based electronics but cannot add significant cost or complexity. The new process must also be reliable, scalable to large silicon wafer sizes (currently 200 mm diameter and soon increasing to 300 mm), and amenable to batch wafer processing.

1. Polymer Thin Film Self Assembly

Self-organizing diblock copolymer thin films are interesting materials because they meet many of these requirements for application to microelectronics. Because diblock copolymer thin films have been previously demonstrated to self assemble with

characteristic dimensions on the order of 10-20 nm, they may find uses in structuring materials and devices at dimensions below photolithographic resolution. Furthermore, the polymer films can be spin cast from a solvent and thus the assembly process is performed over large sample areas. Finally, suitable selection of the polymer materials ensures their compatibility with semiconductor fabrication processes. This discussion focuses on the integration of diblock copolymer films composed of polystyrene-poly(methyl-methacrylate) (PS-PMMA), and the development of reproducible processes for building more complicated structures using these self-assembled thin films.

1.1 Similarity to Photolithography

One appealing aspect of the diblock copolymer thin film assembly process is its similarity to conventional photolithography using a polymer resist. Beginning with the substrate to be patterned, the polymer material (either a standard photoresist or the diblock copolymer) is first applied to the surface by spin casting [see Figures 1(a) and 1(b)]. In photolithography, the polymer resist is illuminated by ultraviolet light which is passed through a mask in order to define the pattern [Figure 1(a)]. Pattern formation in a diblock copolymer film is achieved by self assembly – the substrate is heated in order to facilitate microphase separation of the two constituent polymer blocks [Figure 1(b)]. Finally, in each case a relief image is formed in the film by immersing the substrate in a chemical developer which removes the polymer film from specific areas. Microphase separation of the polymer blocks occurs on a scale determined by the length of the polymer chains, thus enabling pattern formation on a 10-20 nm length scale using diblock copolymer self assembly, albeit with only a limited type of pattern. In contrast,

photolithography allows an arbitrary pattern to be printed on a surface, however the length scale is limited by optical diffraction.

1.2 Polymer Self Assembly Process

The details of the technique for forming diblock copolymer thin films have been previously described several times (Black *et al.* 2001, Thurn-Albrecht *et al.* 2000, Mansky *et al*. 1996, Harrison *et al.* 1998, Park *et al.* 1997), and only a summary of the PS:PMMA assembly process is given here. Following a surface pretreatment with a random copolymer (Mansky *et al.* 1998) in order to neutralize the substrate to the two polymer blocks, a solution of PS-PMMA diblock copolymer (70:30 PS:PMMA molecular weight ratio) dissolved in toluene is spin cast onto the surface. Annealing the film facilitates polymer self assembly into nanometer-scale hexagonal domains. A porous PS film is generated by developing in acetic acid. Scanning electron microscope (SEM) images of a diblock copolymer thin film (after PMMA removal) show characteristic hexagonally-arranged nm-scale pores extending through the thickness of the film [Figures 2(a-c)]. Under optimal processing conditions, it is possible to create films with narrow pore size distributions of 10% (Guarini *et al.* 2002). Cross-sectional views of the sample show a PS film thickness on the order of 30 nm [Figure 2(b,c)], which is thin compared to conventional photoresists which are typically closer to 500 nm in thickness.

1.3 Thickness Dependence of Polymer Self-Assembly

For applications in microelectronics, the self-assembled polymer film will most often serve as a template for pattern transfer into an underlying film or substrate. In these cases it is advantageous to form self-assembled domains in the thickest possible PS film, because the depth to which the pattern can be transferred will be limited in some manner

by the thickness of the polymer mask. Yet the polymer thickness plays a large role in determining film morphology, limiting the achievable thickness of well-ordered templates (Guarini *et al.* 2001, 2002). Figure 3 shows a series of images illustrating the change in film morphology as a function of increasing film thickness. For films 33 nm and below, the template is characterized by nonuniform coverage of irregularly-shaped pores. As the film thickness increases, both the density and uniformity of the nm-scale pores improve, and reach a minimum ~10% variation in pore diameter with ~20% variation in pore separation for optimal film thickness (in this case between ~35-45 nm thick, for 64 kG/mol polymer moleular weight). Films thicker than 45 nm begin to show extended one-dimensional pore structures, which are generally described as cylinders lying parallel to the substrate. As demonstrated in the figure, there is clearly a narrow window of optimum film thickness for high-quality self-assembled films (~35-45 nm).

2. Nanometer-Scale Pattern Transfer Using Reactive Ion Etching

The ability to reproducibly form porous PS films of the type shown in Figure 2 is only a starting point in terms of applying these materials to microelectronics. While meeting the criteria of compatibility, scalability, and suitability for batch wafer processing, the polymer films are best suited to act as templates for transfer of the nanometer-scale patterns into underlying materials (similar to conventional photoresists) because they are neither mechanically robust nor thermally stable. Device applications of these porous PS films therefore require development of a set of integrated pattern transfer processes.

2.1 Low-Aspect-Ratio Etching with a Polymer Mask

Nanostructured diblock copolymer films have previously been used as masks for reactive ion etch (RIE) pattern transfer into a substrate (Harrison *et al.* 1998, Cheng *et al*. 2001, Black *et al.* 2001, Guarini *et al.* 2001). Such processes are essential for any type of device application, as in the fabrication of metal-oxide-semiconductor (MOS) capacitors with nanotextured silicon electrodes (Black *et al.* 2001). For etching low-aspect-ratio features [i.e., etching to a depth on the order of the polymer film thickness (30-40 nm)], the polymer film provides an adequate mask [Figure 4(a,b)]. Figure 4(d) shows a 70 degree tilted SEM image of a silicon surface which has been lightly pitted using a SF_6-based plasma chemistry. The visible textured silicon surface in the lower portion of the image illustrates that the hexagonal pattern is faithfully reproduced in the etched substrate. The top portion of the image shows the remaining PS mask, which can be optionally removed at this stage using an O_2 plasma strip [Figure 4(c)]. The PS holds up well under SF_6 etching, with an etch selectivity of roughly 25:1 for silicon to PS in blanket films. The silicon etch rate in the nanopores is significantly reduced from this blanket etch rate however, and since SF_6 is a relatively isotropic silicon etch this process is limited to patterning low-aspect-ratio features.

2.2 Pattern Transfer into a Dielectric Hardmask

In order to produce more deeply-etched structures in silicon, it is advantageous to first transfer the polymer pattern into a more robust etch mask material such as silicon dioxide (SiO_2) (Guarini *et al*. 2002). This is accomplished by first forming a nanoporous PS thin film on a silicon wafer onto which 20 nm of silicon dioxide has been grown [Figure 5(a)]. The polymer template pattern is transferred into the SiO_2 using RIE [Figure 5(b)]. After PS removal by an O_2 plasma strip [Figure 5(c)], the nanostructured

template pattern is reproduced in the SiO_2 layer [Figure 5(d)]. Comparison of pore dimensions and uniformity in the initial polymer template and the final oxide hardmask shows that the pattern is transferred with a high degree of fidelity. In addition, the RIE step can provide a means for adjusting the template dimensions, since the oxide RIE proceeds laterally (thus widening the pores without changing pore position or spacing) after reaching the underlying silicon.

2.3 Anisotropic Silicon Etching

The dielectric hard mask into which the nanoscale pattern has been etched can subsequently be used for further transfer into the silicon, for example with an anisotropic HBr-based etch gas chemistry developed for transistor gate etching (Guarini *et al.* 2002). This technique has been used to produce dense nanopores in silicon with aspect ratios as large as 10:1 [Figure 6(a,b)]. The etch recipe produces nearly vertical sidewalls, which is essential given the high nanopore density. Any lateral etching at these dimensions would result in merging of adjacent nanopores. The final pore depth can be varied (without producing appreciable changes in the etched pore diameter) by merely adjusting the etch time.

3. Nanometer-Scale Pattern Transfer by Metal Liftoff

For other applications it is desirable to nanostructure surfaces by *adding* material to a substrate, rather than by the *subtractive* etching processes described above. There have been several demonstrations using diblock copolymer thin films as templates for metal deposition using electroplating (Thurn-Albrecht *et al.* 2001) or physical vapor deposition (Black *et al.* 2002, Guarini *et al.* 2001, Park *et al.* 2001). This discussion

outlines a general liftoff process for producing close-packed nanoparticle arrays of a wide variety of materials.

This extremely versatile technique can be used to nanostructure any material that can be directionally deposited. The substrate to be patterned is first coated with a nanoporous PS template (Figure 2). A brief O_2 RIE is used to clean out the pore bottoms and promote metal adhesion to the substrate. The substrate is then blanket coated with a thin film of the desired nanoparticle material by electron-beam evaporation. Finally, the PS template is dissolved in 1-methyl-2-pyrrolidone (NMP) heated to 120 °C under ultrasonic agitation, thereby lifting off the evaporated material that deposited on top of the polymer template. The top-view SEM image of the final structure shows a hexagonal close-packed dot array with dimensions similar to the beginning PS template (~21 nm dot diameter with 42 nm interdot spacing) (Figure 7).

4. Concluding Remarks

Diblock copolymer thin films meet many of the requirements for integration into semiconductor processing. Their ability to self-assemble into uniform domains at sub-lithographic dimensions provides an opportunity to add functionality to microelectronics without adding significant cost or complexity. These materials can be used in the same manner as conventional photoresists, that is, as sacrificial templates for pattern transfer into inorganic materials by RIE or metallization. In this way, self-assembled diblock copolymer thin films have potential use for nanometer-scale patterning in the fabrication of highly complex silicon devices.

FIGURE CAPTIONS

FIGURE 1. Schematic representations of (a) photolithography process and (b) self-assembly process. (a) Patterning with photoresist is performed by spin-casting resist on a substrate, exposure with UV light, and immersion in a chemical developer (b) Diblock copolymer patterning is performed by spin-casting polymer on a substrate, self-assembly via heat treatment, and immersion in a chemical developer.

FIGURE 2. SEM images of a porous PS template after removal of PMMA block. (a) Top-down view of close-packed hexagonal array. (b) Image taken at a 70 degree tilt showing template pore radius 15 nm and center-to-center distance d=45 nm. (c) Cross-sectional view showing that the pores extend down to the silicon surface. Template thickness is 30 nm.

FIGURE 3 (online version). Evolution of diblock copolymer film morphology with changing thickness (Quicktime Movie).

FIGURE 3 (print version). SEM images porous PS films of increasing thickness. (a) 33 nm (b) 45 nm (c) 52 nm.

FIGURE 4. RIE using self-assembled polymer mask. (a) Polymer template formation on silicon surface. (b) RIE pattern transfer of PS template into silicon. (c) Removal of the PS matrix. (d) SEM image at a 70 degree tilt after RIE. Top shows remaining PS template. Bottom shows hexagonal array has been transferred into Si substrate.

FIGURE 5. RIE transfer of self-assembled pattern from polymer film into dielectric hardmask. (a) Polymer template formation on oxide surface. (b) Oxide RIE down to silicon substrate. (c) PS removal. (d) SEM image of nanometer-scale pattern transferred into SiO_2 film.

FIGURE 6. Anisotropic silicon RIE. (a) 70 degree tilt SEM images showing porous silicon substrate. (b) Cross-sectional SEM image shows vertical etch profile.

FIGURE 7. (a) Metal dot array formed by liftoff technique with self-assembled polymer mask. (b) Metal nanoparticle dimensions and uniformity correlate with those of initial polymer template.

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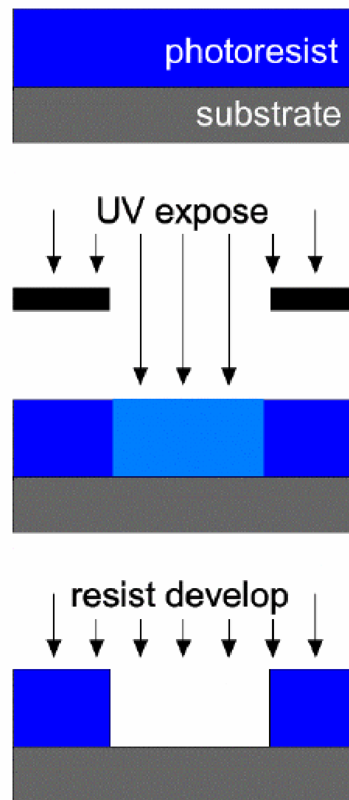

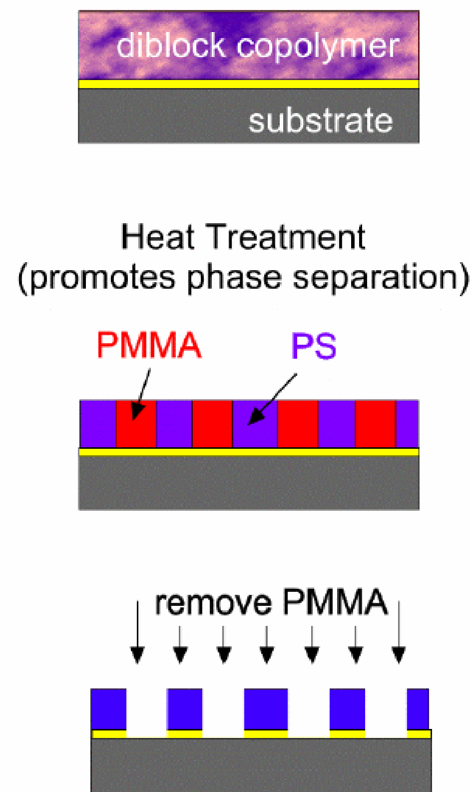

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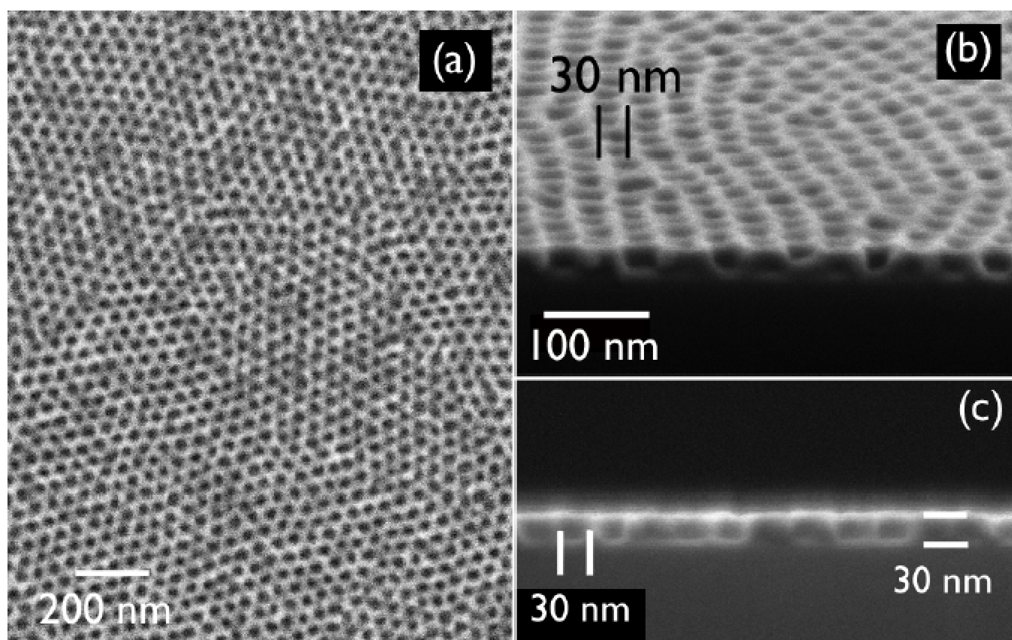

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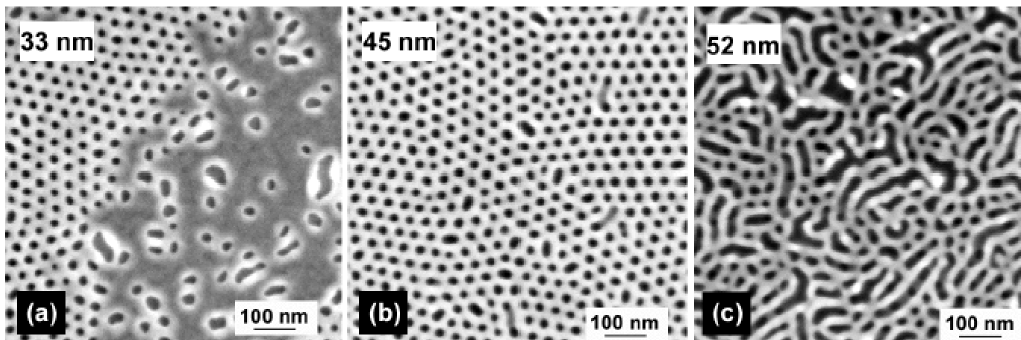
FIGURE 2. SEM images of a porous PS template after removal of PMMA block. (a) Top-down view of close-packed hexagonal array. (b) Image taken at a 70 degree tilt showing template pore radius 15 nm and center-to-center distance d=45 nm. (c) Cross-sectional view showing that the pores extend down to the silicon surface. Template thickness is 30 nm.



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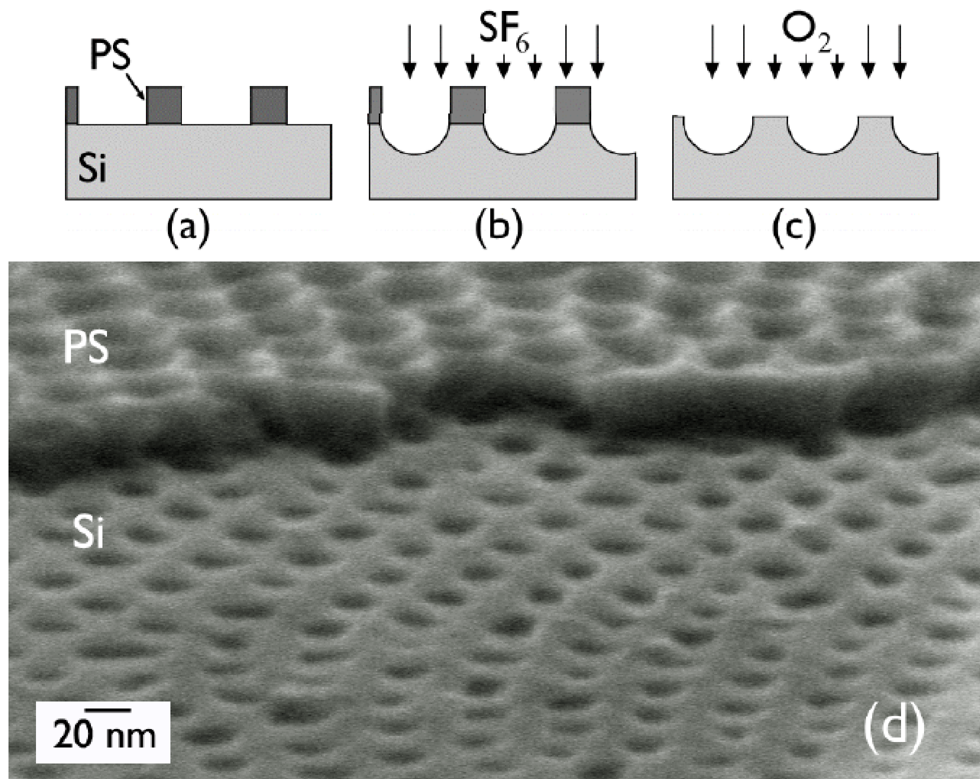

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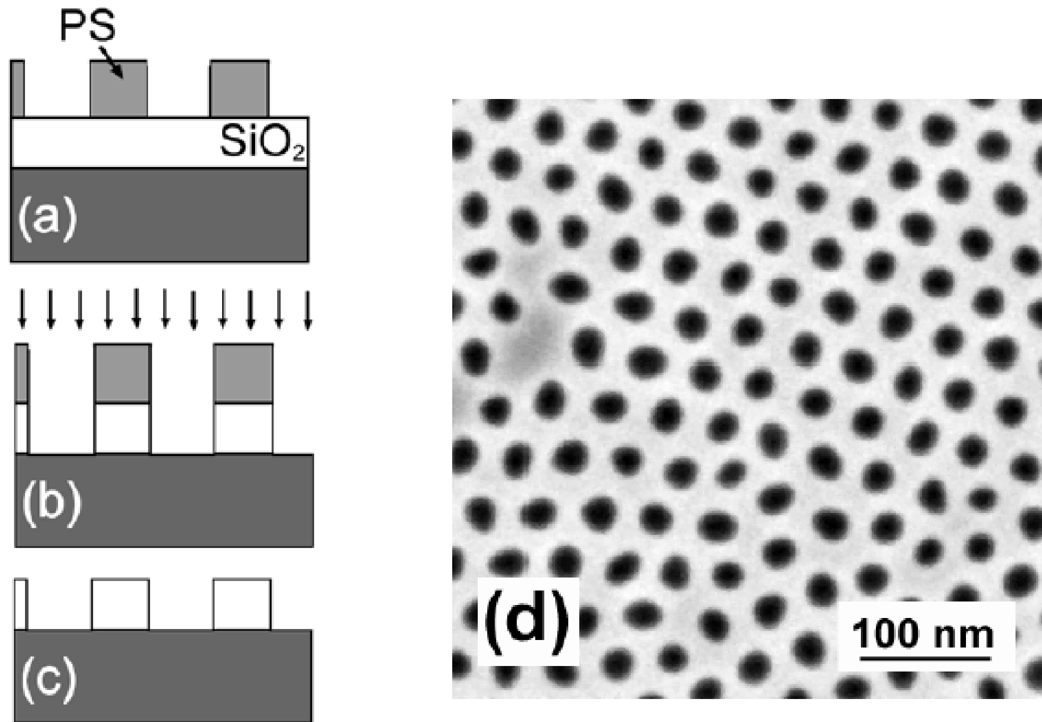

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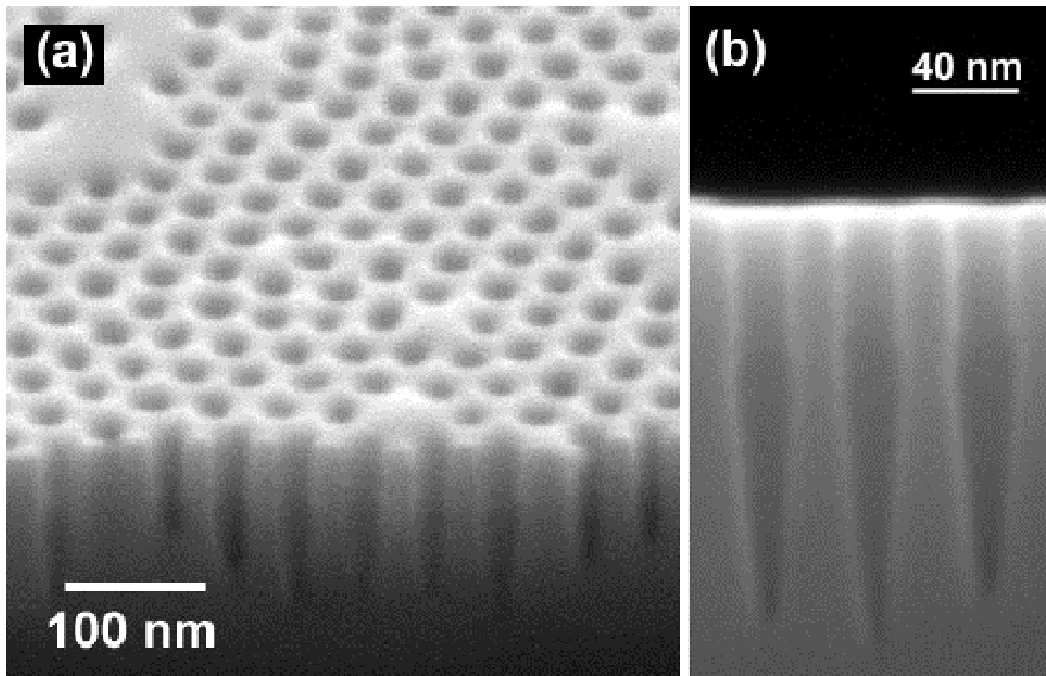

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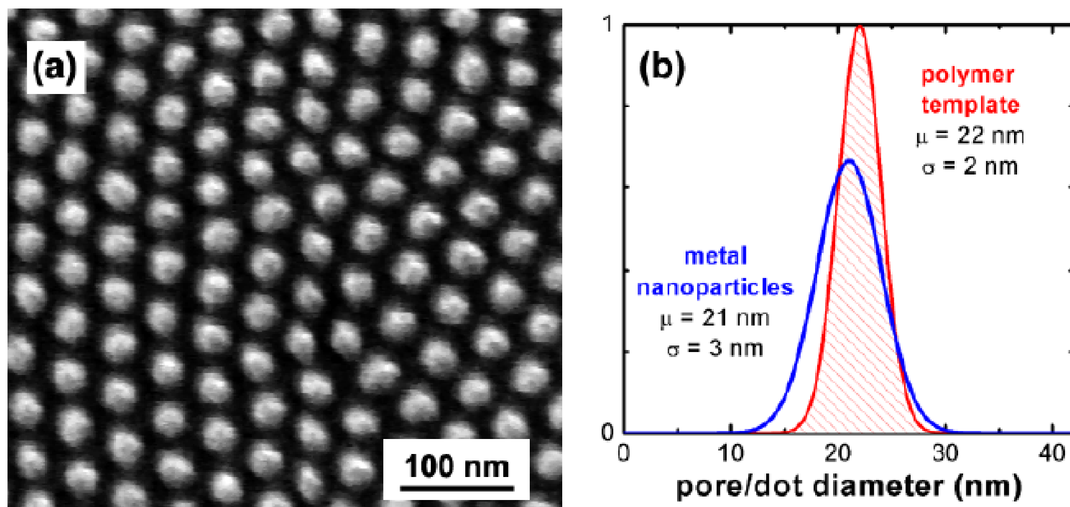

FIGURE 7. (a) Metal dot array formed by liftoff technique with self-assembled polymer mask. (b) Metal nanoparticle dimensions and uniformity correlate with those of initial polymer template.