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Final Report

to

Space and Naval Warfare Systems Center, San Diego
RDT&E Division
for the 1999 Contract N66001-99-C-6000

Investigations of UHV/CVD Deposition of SiGe Alloys on Silicon-on-Sapphire Substrates for Application to Device Fabrication Technology

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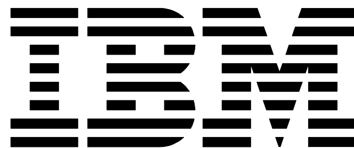


Abstract

We report work on problems related to the fabrication of a SiGe pMODFET static divider circuit on sappahire. We have fabricated SiGe pMODFET devices on silicon-on-sapphire with transconductances as high as 377 mS/mm, f_T = 50 GHz and f_{max} = 114 GHz. We have found that the device characteristics depend very sensitively on the epitaxial layer structure. Very small changes in the layer thickness or doping concentration result in a lower f_T and/or a shift in V_t that can significantly reduce the maximum operating frequency of this circuit. To obtain sufficient device yield to achieve working circuits, choices were made in the fabrication processes that also reduced the operating frequency range of the circuits. Specifically, L_g was chosen to be 0.15 μm and the dielectric layer between M1 and M2 was relatively thin. Devices with a shorter gate length would have a higher f_t and a thicker dielectric layer would reduce the parasitic capacitances. The circuit we fabricated on bulk Si operated up to 3 GHz, with devices having f_T = 17 GHz and V_t = 0.18 V. Circuit modeling indicates that the maximum operating frequency for this circuit fabricated on a thin SiGe-on-sapphire wafer with devices having f_T = 55-72 GHz and an optimized threshold voltage of ~0.3 V would be 25-35 GHz.

Early on we found that the quality of available epitaxial SOS wafers was not good enough for circuit fabrication. Our collaborators at the University of Wisconsin, Madison (UW) have shown that bonded SOS wafers are very promising from a defect perspective. pMODFET layer structures grown on bonded SOS wafers have hole mobility comparable to that on bulk Si. The fact that bonded SOS wafers are stable only up to temperatures of ~600 ^{o}C would not have been a problem for this project, since all fabrication steps are executed at much lower temperatures. Unfortunately, the bonded SOS wafers from UW arrived too late to be used for our final device fabrication run. In any case, to take full advantage of the sapphire substrate, thin SiGe-on-sapphire wafers are required. A similar process can be used for bonding SiGe to sapphire, using thick strain-relaxed step-graded SiGe buffer layers grown epitaxially on SOI as the source of SiGe. However, additional work is necessary to develop a good method to controllably thin the transferred SiGe buffer layer.

I. Introduction

Silicon technology is the mainstream of the semiconductor industry, and IBM advances in the last decade have dramatically increased the performance of silicon based devices. One such recent development is the fabrication SiGe heterojunction bipolar transistor (HBT) circuits and the integration of these circuits with Si CMOS circuits to fabricate BiCMOS chips for applications in wireless telecommunications [1-5]. The use of SiGe in the base region of the HBT has enhanced the performance of Si technology for these applications and SiGe BiCMOS chips are now manufactured at IBM's Burlington plant. Recent research activities at the T.J. Watson Research Center include work on field effect transistors (FETs) using SiGe/Si structures [6-12]. The room temperature mobilities of electrons and holes in a strained Si or SiGe quantum well respectively are about 5-10 times their values in Si CMOS devices. The performance of prototype devices fabricated with these heterostructures is significantly enhanced compared to standard CMOS devices of comparable dimensions [7,9-12]. Another recent development has been the use of silicon-on-insulator (SOI) substrates for improved circuit performance. SOI material has been studied for a number of years, and its use for advanced CMOS circuits is under development. Silicon-on-sapphire (SOS) is another type of SOI substrate now in use for the manufacture of CMOS circuits for applications in RF communications [13].

The goal of this project was to explore the potential of pMODFET devices and circuits on SOS substrates. The pMODFET device was selected, since it can be fabricated using very low temperature processes on small wafers, 5" or less in diameter, using "off-line" processing equipment at IBM. This was necessary because 8" diameter SOS wafers were not available for this project and, consequently, IBM's clean room fabrication facility could not be utilized. The restriction of working with small wafer sizes severely limited the fabrication processes available for this project. The demonstration circuit chosen was a static divider circuit, designed by Prof. Peter Asbek's group at the University of California in San Diego. This circuit has about 50 transistors and thus the device yield must be 98.6% in order to yield 50% working circuits.

In the early phase of this project, pMODFET devices were fabricated on an epitaxial SOS substrate. Our initial work showed, first that epitaxial SOS substrates are not suitable for fabricating pMODFET circuits. Because of high densities of microtwin defects in the Si layer, large faceted pits are found in the pMODFET layer structures. The good area between the pits was smaller than the area required for the divider circuit. Secondly, we found that a much more robust fabrication process would be needed to achieve the device yield necessary to obtain working circuits. The T-gates of the pMODFET devices were mechanically fragile and many of them did not withstand subsequent fabrication steps.

Two parallel activities were then initiated. To address the issue of the high defect density in epitaxial SOS substrates, a collaboration was established with Prof. Thomas Kuech at the University of Wisconsin, Madison (UW) to explore the feasibility of achieving high quality silicon-on-sapphire (SOS) and SiGe-on-sappphire (SGOS) substrates by wafer bonding methods. Good quality bonded SOS wafers were fabricated

and mobility comparable to that in the same layer structure grown on a bulk Si substrate was demonstrated. SiGe layers were transferred to sapphire using a similar process. UW provided bonded SOS wafers suitable for subsequent device and circuit runs. SGOS wafers were also fabricated at UW and looked very good after low temperature annealing. However, because the transferred SiGe layer was very thick, bubbles formed at the bonded interface during annealing at 550 ^{o}C, the growth temperature of the pMODFET layer structures. This problem is easily solved by thinning the SiGe layer prior to annealing at temperatures >250 ^{o}C.

A more robust fabrication process was developed using pMODFET layer structures on bulk Si substrates. Process yield was excellent and working divider circuits that operate up to 3 GHz were fabricated. Circuit modeling demonstrates that this performance is expected from the individual device characteristics and the back end metallurgy that was used. The fact that working divider circuits were achieved also demonstrates that the pMODFET layer structures on bulk Si have a low enough defect density to achieve working divider circuits.

At this point the major problems had been solved and the next step would have been to do another run to fabricate bonded SGOS wafers, then to grow high mobility pMODFET structures on both bonded SOS and SGOS substrates and, finally, to fabricate the divider circuit. However, by this time all the funds available for this contract had been spent, and thus we were not able to continue.

This report is organized as follows. Sections II-IV describe the growth of the pMODFET layer structures on SOS wafers and an evaluation of various types of SOS wafers. Initial device fabrication and device results are presented in sections V and VI and the mask design for a test site that includes the static divider circuit is discussed in section VII. The device fabrication process development and characterization of the fabricated devices and circuits is discussed in sections VIII and IX. An analysis of the potential of these pMODFET devices and this divider circuit on bulk Si and on sapphire based our experimental results and on SPICE modeling is discussed in section X.

II. Growth of SiGe pMODFET Layer Structures on Epitaxial SOS Wafers

The Ultra High Vacuum Chemical Vapor Deposition (UHVCVD) growth technique used in this study was developed and patented by IBM [14]. This growth technique is an isothermal multi-wafer CVD system operating at UHV base pressures of ($P<10^{-9}$ torr) at T=500 °C, with a load-lock transfer system designed to eliminate contamination during wafer entry. Epitaxial growth of silicon (Si) and silicon germanium (SiGe) alloys on both Si and SOS substrates is achieved by pyrolysis of silane (SiH_4) and germane (GeH_4) gas sources under very low deposition pressure (1-2 millitorr). Typical growth temperatures are between 350 to 600 °C. Growth rates for SiGe alloy films can be varied from 5 Angstroms to > 50 Angstroms per minute depending upon Ge incorporation into the film, as well as other factors. Si growth rates are much slower, varying from 1 Angstrom to 25 Angstroms per minute, depending on the growth temperature. Growth rates also vary with the substrate material and orientation. Another attribute of this growth technique is in-situ doping capability using B_2H_6 for p-type doping and PH3 for n-type doping. Doping redistribution does not occur at these low growth temperatures, thus extremely narrow and abrupt dopant profiles can be achieved.

To ensure epitaxial growth quality, wafer preparation is a critical aspect of the overall growth process. It is imperative the initial growth surface be pristine, as a high temperature in-situ clean is not available. An external hydrogen passivation step is done just prior to loading. Typically, starting wafers are initially Huang Cleaned and then etched in (10:1) HF immediately prior to loading into the reactor. This ex-situ hydrogen passivation maintains a hydrogen-terminated silicon surface.

The epitaxial layer structure for the SiGe pMODFETs consists of a thick step-graded strain-relaxed SiGe buffer layer with the active device layers grown on top. As shown in Fig. 1, the strain-relaxed buffer layer, which serves as a "virtual substrate" for the pMODFET device, is $Si_{1-x}Ge_x$ where x~0.35 and the strained $Si_{1-x}Ge_x$ channel is a composite layer with varying alloy composition and x>0.75. The SiGe pMODFET layer structures were grown epitaxially by UHVCVD, using either 5" or 4" diameter Si(001) and SOS wafers. UHVCVD is a batch process; each growth run yields five device-quality wafers.

X-ray diffraction scans of the pMODFET layer structure grown on bulk Si and on an SOS substrate 4" diameter SOS wafer are shown in Fig. 2. The SOS wafer was purchased from Union Carbide and improved at SPAWAR (we will refer to these as UC/SPAWAR SOS wafers) [15,16]. The x-ray measurements were done at beamline X20 at the National Synchrotron Light Source at Brookhaven National Laboratory. The synchrotron x-ray source was needed to provide enough intensity to measure the very thin strained SiGe channel layer. There are differences in these scans, since the wafers are from different growth runs. Note that the diffraction peak from the thin SOS layer is much less intense than that from the bulk Si substrate.

Pieces of a pMODFET structure on a bulk Si substrate wafer were annealed at various temperatures in a He atmosphere to determine the thermal stability of these

layers; some of the results are shown in Fig. 3. A small shift of the SiGe buffer layer peak was seen after annealing at temperatures as low as 650 C, indicating that further strain relaxation of the SiGe buffer layer occurs during annealing. More important, however, is the large (~1°) shift in the diffraction peak from the strained Si channel, seen after annealing at 650 ^{o}C, and still larger (~3°) shift after annealing at 850 ^{o}C. This peak shift indicates that either the strain or the Ge fraction of the SiGe channel has decreased significantly. Strain relaxation results from the formation of misfit dislocations at the lower channel interface, whereas the alloy composition decreases by interdiffusion of Si and Ge at both channel interfaces. Although a detailed annealing study of these layer structures was not performed, the data in Fig. 3 clearly demonstrate the need for very low temperature device fabrication processes to preserve the integrity of the device layer structure.

Figures 4 and 5 show optical images of a pMODFET layer structure grown simultaneously on a bulk Si substrate and on a UC/SPAWAR SOS wafer. There is an obvious and significant difference between the pMODFET layer structure grown on the bulk Si wafer and on the UC/SPAWAR SOS wafer; there are large faceted pits on the SOS wafer surface. The density of these pits is $3 x 10^{5}$ cm^{-2}. Figures 6 and 7 show optical micrographs of the SiGe pMODFET layer structure grown on a 5" diameter SOS purchased from Peregrine Semiconductor Inc. Note the much higher density of faceted pits in the SiGe layers grown on the Peregrine SOS wafers. A bulk Si wafer from the same growth run looked like the bulk Si wafer in Fig. 4; therefore the difference in the density of the pits must be due to a difference in the two SOS wafers.

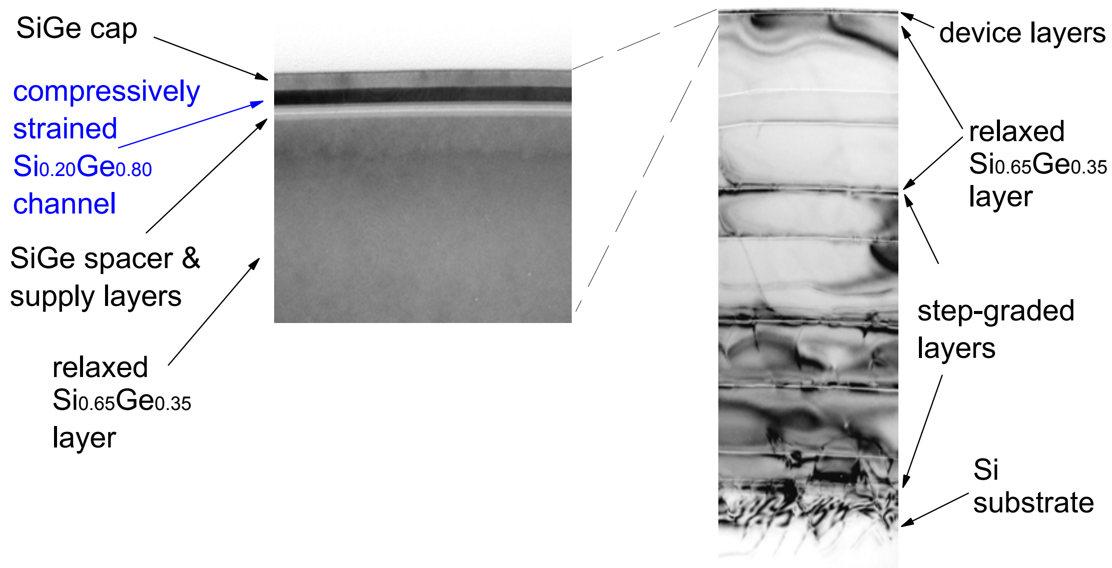
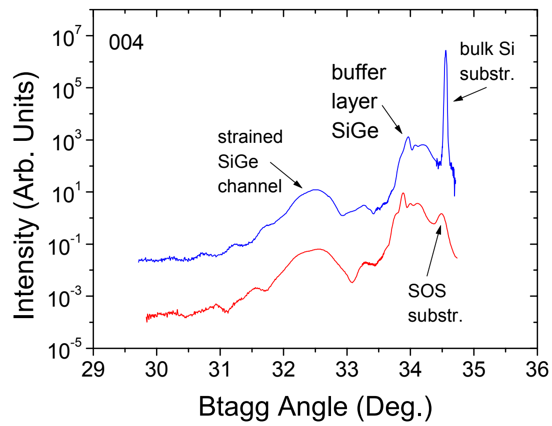


Fig. 1. Cross sectional TEM of a pMODFET layer structure.



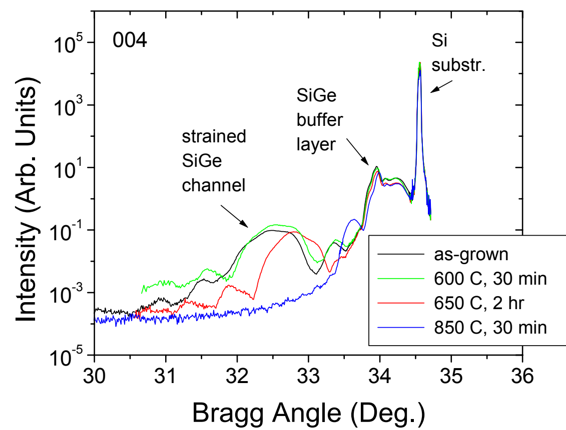
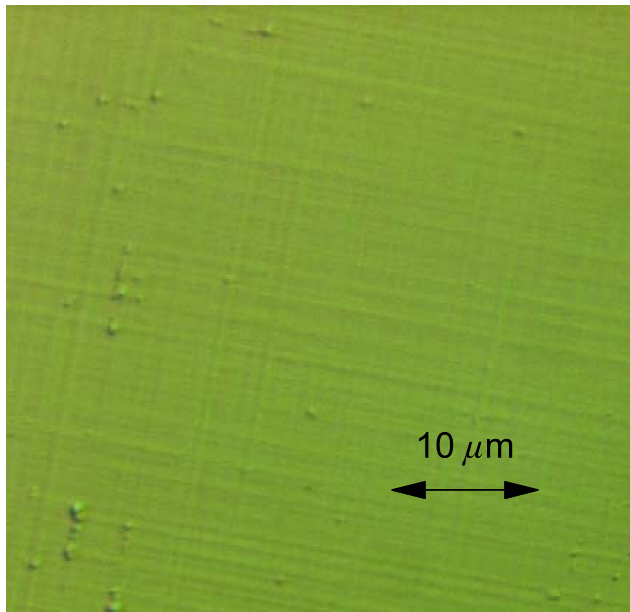


Fig. 2. X-ray diffraction scan of pMODFET structures on bulk Si and on a US/SPAWAR SOS substrate (Gov31).

Fig. 3. X-ray diffraction scans of as-grown and annealed pMODFET structures.



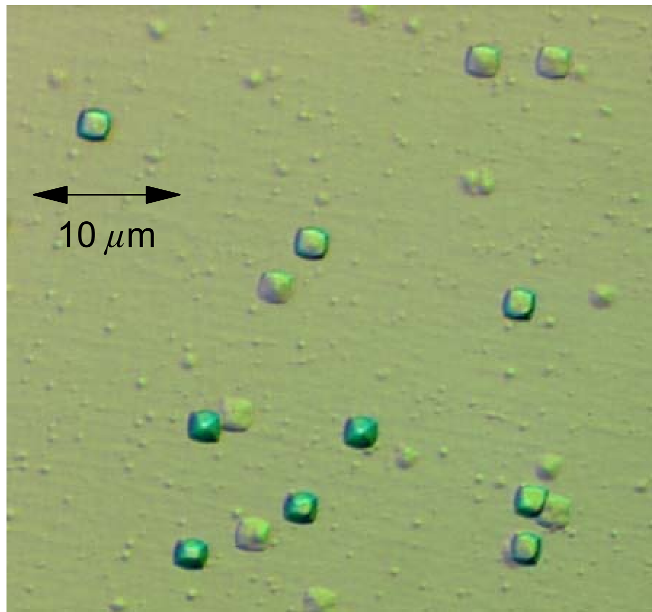


Fig. 4. pMODFET layer structure on a bulk Si substrate (Gov32).

Fig. 5. pMODFET layer structure on a UC/SPAWAR SOS wafer (Gov32).

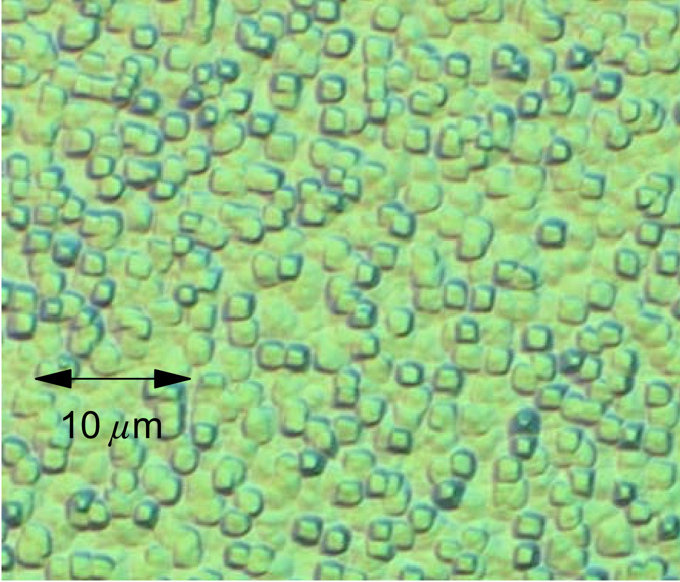


Fig. 6. pMODFET layer structure on a Peregrine SOS wafer measured at the center of the wafer (Gov35).

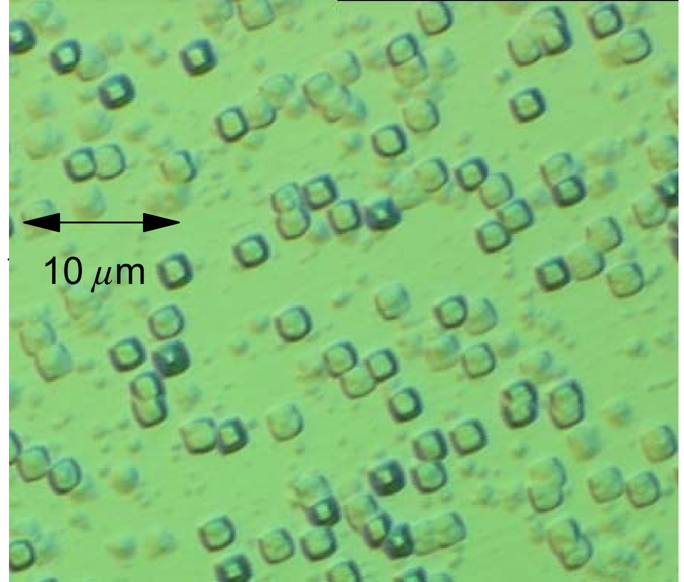


Fig. 7. pMODFET layer structure on a Peregrine SOS wafer measured at the edge of the wafer (Gov35).

Hall effect measurements were performed to determine the hole density and mobility as a function of temperature in these pMODFET layers. A bulk Si wafer and and SOS wafer from each epitaxial growth run was measured. Fig. 8 shows the data for the SOS wafer from run Gov31 as an example. The results of Hall effect measurements from three different growth runs are given in Table I. Note that for the Union Carbide SOS wafers the mobility and carrier concentration are similar to that on bulk Si wafers from the same growth run. Although the hole density on the Peregrine SOS wafer and on the companion bulk Si wafer were comparable, the hole mobility measured on the Peregrine wafer was much lower, presumably because of the high density of pits on this wafer.

This work shows that pMODFET layer structures grown on SOS wafers have a similar hole mobility and hole density to layer structures grown simultaneously on bulk Si(001), provided the density of faceted pits is below $1x10^{6}$ cm^{-2}. While there is a good probability that working devices can be fabricated on UC/SPAWAR wafers, these wafers are not suitable for circuit fabrication.

Table I: Hole density and mobility from Hall effect measurements at 300 K and 20K done on wafers from three different SiGe pMODFET epitaxy runs.

Growth Run **Substrate**	**N_s at 300 K** (10^{12} cm^{-2})	**Mobility at 300 K** (cm^2/Vs)	**N_s at 20 K** (10^{12} cm^{-2})	**Mobility at 20 K** (cm^2/Vs)
Gov31 UC/SPAWAR SOS	2.5	804	2.4	2251
Gov31 Bulk Si	2.5	913	2.0	3565
Gov32 UC/SPAWAR SOS	2.2	595	1.8	1766
Gov32 Bulk Si	3.1	576	2.4	1832
Gov35 Peregrine SOS	2.0	113	1.4	64
Gov35 Bulk Si	2.1	660	1.6	1564

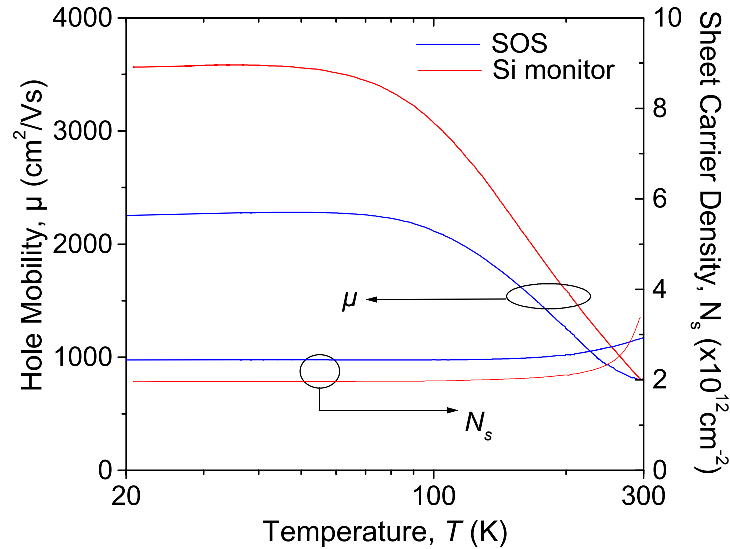


Fig. 8. Hall effect data from a pMODFET layer structures on a UC/SPAWAR SOS wafer and on bulk Si (Gov31).

III. Evaluation of Epitaxial SOS Wafers

In order to understand the origin of the faceted pits seen on the pMODFET wafers, both planar view and cross sectional TEM measurements were done on a 5" diameter Peregrine SOS wafer (Figs. 9 and 10). These measurements demonstrate a very high density of microtwin defects in this wafer compared to UC/SPAWAR SOS wafers [15,16]. An 8" diameter ribbon SOS wafer was also investigated by planar view TEM for comparison. For the ribbon SOS wafer, the Si deposition was done at Lawrence Semiconductor and the improvement was done at IBM using a process similar to the SPAWAR improvement process. Although the Si deposition was done at Lawrence Semiconductor for both the 8" ribbon and 5" Peregrine wafers, the density of microtwins is nearly an order of magnitude lower in the 8" ribbon wafer. The results are summarized and compared with those for UC/SPAWAR SOS wafers in Table II. The data for UC/SPAWAR wafers are from Refs. 15 and 16.

The density of microtwins determined by TEM for the UC/SPAWAR and Peregrine wafers is comparable to the density of faceted pits on the SiGe p-MODFETs grown on these wafers. The growth rate for Si or SiGe is about an order of magnitude slower on Si(111) than on Si(001). At the microtwin defects the crystal orientation is Si(111). The resulting slower growth rate for SiGe at the microtwin defect results in a faceted pit in the case of a thick SiGe layer. We conclude from TEM measurements of the Peregrine wafers that the high density of faceted pits observed in the pMODFET layers originates from the high density of microtwin defects in the Si layer.

When we reported that the SOS wafers we purchased from Peregrine Semiconductor were not suitable for this application, Peregrine undertook a project to provide us with SOS wafers having Si layers with lower defect densities. p-MODFET layer structures were grown to evaluate these new wafers, which included two that had undergone different variations of a double improvement process after deposition of Si at Lawrence Semiconductor and one that received the standard single improvement process. A wafer originally purchased from Peregrine by IBM that had a high temperature deposition of Si to restore the Si layer to its original thickness (done at IBM) and was then implanted and annealed by Peregrine for further defect reduction was also included

Table II: Comparison of the defect densities in various SOS wafers.

Wafer	**microtwin defects** (cm^{-2})	**threading dislocations** (cm^{-2})
4" UC/SPAWAR SOS	$<1x10^6$	$\sim1x10^8$
8" ribbon SOS	$\sim2.5x10^7$	$\sim1.3x10^9$
5" Peregrine SOS	$\sim1.8x10^8$	$\sim1.5x10^9$

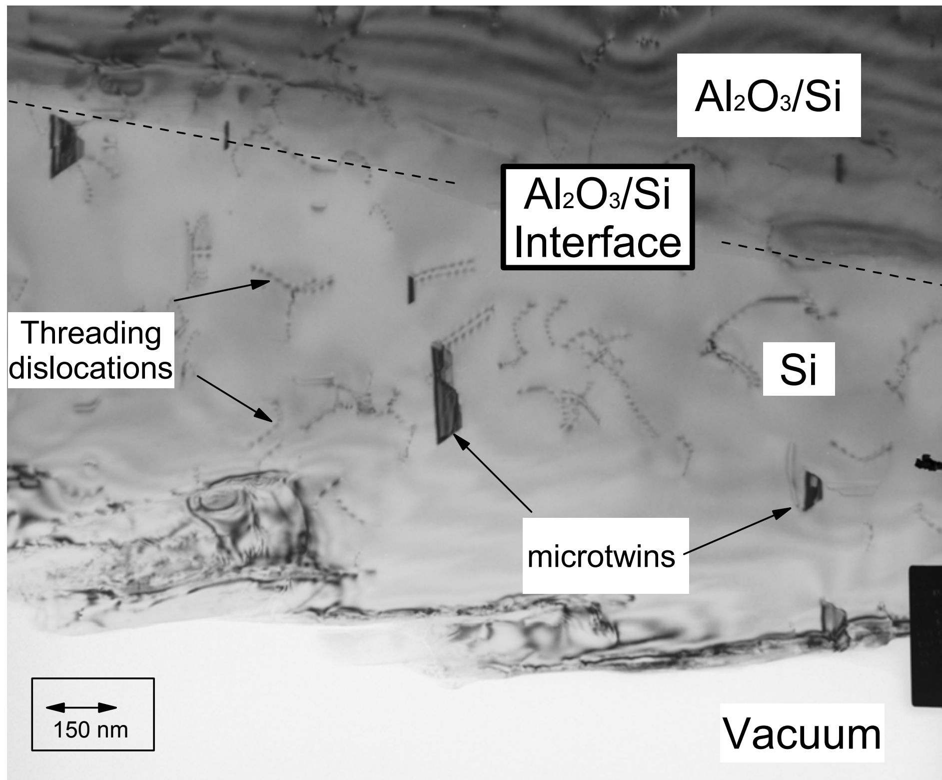


Fig. 9. Planar view TEM image of a Peregrine SOS wafer. Both threading dislocations and microtwin defects are observed.

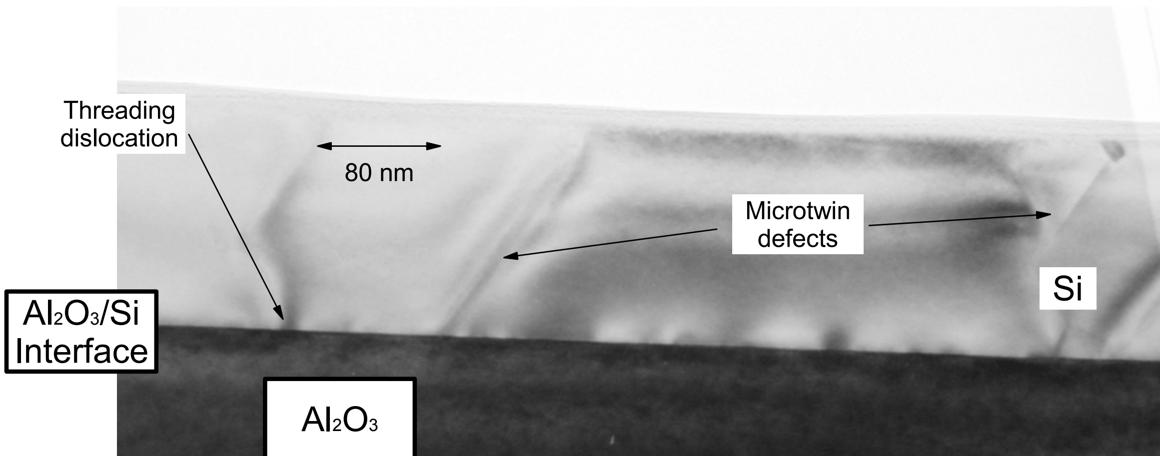


Fig. 10. Cross sectional TEM image of a Peregrine SOS wafer. Both threading dislocations and microtwin defects are observed.

in the UHV/CVD run. The latter wafer (Gov40.3) showed a reduction in surface pits near the wafer edges as did the Peregrine "double improved" wafer that received no anneal after the first implant (Gov40.5).

The results, summarized in Table III, are disappointing. Wafers #0021 and #0008 show a very rough surface. The faceted pits cannot be distinguished as they were on our previous UHV/CVD runs on Peregrine wafers (Gov35 and Gov36). The Nomarski phase contrast images of #0008 (Gov40.6) and from #0021 (Gov40.4) were similar. Wafers #0011 (Gov40.3) and #0020 (Gov40.5) are comparable to our previous growth runs on Peregrine wafers. These wafers are not uniform and have a lower pit density near the edge of the wafer. The bulk Si wafer (Gov40.7) was comparable to previous UHV/CVD runs (e.g. Gov35) indicating that wafer cleaning conditions were normal and that poor cleaning is not the cause of the high pit densities observed on these wafers. The control wafer (#0021) that received the standard single improvement process looked much worse than the wafers we previously purchased from Peregrine. Images from wafer #0011 are very similar to those from previous runs Peregrine wafers from the same batch that received only the standard single improvement process. The Nomarski images on wafers from the UHV/CVD growth of a p-MODFET layer structure indicated no improvement in Peregrine SOS wafer quality, but rather the opposite. None of these new wafers has a density of surface pits as low as the UC/SPAWAR SOS wafers.

These experiments clearly show that the available epitaxial SOS substrates are not suitable for the development of pMODFET devices and circuits. Although the hole mobility is good on the UC/SPAWAR SOS wafers, the density of large faceted pits is high enough that it is unlikely that the device yield would be sufficient to achieve working divider circuits on these wafers.

Table III: Wafer characteristics and results of Gov40 pMODFET layer growth run.

Wafer number	**Processing prior to UHV/CVD growth of p-MODFET layer structure**	**Pit density after UHV/CVD growth of p-MODFET layer structure**
Gov40.3 (#0011)	IBM Si deposition: reprocessed using single improvement process	High pit density at center (frosty surface) but lower density at edges.
Gov40.4 (#0021)	Single improvement process: control	High pit density everywhere as before (frosty surface).
Gov40.5 (#0020)	Double improvement: standard implants but no anneal after 1st implant	High pit density at center (frosty surface) but lower density at edges.
Gov40.6 (#0008)	Double improvement: standard process twice	High pit density everywhere (frosty surface).
Gov40.7	Bulk Si substrate	Shiny flat surface as usual!

IV. Bonded Silicon-on-Sapphire and SiGe-on-Sapphire Wafers

Having high quality SOS wafers is crucial for this project. The use of wafer bonding methods to transfer a thin layer of bulk Si to sapphire to obtain high quality SOS substrates had been proposed earlier [15]. If a successful bonding technology could be developed for Si, the same method could very likely also be used to transfer a thin layer of SiGe to sapphire. A strain-relaxed SiGe buffer layer on Si could be used as the source material for good quality strain-relaxed SiGe. A contract (contract number) was awarded to Prof. Thomas. F. Kuech at the University of Wisconsin, Madison (UW) to investigate wafer bonding of Si and SiGe to sapphire. The plan was to first demonstrate bonded SOS wafers by transferring a thin Si layer from an SOI wafer to sapphire. The same or a similar process would then be used fabricate SiGe-on-sapphire (SGOS) using strain-relaxed SiGe buffer layers grown on SOI substrates provided by IBM.

A major difficulty for SOS is that Si and sapphire have different thermal expansion coefficients. To facilitate transfer of a thin Si layer, an SOI wafer was bonded to a sapphire wafer. Problems related to the difference in thermal expansion were minimized by first annealing the bonded wafers at low temperature (~250 C), then removing the Si substrates form the SOI wafer by grinding and etching using the buried oxide layer as an etch stop, and finally strengthening the bonded interface by heating of the sapphire with the thin Si layer to higher temperature. Direct bonding of Si to sapphire was not successful; however, SOI wafers coated with a thermal oxide were successfully bonded. The UW group found that the quality of the transferred Si layer was good when the bonded SOS wafer was annealed at temperatures up to ~600 C. Annealing at higher temperatures resulted in degradation of the Si layer as indicated by the increased width of the x-ray rocking curve [17-19]. The exact temperature that the bonded SOS wafer can withstand without degradation of the Si layer very likely depends on the both the properties of the interfacial oxide layer and the thickness of the transferred Si layer.

Bonded SOS wafers received from UW were evaluated at IBM by optical microscopy before and after growth of a pMODFET layer structure. An example of a good quality bonded SOS wafer as-received from UW is shown in Fig. 11. This image shows an area of the bonded SOS wafer with only one visible defect, a small “bubble”. Other areas of this wafer showed a slightly higher density of bubbles. Fig. 12 is the optical image of a pMODFET layer structure grown on a bonded SOS wafer. Except for the small bubbles, the wafer surface looks like a pMODFET layer structure on bulk Si. When few defects are seen at the bonded interface, the pMODFET layer looks good.

Fig. 13 shows an AFM image of the pMODFET on bulk Si. The usual cross-hatch pattern is observed. As is seen in Fig. 14, the surface of the pMODFET structure on SOS1 is similar. The RMS roughness is slightly less on the image of the structure on the SOS substrate. The lower value for the RMS roughness on the SOS substrate is expected, since there are fewer rows of pits due to dislocation interactions when the SiGe buffer layer relaxes on this wafer.

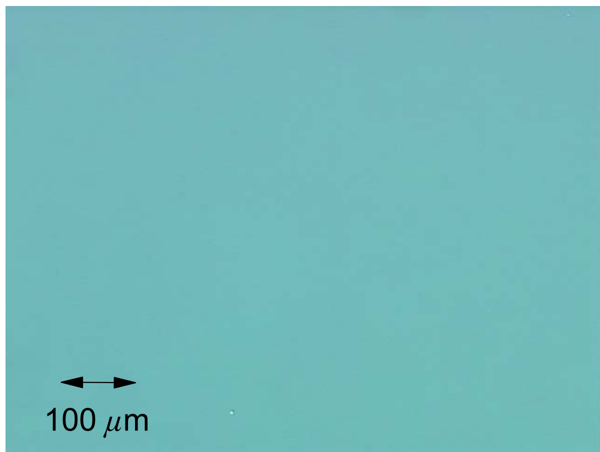


Fig. 11. Optical micrograph of a bonded SOS wafer as-received from UW. This wafer had been annealed at 600 C.

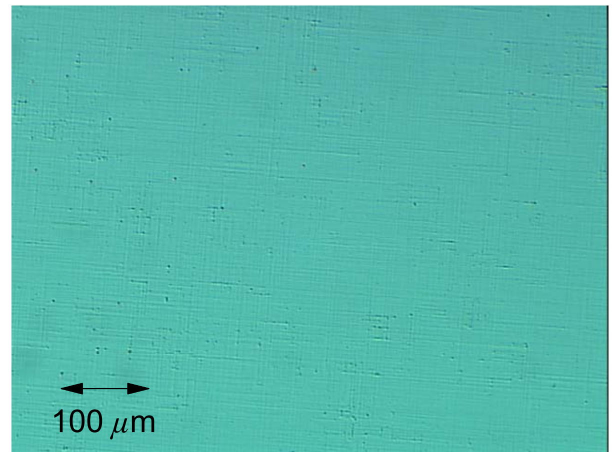


Fig. 12. Optical micrograph of a pMODFET layer structure on a bonded SOS wafer (Gov67A.08).

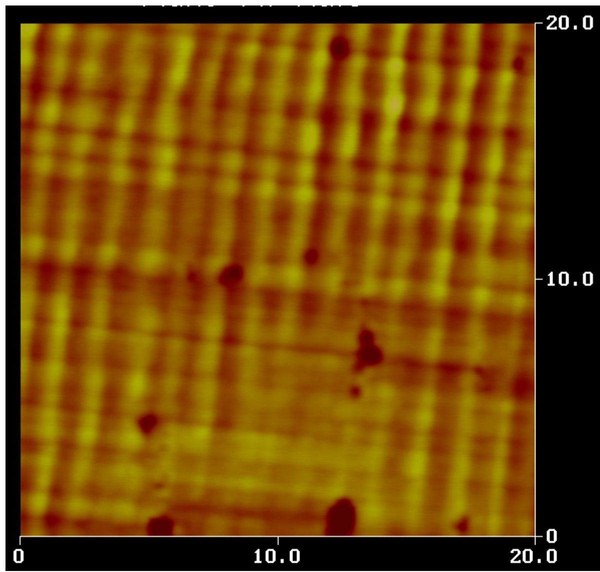


Fig. 13. AFM image of the surface of the p-MODFET structure on bulk Si (Gov66A). The Z-range of this image is 98 nm and the RMS roughness is 7.0 nm

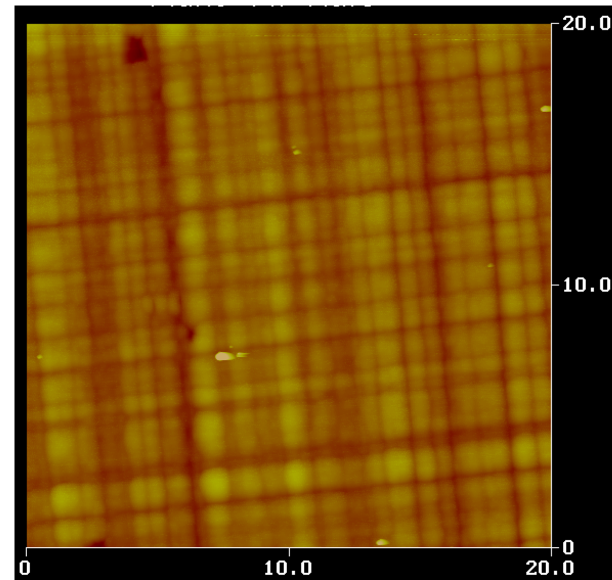


Fig. 14. AFM image of the surface of the p-MDFET structure on SOS1 (Gov66A). The Z-range of this image is 104 nm and the RMS roughness is 4.4 nm.

Table IV summarizes the HRXRD results from a bulk Si and SOS wafer from two growth runs. For both growth runs, the structure on the SOS substrate has slightly higher alloy composition and is a little less relaxed. The buffer layers on the two structures on bulk Si substrates appear to be identical.

Temperature dependent Hall effect measurements were done on the two wafers from Gov66A and the bulk Si wafer from Gov67A and the results are given in Table V. Hall effect data from the bonded SOS wafer are shown in Fig. 15. The data are similar for the pMODFET structures from Gov66A on the bulk Si and SOS substrates with a slightly (6%) higher mobility on the SOS substrate. The mobility on Gov67A.07 (bulk Si substrate) was 35% higher at room temperature and 73% higher at low temperature than that of Gov66A.07 (bulk Si substrate). The low temperature carrier density was 22% lower in Gov67A.07. The reason for this difference is not clear at this time. These room temperature mobility values are similar to those of the pMODFET wafers that are being used for fabrication process development.

Table IV: Alloy composition and strain relaxation

Wafer	Substrate	Alloy Composition, x, of Buffer Layer	% Strain Relaxation in Buffer Layer
Gov66A.07	Bulk Si	0.41	87
Gov66A.08	SOS1	0.42	77
Gov67A.07	Bulk Si	0.41	85
Gov67A.08	SOS2	0.43	81

Table V: Hole mobility (μ_h) and hole density (n_s)

Wafer	Temperature (K)	μ_h (cm^2/V-s)	n_s (10^{12} cm^{-2})
Gov66A.07 (bulk Si)	300	412	2.82
"	25	2344	1.61
Gov66A.08 (SOS1)	300	439	2.66
"	29	2440	1.88
Gov67a.07 (bulk Si)	300	556	2.95
"	25	4056	1.26

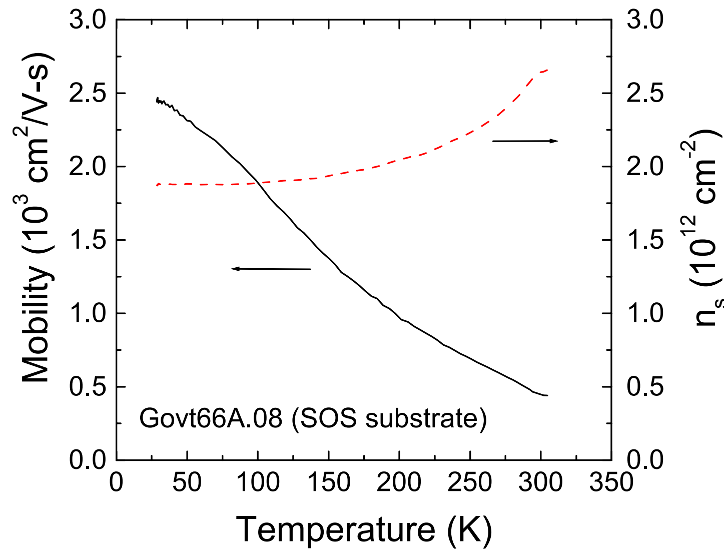


Fig. 15. Hole mobility and sheet density vs. temperature for the pMODFET structure on a bonded SOS substrate.

In summary, good quality p-MODFET structures were grown on bonded SOS substrates received from UW. Although one wafer had areas with a very high density of bubbles at the interface, both wafers behaved similarly during UHC/CVD epitaxy at about 550 ^{o}C. No large faceted pits were observed on the SOS wafers. This is primarily due to the absence of microtwin defects in the bonded SOS layer. The better surface morphology on the SOS wafers, i.e. the reduced density of rows of pits due to dislocation interactions when the SiGe buffer layer relaxes, suggests that device yields on SOS substrates may be higher than on bulk Si. These initial results on bonded SOS wafers are very encouraging and UW then provided additional wafers to IBM for pMODFET device and circuit fabrication runs.

The pMODFET devices are grown on a relaxed SiGe buffer layer that is on the order of 1-2 microns thick and thus the full advantage of the sapphire substrate will not be realized when the pMODFET layer structure is grown on an SOS wafer. It is therefore more desirable to transfer a thin SiGe layer to sapphire to form SiGe-on-sapphire (SGOS) for this application. To investigate the use of wafer bonding methods to transfer the upper part of a relaxed SiGe buffer layer to sapphire, relaxed SiGe buffer layers were grown on SOI substrates for wafer bonding experiments. Bonding SiGe to sapphire is more complicated than bonding Si to sapphire for several reasons. First, the surface of the relaxed SiGe buffer layers is not smooth enough for bonding; there is a cross-hatch surface pattern, which originates from the 60° misfit dislocations that relieve the lattice

mismatch strain. A typical value for the RMS roughness is ~4 nm as shown by the atomic force micrograph in Fig. 16. Chemical-mechanical polishing (CMP) was used successfully to achieve the smooth SiGe surfaces required for wafer bonding of 5" diameter bonded silicon-on-insulator wafers [20]. A second complication is that a good quality thermal oxide does not form on SiGe and thus a deposited oxide layer must be used instead. Typically, the wafer surface must be polished a second time after oxide deposition to be smooth enough for wafer bonding.

Experiments were done to develop a CMP process for relaxed SiGe buffer layers grown on 4" diameter Si or SOI substrates. Polishing of SiO_2 films deposited on polished and unpolished SiGe buffer layers was also investigated. Wafer cleaning after CMP is the most critical and difficult step of this process. All particles must be removed after polishing in order for the wafer to be useful for further processing. The AFM image of a polished SiGe wafer is shown in Fig. 17. Figures 18 and 19 show AFM images of an unpolished SiGe wafer (Gov42) with 750 nm of deposited SiO2 and the wafer surface after polishing. Polished SiGe buffer layers and buffer layers with a polished oxide surface on SOI substrates were sent to UW for wafer bonding experiments.

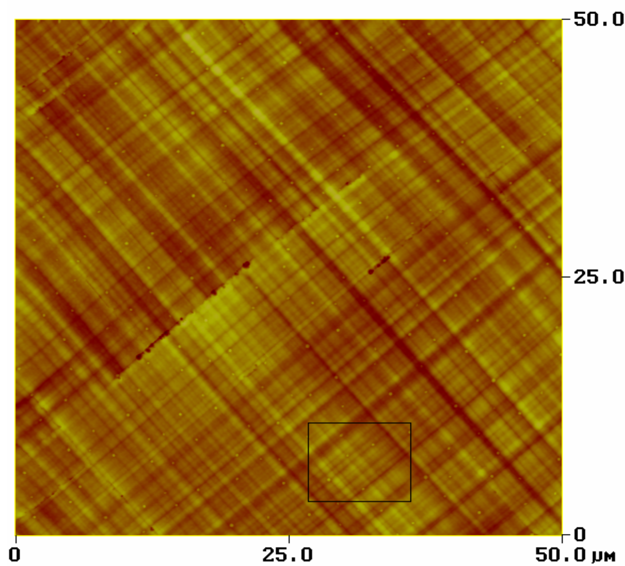


Fig. 16. AFM image of a relaxed SiGe buffer layer (Gov41) for wafer bonding experiments. The Z-range in the box is 25.79 nm and the RMS roughness is 4.07 nm.

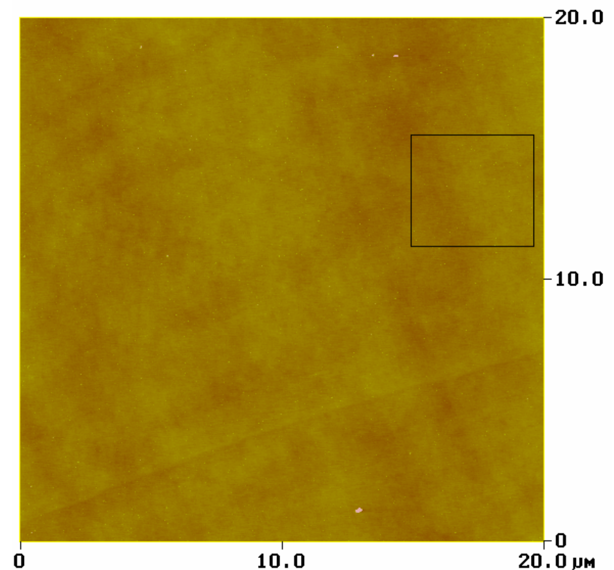


Fig. 17. AFM image of a polished SiGe buffer layer (Gov41) for wafer bonding experiments. The Z-range in the box is 2.8 nm and the RMS roughness is 0.401 nm.

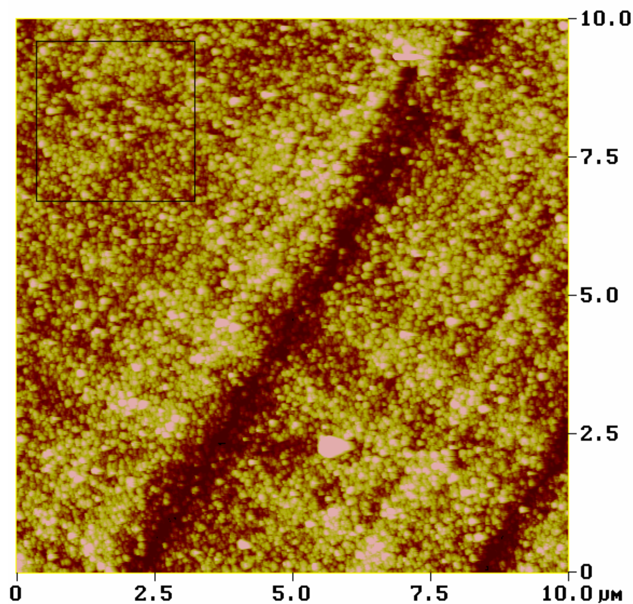


Fig. 18. AFM image of a relaxed SiGe buffer layer with 750 nm of deposited SiO2. The Z-range of the entire image is 75.12 nm and the RMS roughness is 5.31 nm.

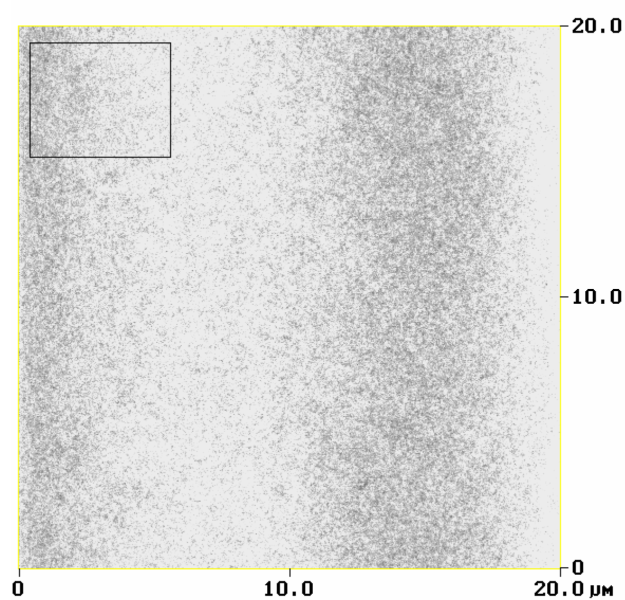


Fig. 19. AFM images of a polished SiGe buffer layer with deposited SiO2. The Z-range of the entire image is 7.12 nm and the RMS roughness of 0.43 nm.

The SiGe wafers sent to UW were bonded to sapphire using a process similar to that used for bonding Si to sapphire. The bonding at low temperature was successful and the Si substrate was successfully removed leaving the SiGe graded buffer layer and buried oxide layer. However, after subsequent annealing of these wafers at either 300 ^{o}C or 550 ^{o}C, bubbles appeared at the bonded interface. This indicates that the bonded interface did not withstand the stresses that are present at elevated temperatures due to the different thermal expansion of the SiGe and the sapphire. The transferred SiGe layers were considerably thicker than the transferred Si layers and thus the stresses at the bonded interface were greater for the bonded SiGe layers than for the Si layers. These layers ought to have been thinned prior to annealing at 550 ^{o}C.

Considerable progress has been made on our understanding of the critical issues for wafer bonding of Si and SiGe to sapphire. The work at UW shows that wafer bonding methods can provide a good quality Si layer on sapphire that is stable up to about 600 ^{o}C. Initial results indicated that the same process can be used for bonding SiGe to sapphire. However, additional work is needed to develop a method to obtain a controlled thickness of the transferred Si layer, perhaps by means of an etch stop layer incorporated during the growth of the relaxed SiGe buffer layer structure.

V. SiGe pMODFETs on SOS: Fabrication and Characterization

Despite the presence of faceted pits on the UC/SPAWAR wafers, it was decided to fabricate pMODFET devices in order to demonstrate SiGe pMODFETS on sapphire substrates, since no better quality SOS substrates were available at the time. This fabrication run would serve as a “pipe cleaner” run to identify any difficulties in processing pMODFETS on sapphire substrates and to provide information on aspects of the fabrication process that might negatively impact the device yield.

A detailed schematic of the device structure in shown in Fig. 20. The device fabrication steps are indicated schematically in Fig. 21. The Source and Drain Ohmic contacts were formed using a simple, self-aligned evaporation of 20 nm Pt, followed by a sinter of 350 ^{o}C for 7.5 minutes. No implantation step was used for the Ohmic contacts. Typically the devices show a low on-resisitance of approximately 1.3 Ohm mm.

Optical micrographs of DC device structures taken on bulk Si and on SOS are shown in Figs. 22 and 23 respectively. Note the large faceted pits present only on the SOS wafer. When gate of a device falls on a pit, the device does not operate.

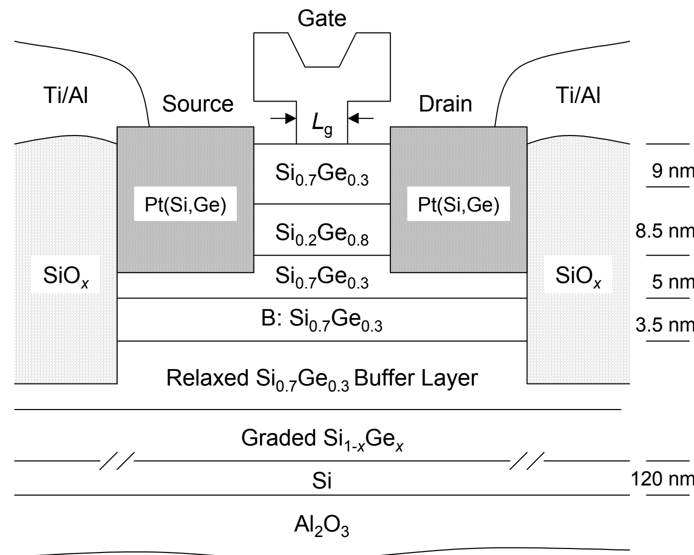
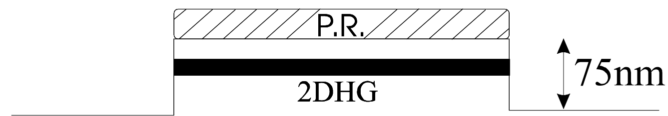


Fig. 20. Cross-section of layer structure and pMODFET device design.

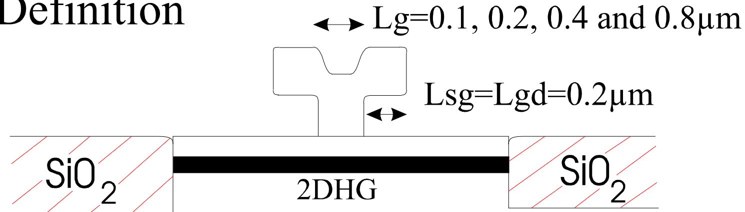
Device Fabrication Steps

1. Mesa Isolation

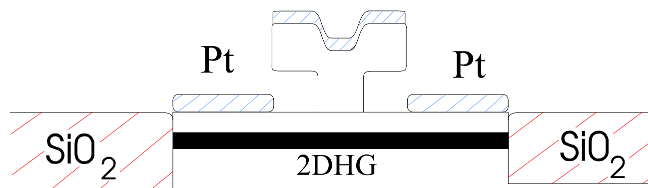


2. Pad Isolation

3. T-Gate Definition



4. Self-Aligned Ohmic



5. Ohmic Sinter And Pad Definition

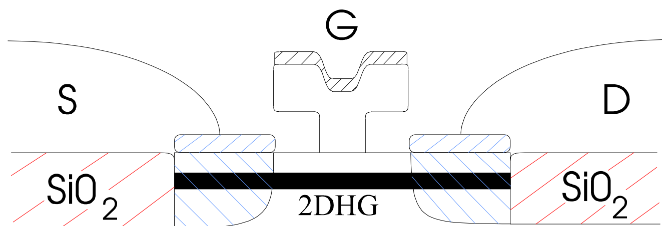
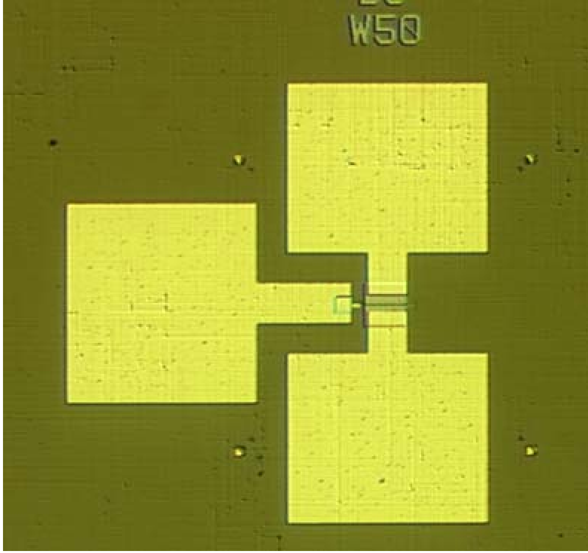


Fig. 21. Device fabrication steps.



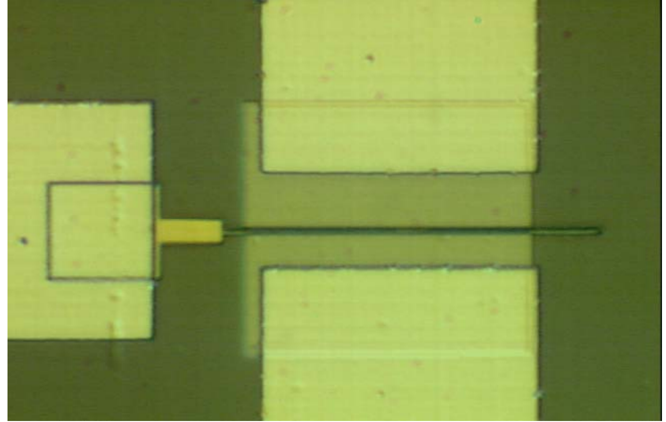
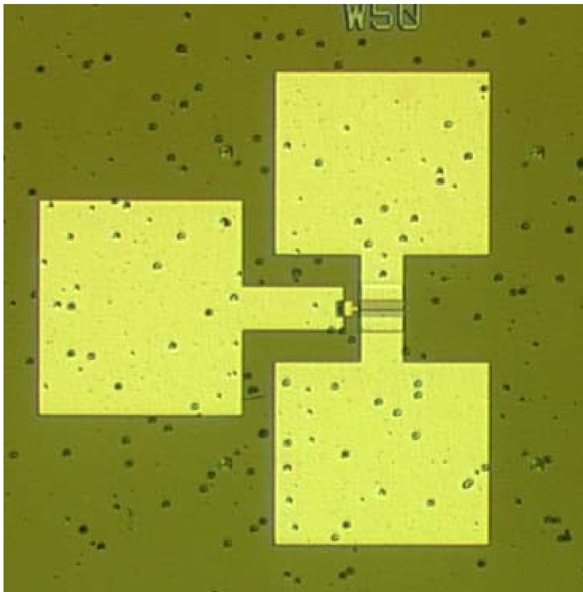


Fig. 22(a). Photo of a DC device on bulk Si.

Fig. 22(b). Photo of a DC device on bulk Si.



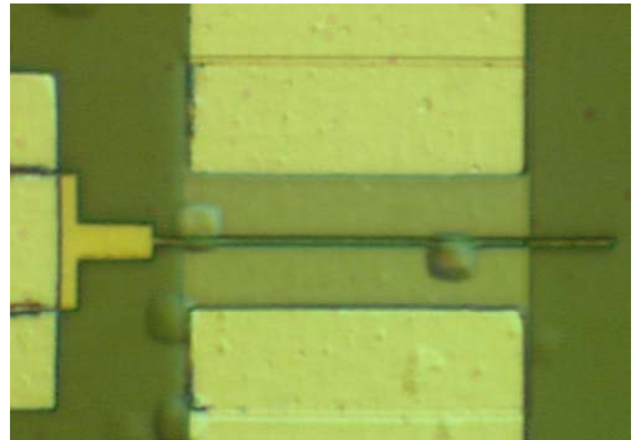


Fig. 23(a). Photo of a DC device on SOS.

Fig. 23(b). Photo of a DC device on SOS. .

A. DC Characteristics

DC characteristics were measured for devices having gate lengths, L_g, of 0.1, 0.2, 0.4 and 0.8 µm and width, W_g, of 20 µm. The DC outpit characteristics and transconductance for a 0.1 µm device are shown in Figs. 24(a) and (b). Fig. 25 shows the extrinsic transconductance as a function of inverse gate length. The DC characteristics for all these devices are summarized in Table II.

The 0.1µm devices exhibit a peak extrinsic transconductance, g_m, of 377 mS/mm at a drain-source bias, V_{ds}, of -0.6 V and a gate bias, V_g, of +0.1 V. This compares favorably to the record extrinsic transconductance of 488 mS/mm obtained from *any* Si/SiGe-based p-FET. The record extrinsic transconductance was obtained at a gate length of 0.1µm from a compressively strained *pure* Ge channel p-MODFET, fabricated using a similar technique [21]. To the best of our knowledge, these values represent new record extrinsic transconductances for any SiGe p-FETs grown on SOS substrates and show a considerable improvement over SiGe/SOS p-MOSFETs which have demonstrated a peak g_m of 77.7 mS/mm at a gate length of 1.0 µm [22]. In addition, due to the peak g_m occuring at a V_{ds} of only -0.6 V, these devices may be useful for low power, low noise applications. Furthermore, the SOS p-MODFETs show only a 30% decrease in extrinsic transconductance, from 377 to 265 mS/mm, for an 8-fold increase in nominal gate length, from 0.1 to 0.8 µm respectively. The output transconductance, is observed to decrease from 19 mS/mm to 8.2 mS/mm (at V_{ds} = -0.6 V) as the gate length is increased from 0.1 µm to 0.8 µm respectively, yielding a maximum available voltage gain of 32 at a gate length of 0.8 µm.

Table VI: Summary of the DC characteristics.

Gate length	0.1 µm	0.2 µm	0.4 µm	0.8 µm
R_{on} (mm)	1.2	1.4	1.5	
g_{out} (mS/mm) (at V_g = +0.1 V)	19.0	11.9	8.5	8.2
$g_{m,max}$ (mS/mm) (at V_{ds} = -0.6 V)	377	340	316	265
Max Gain	19.8	28.6	37.2	32.3

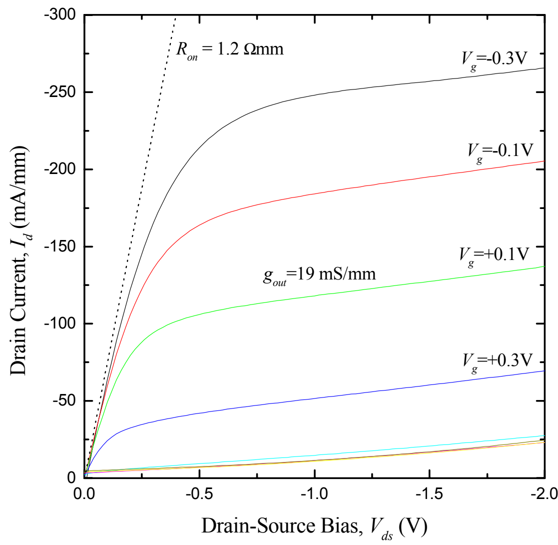


Fig. 24(a). DC characteristics for a pMODFET on SOS having a gate length of 0.1 µm.

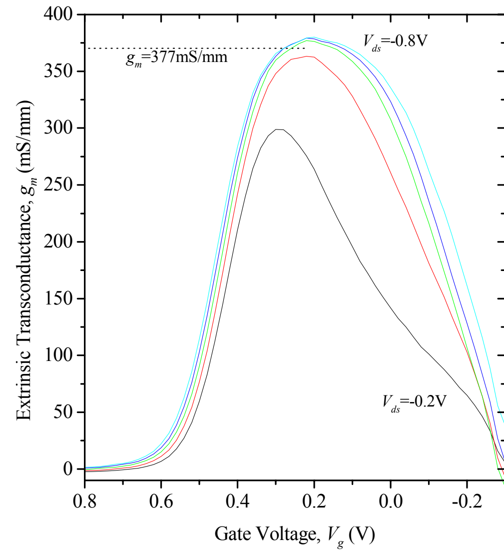


Fig. 24(b). Transconductance for a p MODFET on SOS having a gate length of 0.1 µm.

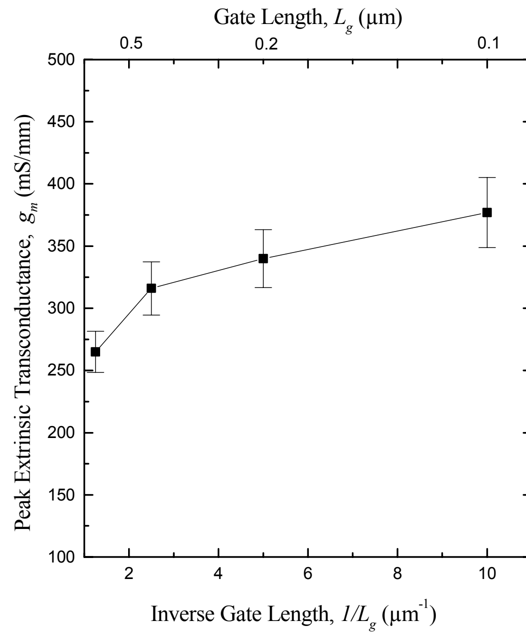


Fig. 25. Variation in extrinsic transconductance with inverse gate length for pMODFETS on SOS.

B. Microwave Characteristics

These $Si_{0.7}Ge_{0.3}/Si_{0.2}Ge_{0.8}$ pMODFETs fabricated on SiGe heterostructures grown on SOS wafers were characterized using a new 50 GHz measurement system consisting of an HP 8510B network analyzer, waveform synthesizer and *s*-parameter test kit, as well as a cascade probe station connected by 50 GHz probes and cables. The devices were tested under varying bias conditions at room temperature. Open-circuit geometries were also measured to deembed the parasitic effect of the contact pads. The results of measurements on a device with L_g = 0.1 μm and W_g = 50 μm are shown in Fig. 26. The figure shows the deembedded forward current gain, $|h_{21}|^2$, and the maximum unilateral power gain, MUG, plotted vs frequency for V_{gs} = +0.3 V, and V_{ds} = –1.5 V. Extrapolation of the data shows f_T = 49 GHz and f_{max} = 114 GHz. To our knowledge, this f_{max} value is the highest ever reported for a SiGe p-type field effect transistor.

The results of the small-signal extraction as shown below in Fig. 27. The s-parameters calculated from this small-signal equivalent circuit agree very well with the measured data up to 50 GHz, as shown in Fig. 28.

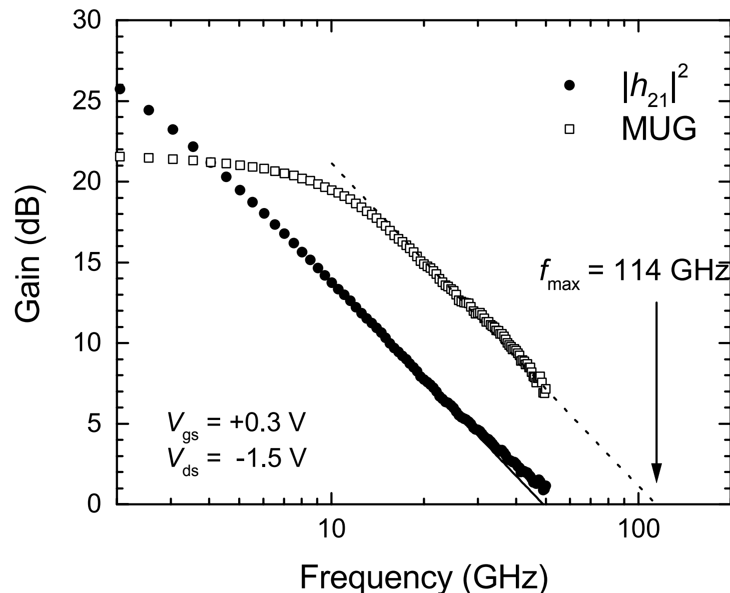


Fig. 26. $|h_{21}|^2$ and MUG plotted vs frequency for a 0.1 x 50 μm^2 pMODFET on SOS measured up to 50 GHz.

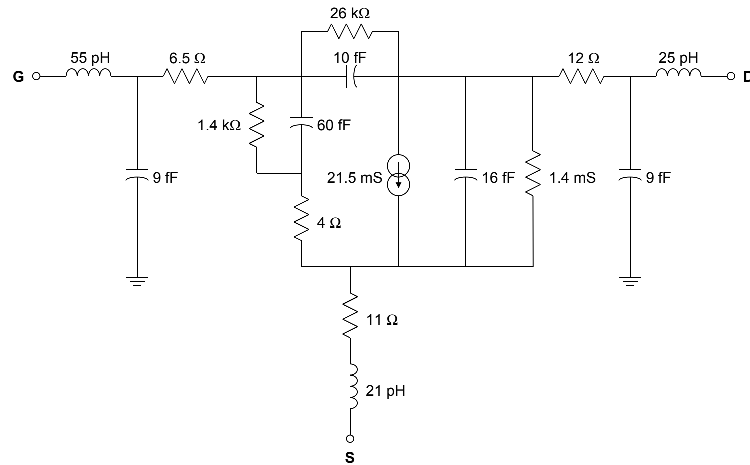


Fig. 27. Small-signal equivalent circuit for a 0.1 x 50 m^2 pMODFET on SOS extracted from the raw (non-deembedded) s-parameter data.

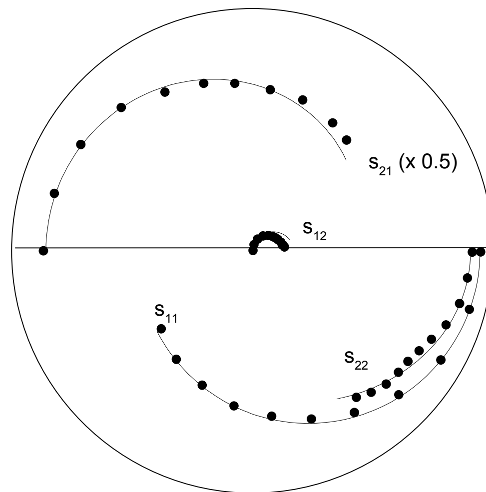


Fig. 28. Plot of *s*-parameters for same pMODFET at frequencies from 0 to 50 GHz. Circles: experimental data, lines: values calculated from small signal equivalent circuit.

C. Noise parameter characterization of p-MODFETs on SOS

The p-MODFETs fabricated on SiGe heterostructures grown on SOS wafers were characterized at IBM Burlington using a standard noise parameter measurements at frequencies ranging from 3 to 26 GHz. The devices were tested under varying bias conditions at room temperature to determine the optimum bias conditions for low noise operation. The devices were tested "as is", meaning no deembedding of the contact pads was performed.

The results of measurements on a device with L_g = 0.1 µm and W_g = 90 µm are shown in Fig. 29. The figure shows the minimum noise figure, F_{min}, and the associated power gain, G_a, plotted vs frequency for V_{gs} = +0.3 V, and V_{ds} = –0.6 V. The plot indicates that excellent noise figure values can be obtained, particularly at high frequencies. For instance, values of F_{min} = 2.5 dB and G_a = 7.5 dB were obtained at 20 GHz. Combined with our previously reported results of f_{max} > 100 GHz, these results clearly demonstrate the performance potential of SiGe MODFETs on sapphire.

In order to understand the results more clearly, the bias dependence of the noise figure was investigated. The results are shown in Fig. 30, where F_{min} is plotted vs V_{gs} at two different frequencies (3 and 26 GHz), for a constant drain bias of -0.6 V. The plot shows that the optimum bias condition for minimum noise figure changes with frequency. At 20 GHz, the lowest minimum noise figure occurs at V_{gs} = + 0.3 V, while at 3 GHz, the lowest value occurs at V_{gs} = 0. Fig. 30 also shows the dc gate leakage current on the same plot as F_{min}. The plot clearly shows that the noise figure at 3 GHz follows the same trend as the gate leakage current. Therefore, we conclude that the low-frequency noise figure is significantly influenced by the dc gate current, and that even lower noise figures could be obtain if the gate current can be reduced. This is an encouraging result, since the Si control devices fabricated along with the SOS devices showed over an order of magnitude reduction in the gate current, presumably due to the reduced dislocation density in these devices. Therefore, further improvement in the quality of the starting SOS material should directly lead to improved noise performance.

In this section we have described the fabrication scheme for SiGe pMODFETS and reported device results for the first SiGe pMODFETS fabricated on sapphire substrates. These devices have transconductances as high as 377 mS/mm, f_t equal to 50 GHz and f_{max} of 114 GHz. The latter is the highest value ever reported for a SiGe p-type field effect transistor. The 20 GHz the minimum noise figure is 2.5 dB with associated gain of 7.5 dB.

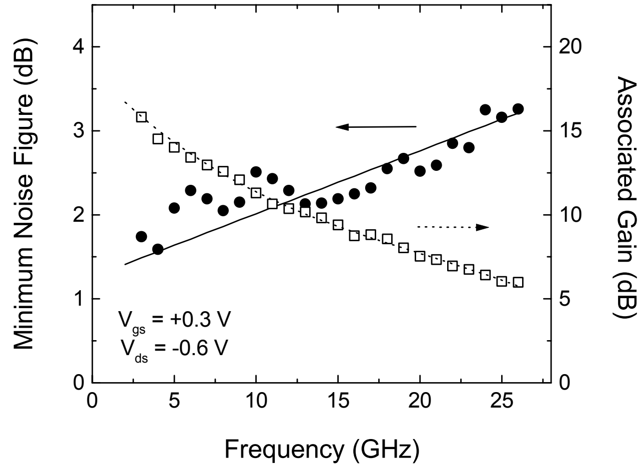


Fig. 29. Minimum noise figure and associated gain plotted vs. frequency for a 0.1 x 90 μm^2 p-MODFET on SOS.

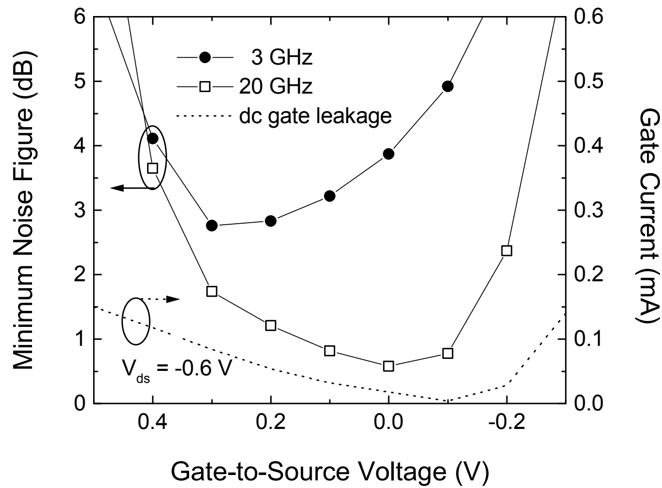


Fig. 30. Minimum noise figure and gate current plotted vs. V_{gs} for same device as in Fig. 29. The plot shows the correlation between F_{min} at 3 GHz and the DC gate leakage correlation between F_{min} at 3 GHz and the dc gate leakage.

VI. Second device fabrication run: pMODFETs on bulk Si

The DC characteristics of high-performance SiGe p-MODFETs grown by UHV-CVD epitaxy on silicon-on-sapphire substrates were discussed in the previous section, as were microwave measurements (up to 50 GHz) on devices from the same wafer. SOS devices with L_g = 0.1 μm displayed unity current gain (f_T) and unilateral power gain (f_{max}) cutoff frequencies of 49 GHz and 114 GHz, respectively. The latter is the highest value ever reported for a SiGe p-type field effect transistor. However, the value of f_T was lower than previously reported values for SiGe pMODFETs of comparable nominal gate length [9-12]. The primary difference between the device layer structures used by Arafa, et al. and those on the SOS wafer was the thickness of the SiGe cap layer. We therefore undertook another device fabrication run using a modified pMODFET layer structure grown on bulk Si aimed at increasing f_T.

The purpose of this run was to increase the cap thickness compared to our previous devices with $d \simeq 10$ nm, in order to improve f_T by reducing the effect of parasitic source resistance. Our previous devices, had f_T = 50 GHz, though they did produce a record f_{max} of 116 GHz. Unfortunately, this run did not produce the intended results. Fig. 31 shows a plot of f_T and f_{max} vs gate voltage for a 0.1 x 100 μm^2 pMODFET fabricated on a $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}$ layer structure with a $d \simeq 20$ nm. The peak f_T and f_{max} values were only 40 and 45 GHz, respectively, despite the fact that the layer structure had slightly higher carrier mobility compared to that of our previous layer structures.

We believe that the decreased frequency performance can be explained by considering the equation, $f_T = (g_{mi}/2\pi C_g) / (1 + g_{mi}R_s)$, where g_{mi} is the intrinsic transconductance, C_g is the total gate capacitance and R_s is the source resistance. For an ideally scalable FET, both g_{mi} and C_g should be inversely proportional to the cap thickness. Therefore, f_T should increase with increasing d due to the reduction of the transconductance in the $(1 + g_{mi}R_s)$ term. Unfortunately, small-signal analysis of our previous devices indicated that this effect is actually quite small; increasing the cap thickness from 10 to 20 nm, leads to an f_T increase of only 10-15%. However, our analysis also revealed that the value of C_g in those devices was roughly 50% larger than expected from a simple parallel-plate approximation. We believe that this additional capacitance is parasitic in nature and is the cause of the reduced f_T in our devices. In fact, our calculations indicate that by increasing d from 10 nm to 20 nm, the parasitic component of C_g *increases* from 33% to 50%, leading to a *reduction* of f_T by a factor of ~1/3. Therefore, based upon our value of f_T = 50 GHz for d = 10 nm, increasing d to 20 nm should increase f_T to 57 GHz, but then be reduced by the parasitic capacitance effect to 38 GHz, in close agreement with our experimental value of 40 GHz. One possible way of eliminating this parasitic capacitance could be to utilize a thin SiGe on sapphire substrate, where the SiGe buffer layer can be completely removed beneath the isolation regions, dramatically reducing substrate-related parasitic effects. Another method of improving f_T could be to *decrease* the cap thickness to reduce the parasitic content of C_g. Values of d = 5-10 nm should increase f_T, but below 5 nm, the $(1 + g_{mi}R_s)$ term again begins to dominate. Increasing the channel conductance to reduce R_s could relax this constraint, and provide further improvements in f_T.

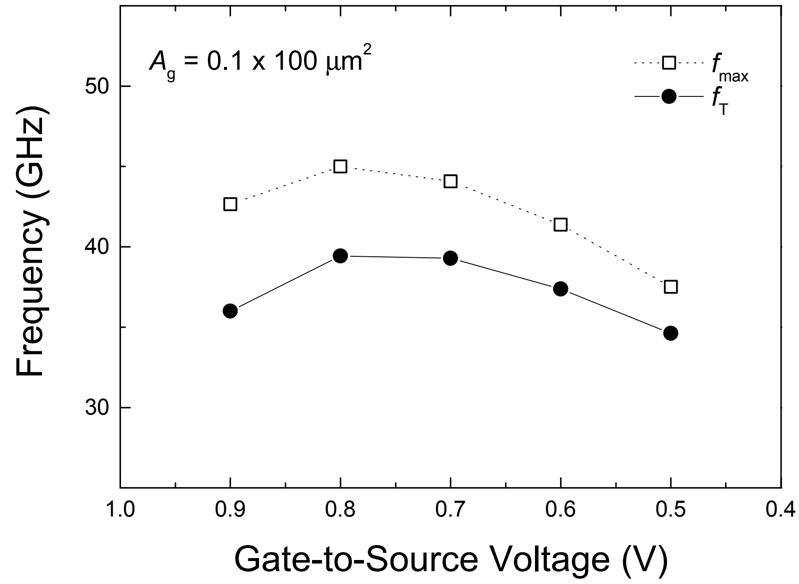


Fig. 31. Plot of f_T and f_{max} vs V_{gs} for a 0.1 x 100 μm ^{2} pMODFET on a $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}$ heterostructure with 20 nm-thick cap.

VII. pMODFET Test Site with Static Voltage Divider Circuit

A new mask set was prepared in order to fabricate a demonstration pMODFET circuit. As shown in Fig. 32, the test site consists of the static divider circuit design provided by Prof. Asbeck's group at UCSD, various discrete devices for DCc and AC characterization and process evaluation structures to measure contact resistance, gate resistance, and via continuity.

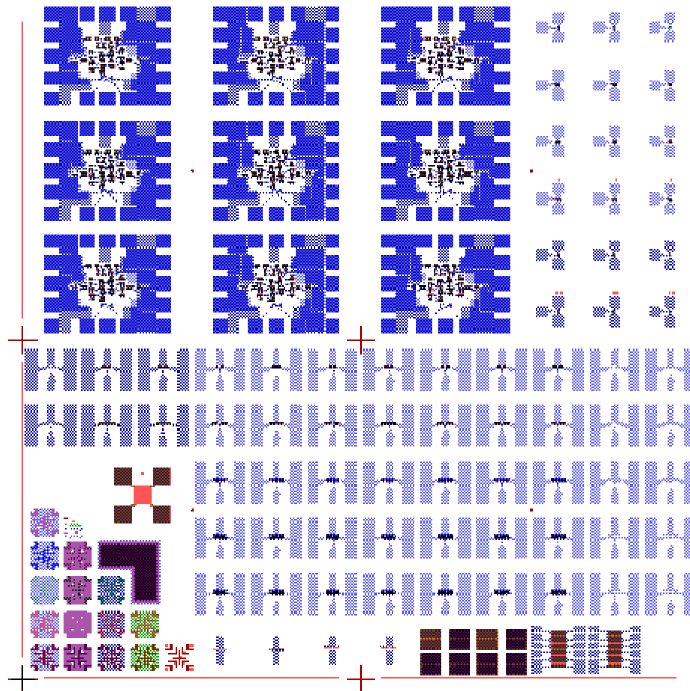


Fig. 32. Test site for SiGe pMODFET frequency-divider circuits.

VIII. pMODFET Divider Circuit Fabrication

The performance of discrete pMODFET devices is determined to a large extent by the epitaxial layer structure. While process innovations can be used to minimize the parasitics for a given device geometry, the intrinsic performance of the device is largely determined by the layer structure. Several key device parameters such as the effective mobility (which determines to a large extent the high frequency performance of the device) and the threshold voltage (which is critical for circuit operation) are very sensitive to the layer structure. The complex relationship between various layer parameters, e.g. thickness, doping concentration, and the device performance makes the layer structure optimization a difficult and time consuming process. As an example: the effective mobility depends on several factors such as the supply layer doping, it's distance from the high mobility channel, the depth of the quantum well forming the channel and the material quality. All these parameters need to be optimized in order to get a high effective mobility.

Apart from the epitaxial layer structure, device yield is another key issue in the realization of the pMODFET based frequency divider circuits. There have been no prior demonstrations of circuits using strained SiGe pMODFETs, and it is not obvious how the numerous threading dislocations at the wafer surface will affect device yield and characteristics. Since the entire process is being done on 4" wafers in a non-cleanroom environment, processing yield is also a serious issue. There are numerous steps in the existing process, e.g. the T-gate formation, that are inherently low yield. A divider circuit with 50 transistors requires a 98.6% device yield, in order to yield 50 % of the circuits.

The demonstration of frequency divider circuits using *p*-MODFETs requires a process with a high yield. A high yield implies not only a large fraction of working devices, but also minimal variance in device parameters, such as the threshold voltage, which play an important role in circuit design. In this section we will outline some of the key issues limiting yield in the existing *p*-MODFET process flow and describe some of the process innovations leading to the development of a high yield *p*-MODFET process.

Two circuit fabrication runs were done. The first fabrication run, based on wafers from the UHVCVD run Gov61 served as a test-bed for hitherto untried process modules that have been implemented to achieve the necessary device yield. Discrete pMODFET devices fabricated during this run had a high yield and displayed DC electrical characteristics consistent with the measured mobility in the starting material. We were, however, unable to fabricate a complete divider circuit due to an unforeseen processing problem after testing the discrete devices. Therefore a second fabrication run was done in order to complete and test the divider circuits.

As discussed in section V, we had previously achieved hole mobilities of ~900 cm^2/V-s, with the layer structure shown in Fig. 20. This layer structure also resulted in depletion mode (i.e. normally ON) pMODFET devices, which is crucial to divider circuit

performance. The impact of the threshold voltage on the divider circuit performance will be discussed in more detail later in this report. Several growth/characterization iterations were done to replicate the structure shown in Fig. 20. However, the wafers (Gov61) had relatively low hole mobility, $\mu \sim 475$ cm^2/V-s and relatively low sheet densities, $n_s \sim 8 \times 10^{11}$ cm^{-2} compared to previous values. Because the calibration of the UHCVD reactor drifts over time, it was decided to use these wafers for process development and wait until SOS and or SGOS wafers became available before doing further work to optimize the pMODFET layer structure. Additional layer structures (Gov66A and Gov67A) grown for a second circuit fabrication run had a hole mobility of ~550 cm^2/V-s and sheet carrier density of $\sim 3 \times 10^{12}$ cm^{-2}. The temperature dependent Hall mobility data for one of these wafers is shown in Fig. 33.

Fig. 34 shows a cross-sectional TEM image of the pMODFET layer structure. As indicated on the figure, these layers are thinner than the layers in the targeted structure. This partially explains the lower mobility in these samples. A thinner SiGe quantum well results in less confinement and hence a larger parallel conduction path resulting in lower effective mobility. The thinner cap layer also results in the less positive threshold voltages observed in the fabricated pMODFETs.

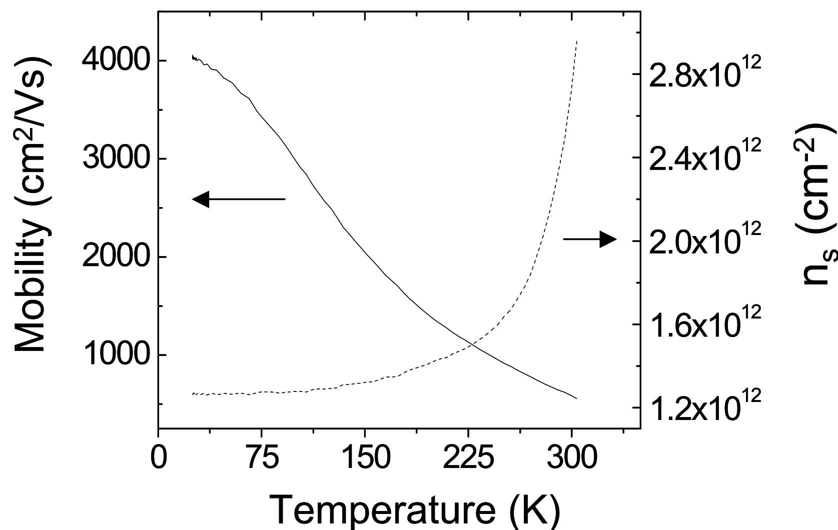


Fig. 33. Measured hall mobility and sheet density vs. temperature for wafer Gov67.07.

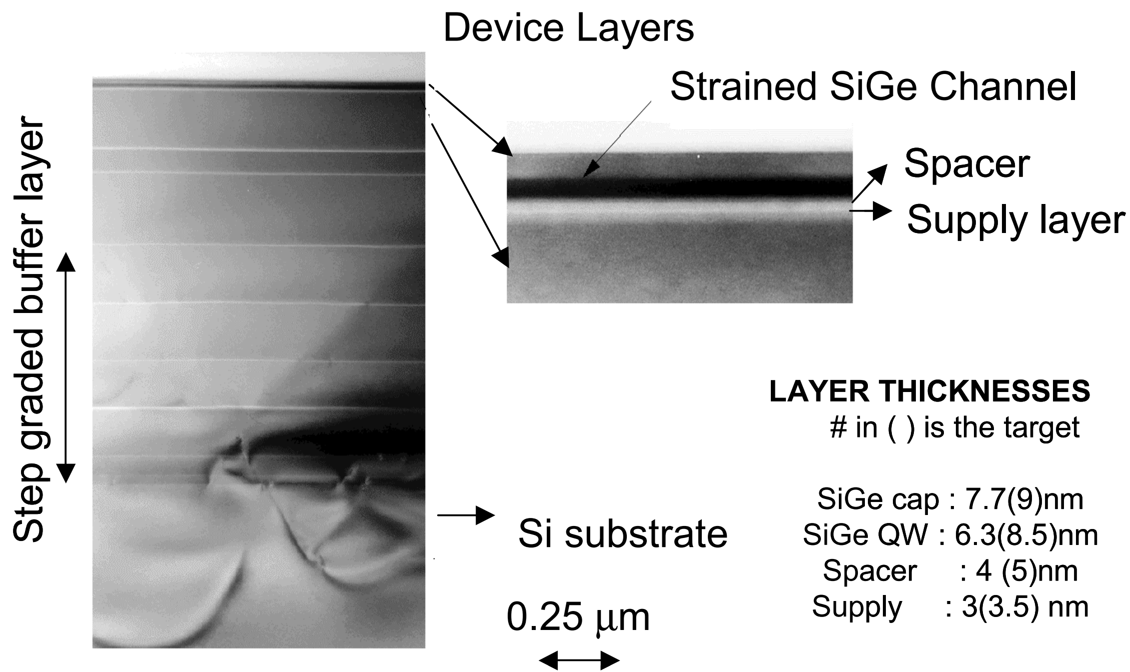


Fig. 34. Cross-sectional TEM image of wafer Gov64.07grown under identical conditions as wafers Gov66.10 and Gov67.11 that were used for fabricating the divider circuits. The target layer thickness is given in parentheses next to the measured thickness.

A. Yield issues affecting circuit fabrication

The processing runs completed previously produced individual working p-MODFET devices. However several processing issues affecting device yield precluded the demonstration of a functioning frequency divider circuit. Fig. 21 shows the original process flow for fabricating pMODFET devices. This does not include the back-end processing for incorporating the second metal level that is required for the divider circuit. The key yield limiting steps in the process have been identified and are described below.

T-Gates:

While the shape of the T-gates (Fig. 35) is crucial to obtaining good device performance, it compromises their mechanical stability, especially as the gate length is scaled. This problem is further exacerbated by the necessity of doing an HF dip prior to the evaporation of Pt for the source/drain contacts. The undercutting of the T-Gates by HF, as shown schematically in Fig. 36, poses a serious yield issue as well as an obstacle to scaling the gate length. Repeated processing of the wafers was also found to rapidly degrade the T-gate yield. In earlier process runs there were problems aligning the metal

contacts to the T-Gates and repeated lithography attempts resulted in the loss of a significant fraction of the T-gates.

Source/Drain silicide formation:

The Pt for the source and drain silicide regions is patterned using a lift off process. However the current lift-off process often results in lift-off flags or ears causing the source and gate to short. Additionally, the lift-off flags often peel off during processing, resulting in shorts between adjacent devices. Hence this seriously limits the yield of the devices. Figure 37 shows an SEM image of the lift-off flags formed around the periphery of the Pt layer.

B. Process development to improve yield

Enhanced T-Gates:

In order to overcome the yield problems associated with T-gates we have implemented a novel spacer scheme using diamond-like-carbon (DLC) that protects the delicate neck of the T-Gate. This scheme not only protects the T-gate from chemical attack during processing, e.g. the HF dip prior to the silicide formation step, but also provides an additional degree of mechanical support to the T-gates. The efficacy of the DLC sidewall spacers in protecting the T-gates during the HF dip is clearly demonstrated in Fig. 38, which shows optical micrographs of conventional T-gates before (a) and after (b) a 20s 9:1 BOE ($HF:NH_4F$) and enhanced T-gates before (c) and after (d) a 20s 9:1 BOE dip. A large fraction of the conventional T-gates comprising a Ti/Pt/Au stack are no longer attached to the substrate, a result of the high etch rate of Ti in BOE. In contrast to the results of Fig. 38(a) and (b), all enhanced T-gates are intact and adherent to the substrate. A patent application was filed for this enhanced T-gate process on July 29, 2002 (docket #YOR920010768US1).

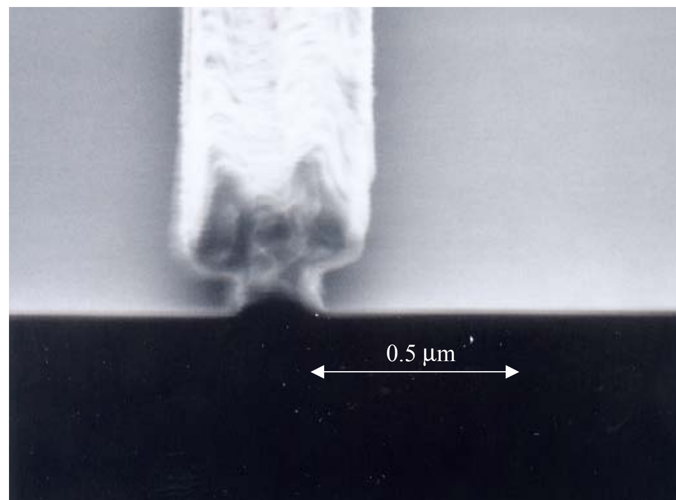


Fig. 35. SEM image of a T-gate.

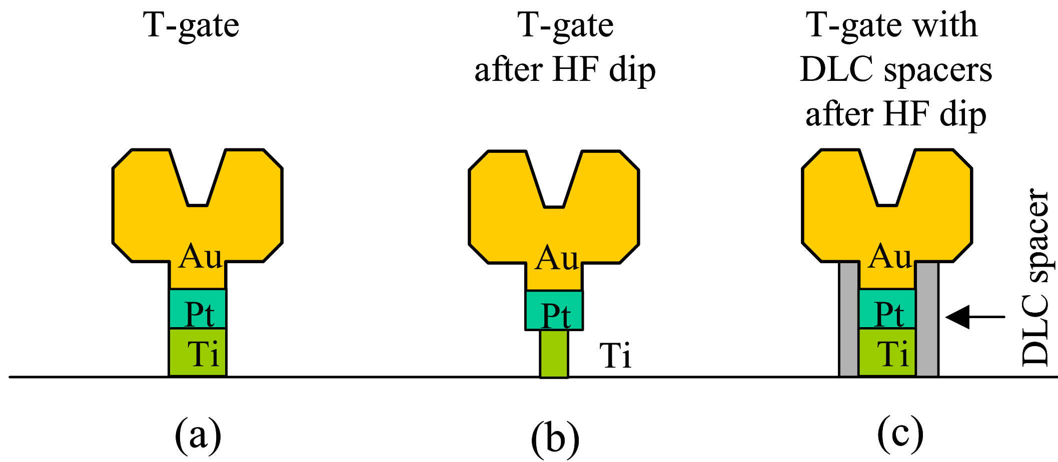


Fig. 36. Effect of an HF dip on the structural integrity of a Ti/Pt/Au T-gate with and without DLC spacers.

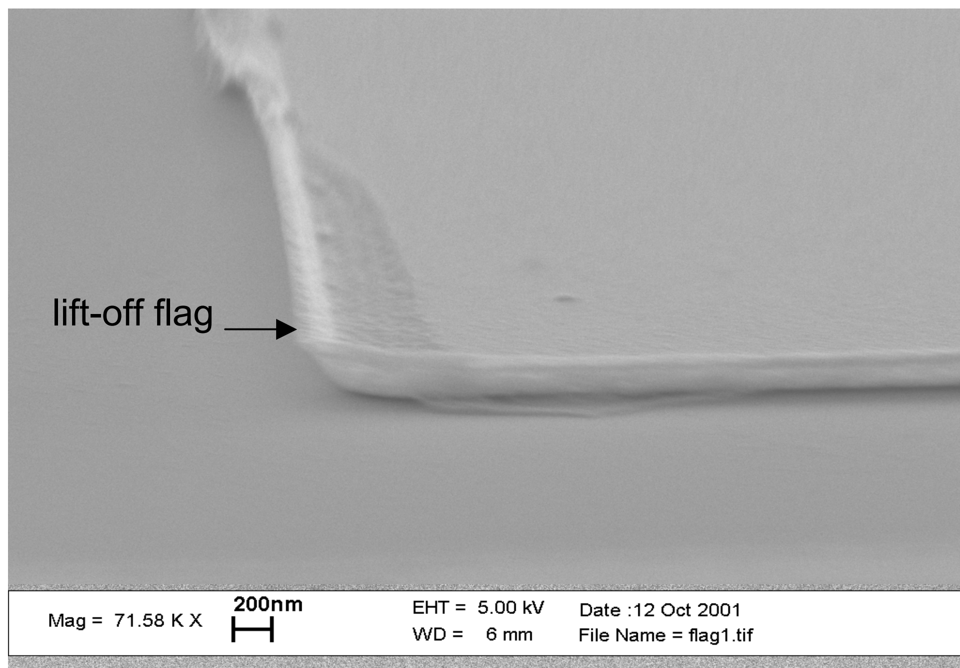
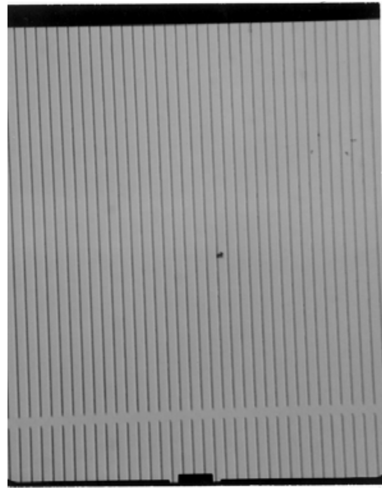
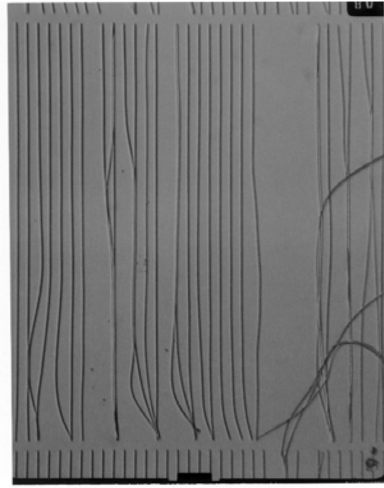


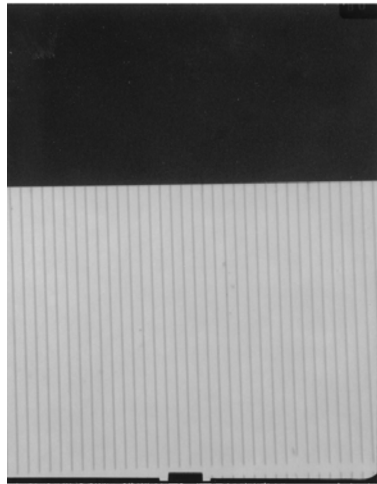
Fig. 37. Patterning the Pt by conventional lift-off processes results in lift-off flags, which are large enough to short the source and the gate, along the periphery of the Pt.



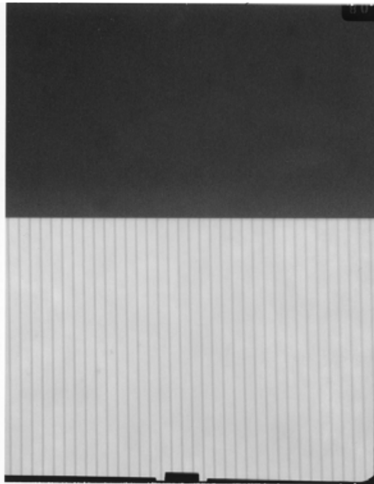
(a)



(b)



(c)



(d)

Fig. 38. Plan view optical micrographs of conventional T-gates before (a) and after (b) a 20 sec exposure to 9:1 buffered oxide etch (BOE) and T-gates with DLC sidewalls before (c) and after (d) exposure to 9:1 BOE.

Improved lift-off for source/drain silicide formation:

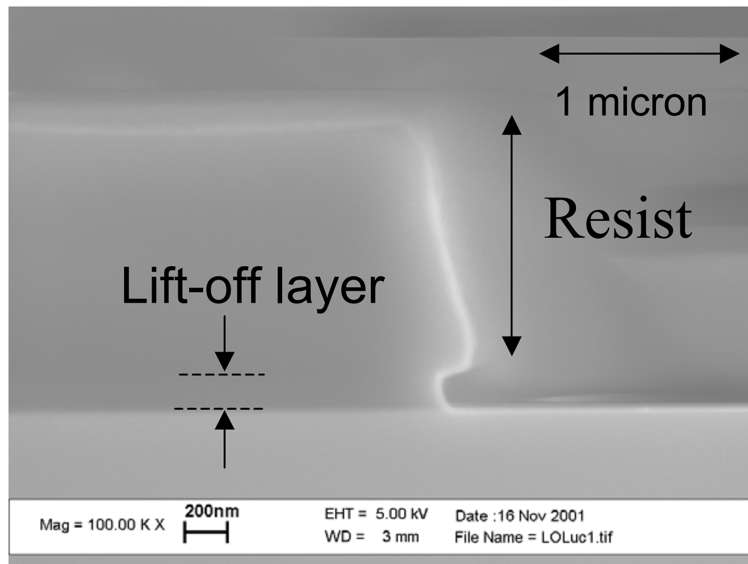
We have developed a more sophisticated lift-off process using a bilayer process in order to improve yields. This involves spinning on an enhanced dissolution rate PMGI, (microposit LOL2000) prior to spinning on the photoresist. During development the LOL2000 dissolves at a faster rate than the unexposed resist, resulting in a resist profile having an undercut. This undercut resist profile results in good lift-off's minimizing the possibility of source-gate shorts. The SEM images of the bilayer resist profile shown in Fig. 39 confirm the presence of an undercut.

Lithography issues:

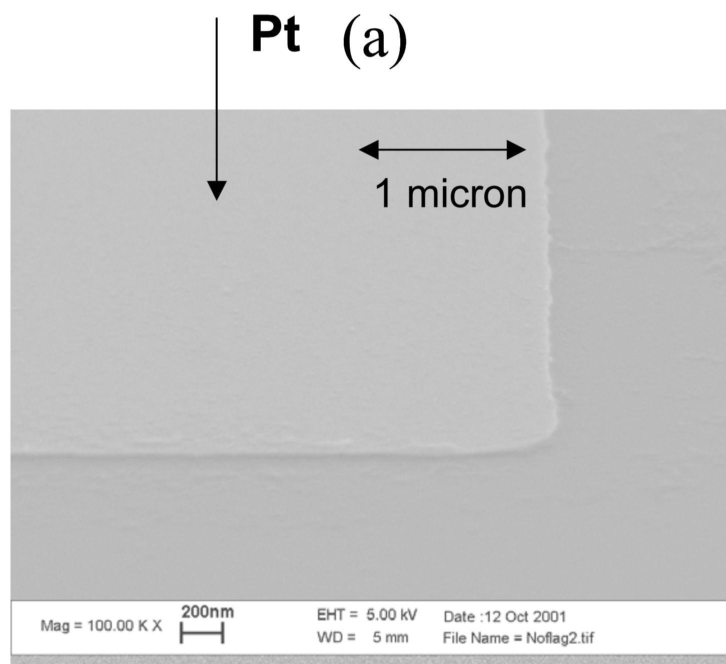
In previous process runs there were problems aligning the metal contacts to the T-Gates, due to wafer slippage during contact with the mask. In the current run we are using a projection aligner as opposed to the contact aligner (Karl Suss) used previously. This effectively solves the wafer slippage problem and results in good alignment. Fig. 40 shows a plan view SEM image of the divider circuits after the M1 level had been completed. This image shows excellent T-gate yield and alignment between various levels up-to this point.

Interconnect metal level (M2):

After device characterization at the M1 level, the wafers were further processed to include a second level of metal required for divider circuit fabrication. SICOH was used as the intermetal dielectric, and was selected due to its relatively low dielectric constant (~2.8 compared to 3.9 for SiO_2). From the point of view of minimizing parasitics it is desirable to make the intermetal-dielectric as thick as possible. This not only reduces overlap capacitance between M1 and M2, but in the case of a Si substrate also reduces the capacitance from M2 to the substrate. However, due to the limited processing capability on 4" wafers and in order to ensure a good yield, we had to use a relatively thin layer of SICOH (~200 nm). A thicker layer of SICOH requires deeper via holes and hence longer overetch times in order to ensure that all the via holes are open. This puts more stringent demands on the selectivity of the via etch to the underlying material. In addition a thicker layer of SICOH necessitates the use of a thicker back-end metal M2 in order to ensure complete filling of the via holes. Patterning and etching a thick metal layer, without reducing the lateral dimensions of the thin metal lines requires an anisotropic etch, typically a plasma etch. Unfortunately we did not have the capability for anisotropic etching of M2. Thus, the decision to use a relatively thin layer of SICOH as the intermetal dielectric was made in the interest of preserving circuit yield. Since the devices comprising the circuits are relatively slow, and not expected to result in fast circuit performance even with no interconnect parasitics, it was considered more important to ensure working circuits, thereby establishing that the material quality is sufficiently good for circuit fabrication. Fig. 41 shows a plan view optical micrograph of the fully fabricated divider circuits. This image shows excellent yield and alignment between various levels up-to this point.



Pt (a)



(b)

Fig. 39. (a) Cross section SEM of dual layer resist profile after developing. The undercut results in an excellent lift-off. (b) with no lift-off flags along the periphery.

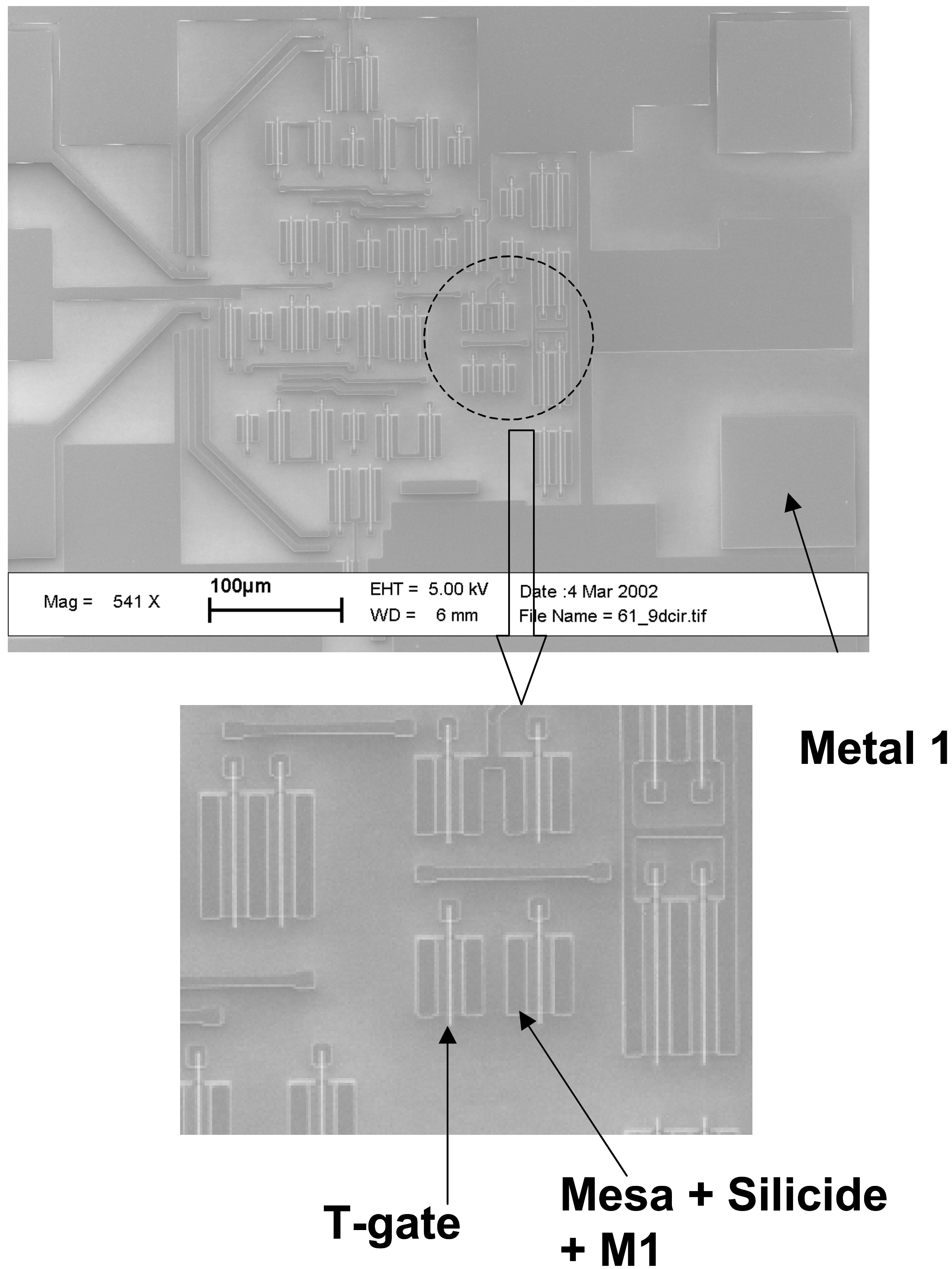


Fig. 40. SEM images of a divider circuit after completion of the metal 1 level. Excellent T-gate yield and alignment between levels is observed.

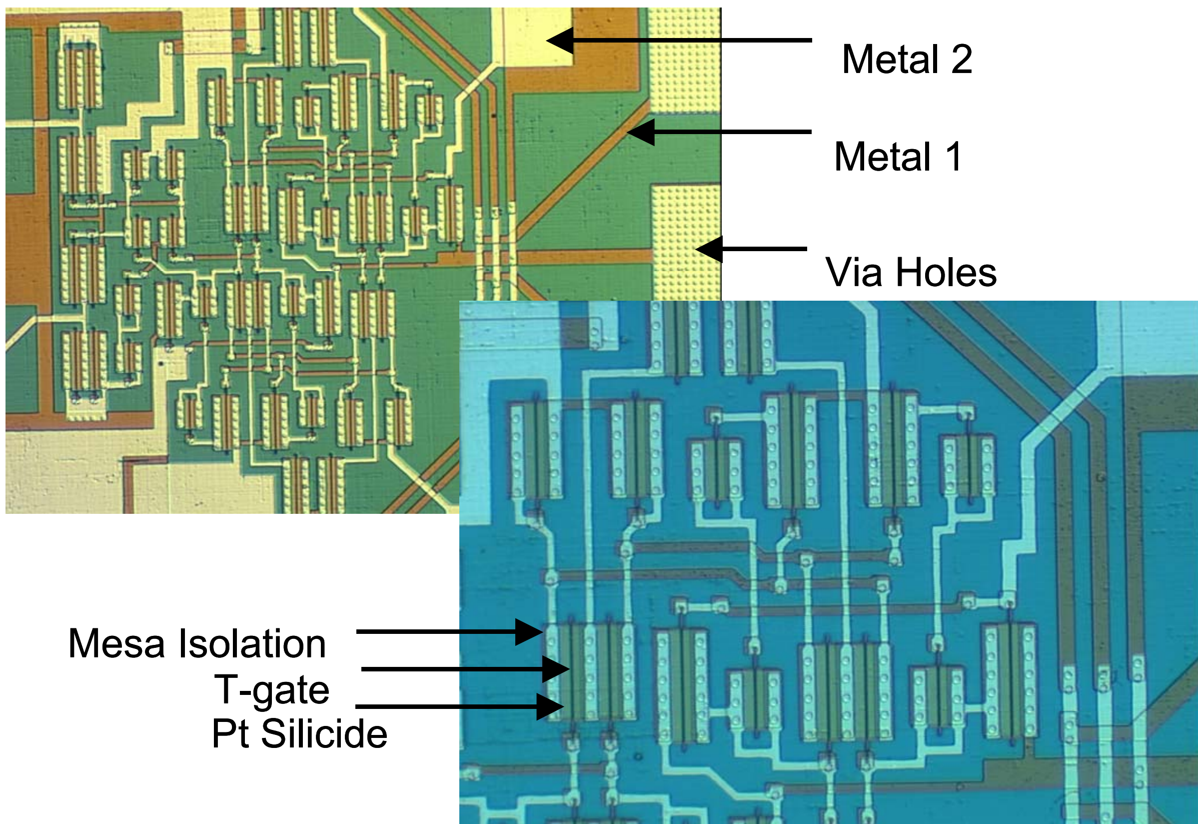


Fig. 41. Plan view optical micrograph of a fully fabricated frequency divider circuit.

IX. Electrical Characterization of pMODFET Devices and Circuits

Completed divider circuits were fabricated on wafers Gov66.10 and Gov67.11. After completion of the first metal level, M1, both the DC and AC electrical characteristics of discrete *p*-MODFET devices were measured. Characterization of discrete devices at this point provides useful feedback regarding the device performance and yield. Individual devices were measured again after completion of the M2 level and the divider circuits were electrically tested as well.

A. DC electrical characterization of *p*-MODFETs after M1

DC electrical measurements performed on discrete *p*-MODFET devices indicate good device yield (100% of 42 devices measured). This is quite significant from the point of view of circuit fabrication. Fig. 42 shows the transfer characteristics (i.e. I_d vs. V_{gs}) of a typical device. A reasonably high peak transconductance ($g_{m,ext}$) of ~300 mS/mm at V_{DS} = -0.8 V is obtained, with the peak occurring at a gate-source voltage (V_{GS}) of –0.15 V. While the measured peak $g_{m,ext}$ is lower than the record transconductance of $g_{m,ext}$ ~377 mS/mm at V_{DS} = -0.6V demonstrated by Koester et al [23], it is consistent with the lower mobility measured in these wafers (μ~550 cm^2/V-s for wafers in this run, compared to μ~800 cm^2/V-s used in prior work [23]). If one takes onto account the lower mobility and the thinner capping layer (which determines C_{gs} and hence g_m) in our samples the measured value of g_m is in excellent agreement with g_m measured on devices fabricated by Koester et. al. The average threshold voltage determined for these devices is V_t ~ 0.182 ± 0.025 V. The devices are ON at zero volts (i.e depletion mode devices), however due to the relatively thin cap layer, the threshold voltage is not as positive as in earlier devices based on the target layer structure shown in Fig. 20. This results in slower performance in the divider circuits as will be discussed later. Figure 43 shows the distribution of the threshold voltages measured for 42 devices over an area of 2 x 2 cm^2. The distribution can be approximated by a Gaussian peaked at 0.182 V and having a standard deviation of 25 mV. In-spite of the fact that several of the T-gates appear to have pits underneath them, V_t has a sufficiently narrow distribution to yield working divider circuits.

The output characteristics (I_D vs. V_{DS}) for the same device are shown in Fig. 44. The output conductance (g_o) corresponding to the peak transconductance is ~9 mS/mm, leading to a relatively large DC gain ($g_{m,ext}$/ g_o) of ~33. The gate leakage characteristics are shown in Fig. 45.

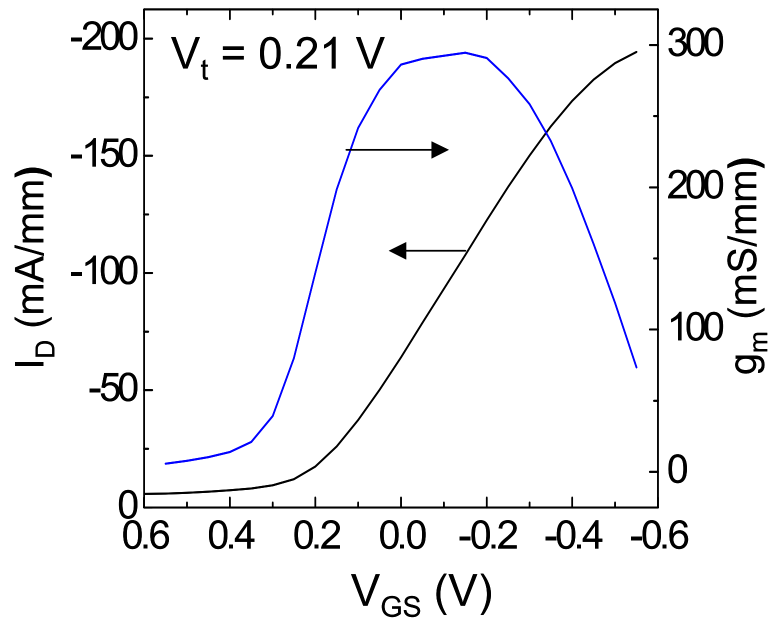


Fig. 42. Transfer characteristics (Id vs. Vg) of a device with 0.1 μm gate length and 20 μm gate width at VDS = -0.8V.

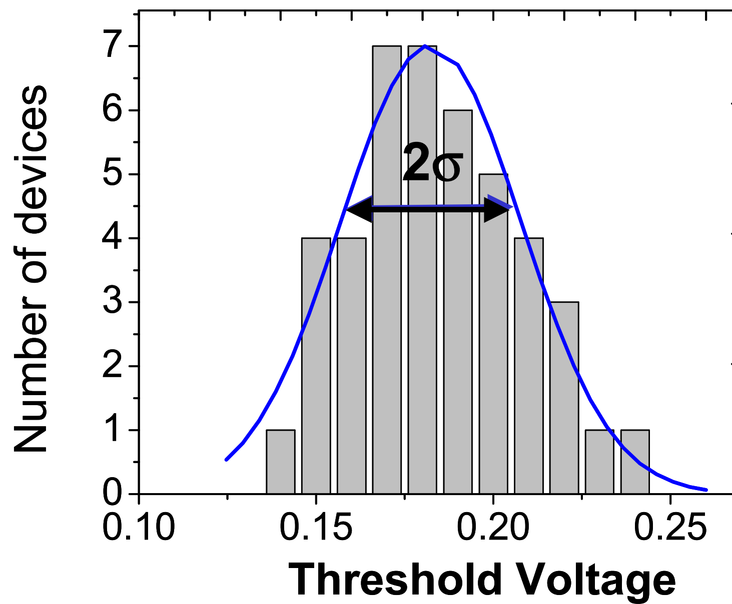


Fig. 43. Threshold voltage distribution of ~ 42 devices after the M1 level. The distribution is well approximated by a Gaussian peaked at 0.182 V and have a standard deviation of 25mV.

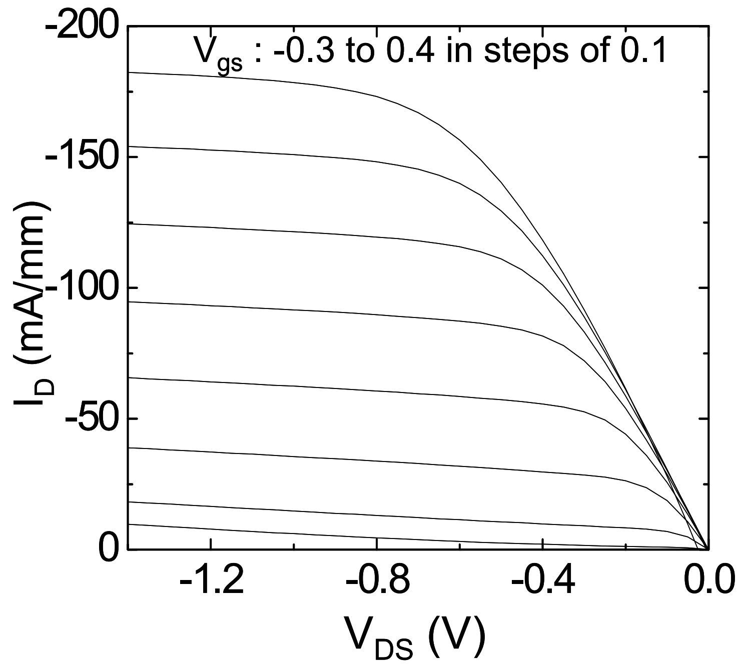


Fig. 44. Output characteristics (Id vs. VDS) of a typical device with 0.1 m gate length and 20 m gate width.

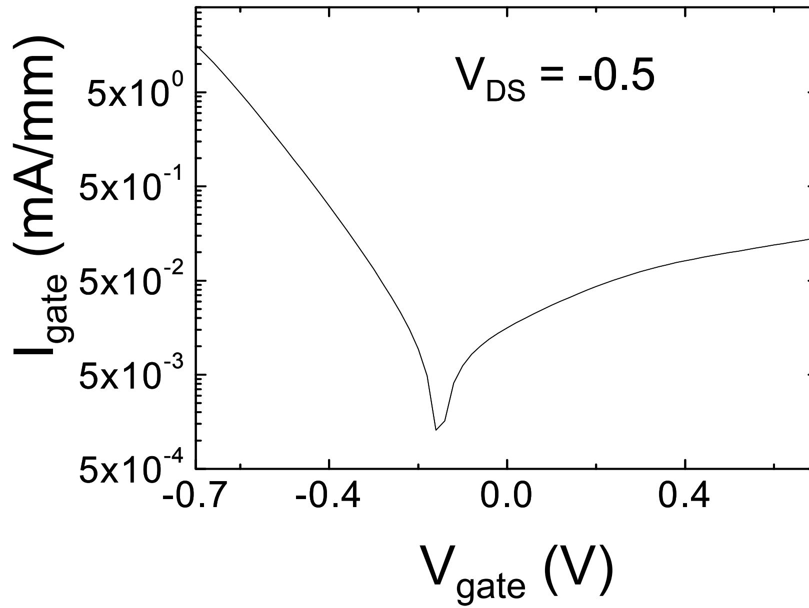


Fig. 45. Gate leakage characteristics of a typical device.

B. AC Electrical Characterization after M1

S-parameter measurements were performed on a cascade probe station using an HP8510C network analyzer for frequencies up-to 50 GHz on two-gate-finger MODFET devices with a nominal L_g = 0.15 μm and a gate width of 50μm. The frequency dependence of the forward current gain ($|h_{21}|^2$) and Mason's unilateral gain (MUG), calculated from the S-parameters after de-embedding the pad parasitics are shown in Fig. 46 and Fig. 47 for V_{gs} = -0.1 and V_{ds} = -1.0. The forward current gain ($|h_{21}|^2$) showed the expected roll-off with frequency of 20dB/decade, yielding a maximum f_t value of ~27 GHz (average was 21 GHz.). The MUG showed an anomalously sharp roll-off (>20 dB/decade) crossing unity at ~25 GHz. Fig. 48 shows a plot of f_t vs V_{gs} revealing a fairly broad peak which peaks at roughly the same V_{gs} value g_m.

Table VI shows a comparison of the measured transconductance and unity gain frequency f_t for discrete *p*-MODFET devices fabricated in this run and devices fabricated on SOS wafers earlier by Koester et. al [23]. The differences in these two quantities are consistent with the lower mobilities and altered layer structure of the samples used in this run compared to the samples described by Koester et al [23].

Table VI: Comparison of Gov66.10 and previous pMODFET devices.

Parameter	**66.10**	**Koester et al. [22]** ***IEEE EDL 2001***	**Ratio 66.10/Koester (measured)**	**Ratio 66.10/Koester (expected)**
Mobility, μ (*cm²/Vs*)	450 - 550	800	0.56 - 0.69	**NA**
Gate to Source Capacitance (C_{gs})	$\propto 1/d$ (d measured by XTEM) d is the distance of the QW from the T-gate		1.3	**NA**
Transcondustance, g_m *(mS/mm)*	300	388	0.77	0.72 - 0.90
Cut-off frequency, f_t *(GHz)*	28	50	0.56	0.55 - 0.69

C. AC Electrical Characterization after M2

After completing the M2 level we repeated S-parameter measurements on the discrete p-MODFET devices. The frequency dependence of the forward current gain ($|h_{21}|^2$) and Mason's unilateral gain (MUG), calculated from the S-parameters after de-embedding the pad parasitics for two finger devices (L_g = 0.15 µm and width = 50 µm) are shown in Fig. 46 and Fig. 47. It is found that the devices have a significantly lower f_t and f_{max} subsequent to the M2 process compared to devices measured after the M1 level. The maximum value of f_t was 21 GHz (average was 17 GHz) and the maximum value of f_{max} was 25 GHz respectively. The backend process probably adds a small series resistance, resulting in a lower value of the extrinsic transconductance. However based on estimates of the intrinsic series resistance of the device (dominated by the resistance of the high mobility channel between the source silicide and the gate) we believe that the additional series resistance between M1 and M2 will result in only a marginal decrease in g_m (< 5 %) which does not account for the lowering in f_t by almost 20 %. A likely cause of the decreased performance of the devices is increased parasitic gate capacitance. After the M2 level, the gates are surrounded by the back-end dielectric. This increases the fringing fields from the gate, which contribute to C_{gs}, but do not result in an increase in g_m. This degradation in the device performance is thus unavoidable in the present processing scheme, although more sophisticated processes can be envisioned which, leave an airgap under the overhang of the T-gate.

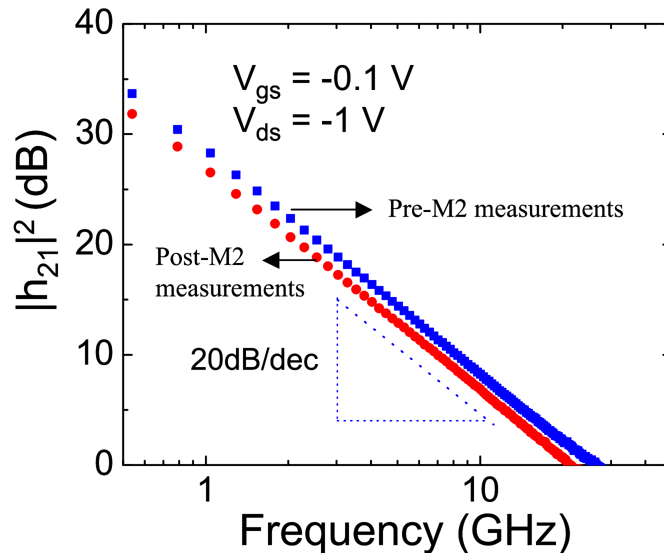


Fig. 46. Forward current gain plotted as a function of frequency for a device on wafer Gov66.10 before (squares) and after (circles) the M2 level. The intercept reveals a ft ~ 27Ghz for preM2 measurements and ft ~ 21 GHz for post-M2 measurements.

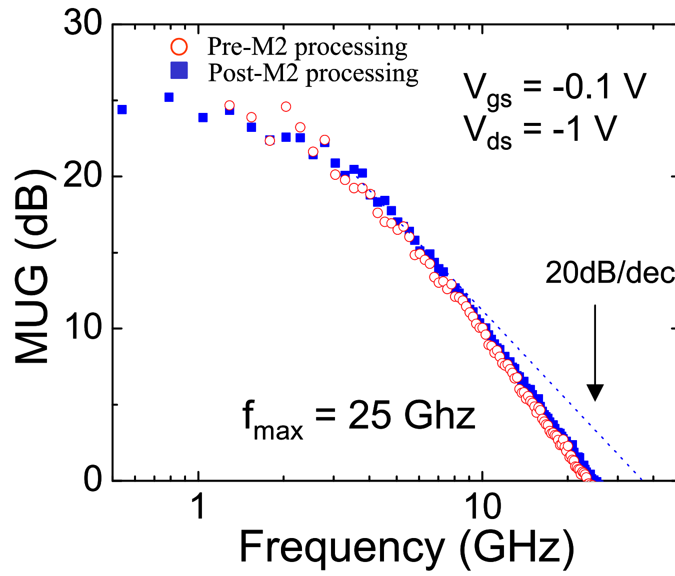


Fig. 47. Maximum unilateral gain plotted as a function of frequency for a device on wafer Gov66.10 before (open circles) and after (closed squares) M2 processing. The intercept reveals f_{max} ~ 25Ghz both before and after M2 processing.

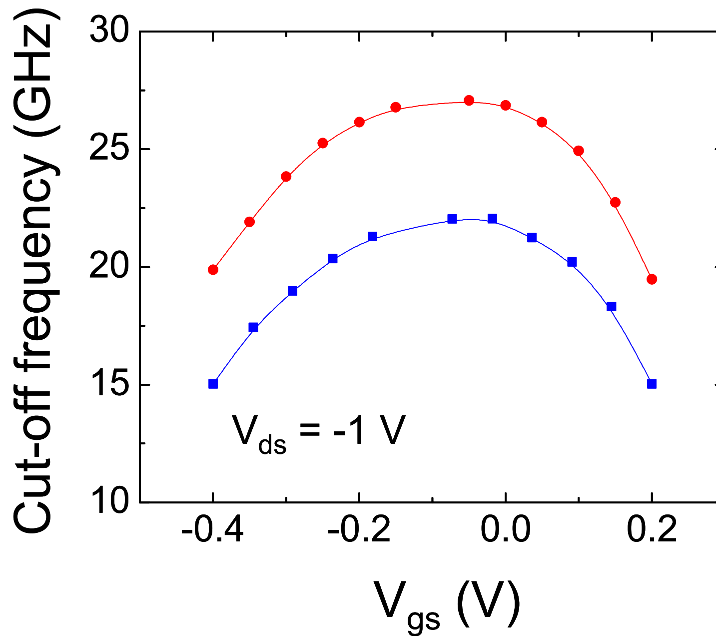


Fig. 48. Plot of ft vs V_{gs} for a device before (red circles) and after (blue squares) M2 processing.

D. Divider Circuit performance

The divider circuit is a static frequency divider that was designed in Prof. Peter Asbeck's research group at the University of California, San Diego. It consists of two cascaded latches with the *out* and *out-* outputs of the second latch connected to the *in-* and *in* inputs of the first latch. In addition to a main differential pair (the reading pair), the latches contain a cross-connected transistor pair or latching pair. The reading pair and the latching pair are driven by different phases of the clock. It is important to point out that the circuit design does not contain any resistor layers, instead it uses gate-to-source shorted MODFETs as active loads. Thus it is essential that the transistors be depletion mode devices (i.e ON for $V_{gs} = 0$). In fact circuit simulations using SPICE suggest that for the design layout in our present mask set, devices having a threshold voltage close to 0.3V result in faster circuits than if $V_t = 0.18$ V as is the case in our devices.

The circuit measurements were performed on-wafer, using high-speed signal-ground-signal (SGS) probes for the clock input and the divide-by-two output. The DC power supply probes were filtered using bypass capacitors close to the probe tip. The measurement set-up for the divider circuit is shown in Fig. 49. An HP8350B sweep oscillator was used to generate the clock input. The signal was then split and one of the split signals was phase shifted 180° with respect to the other. These were then fed to the *clock+* and *clock-* inputs of the frequency divider using matched transmission lines. The divide-by-two output was measured using a LeCroy WaveMaster 5 Ghz oscilloscope. The maximum frequency of operation for the divider circuit was found to be 3 GHz . Figure 50 shows the clock input and the divide-by-two output of the circuit at 3 GHz. At this frequency the DC power consumption of the circuit is 155 mW.

Although these circuits are slower than divider circuits demonstrated using technologies such as NMOS [24], they do represent the first circuits built using pMODFETs. In order to gain a better understanding of the impact of device characteristics, and interconnect capacitance on circuit performance, we have carried out SPICE simulations in conjunction with device-modeling studies in MEDICI [25]. Device and circuit modeling discussed in the following section show that the divider circuit speed can be considerably improved by optimizing the device layer structure as well as minimizing the parasitic components in the backend process.

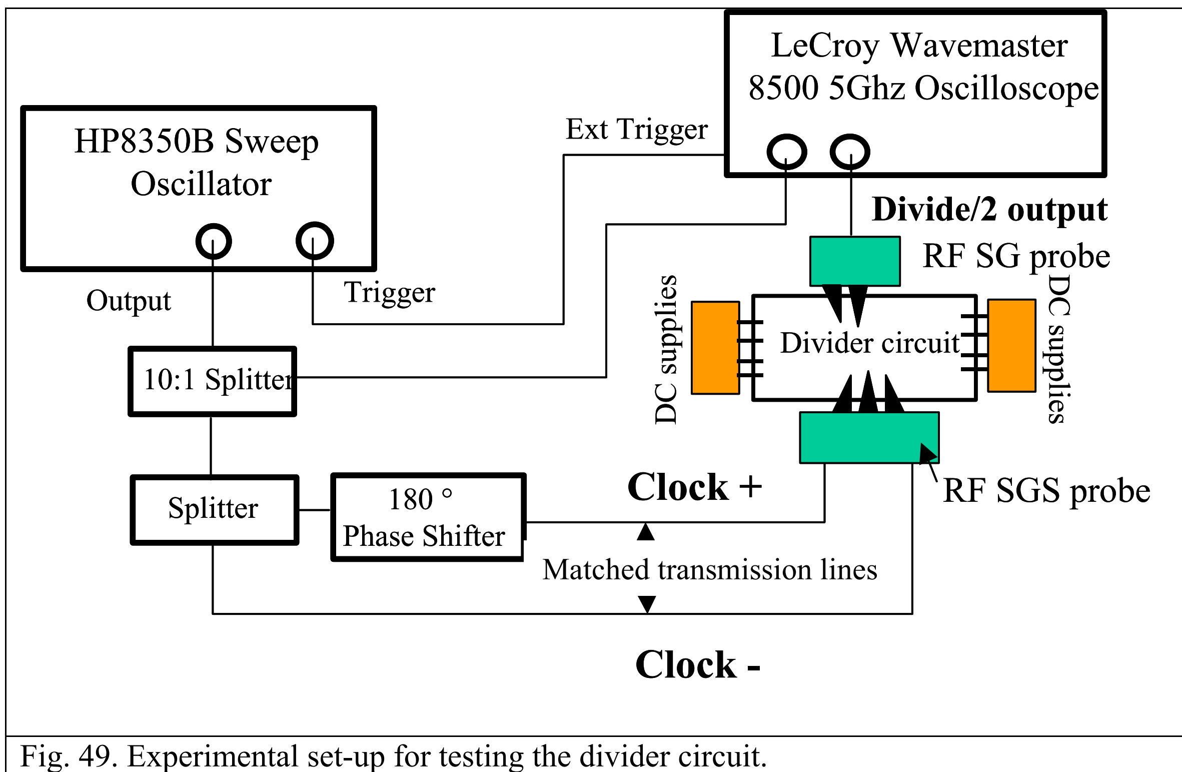


Fig. 49. Experimental set-up for testing the divider circuit.

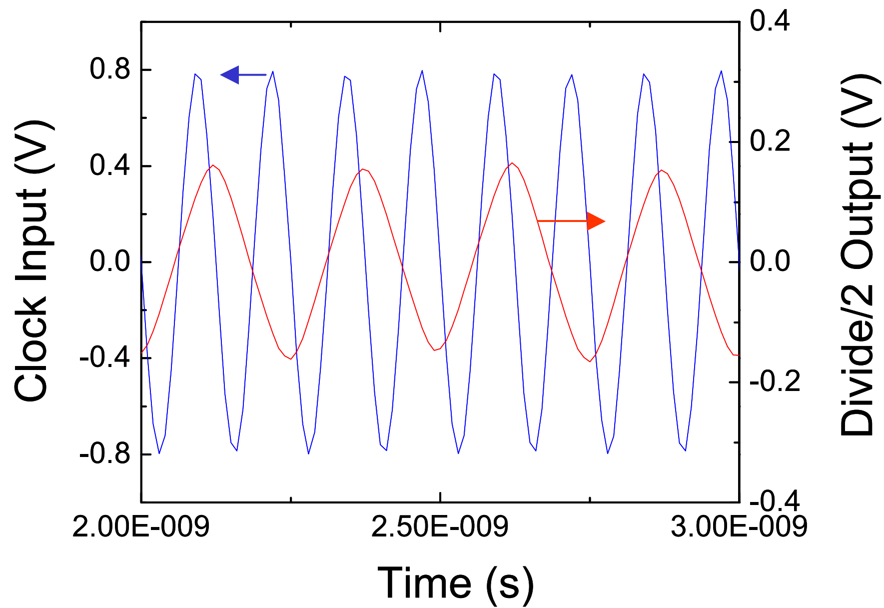


Fig. 50. Oscilloscope trace of the clock input (@ 3GHz) and the divide by 2 output from the frequency divider.

X. Divider Circuits: Simulations

Accurate simulations of circuit performance in SPICE rely on creating good models for simulating both the DC and AC characteristics of the discrete devices comprising the circuit. We have used the Statz model (which is the most complete model available in SPICE for MESFETs) for simulating the device characteristics. The DC parameters for the Statz model [26] were determined by fitting the SPICE model to the measured output characteristics of the pMODFETs, using the criterion of least squares fit. Figure 51 shows a comparison of the measured DC output characteristics and the predictions of the SPICE model for a typical device after M2 metallization. The parameters for the AC model were extracted by fitting the measured V_{gs} dependency of the unity gain cut-off frequency (Fig. 52).

Due to the relatively thin field oxide and thin intermetal dielectric (SICOH) in our process, we expect the parasitic capacitances due to the interconnect wiring to significantly slow down the circuit. In the SPICE simulations we have accounted for the parasitic capacitances from metal 1 (M1) to the substrate, metal 2 (M2) to the substrate and between M1 and M2. The dielectric constant for SICOH was assumed to be 2.8. The SPICE simulations are in excellent agreement with the measured circuit performance, predicting a maximum speed of ~ 3.4 GHz. The good agreement between the simulations and the measurements lends credence to the accuracy of the underlying SPICE models of the discrete devices. In order to isolate the effects of the parasitics on circuit performance we have simulated the circuit performance without any parasitic capacitances. This results in a maximum predicted frequency of operation of 6.3 Ghz, emphasizing the need for a "real" back-end process with low parasitics and a high resistivity substrate (e.g sapphire).

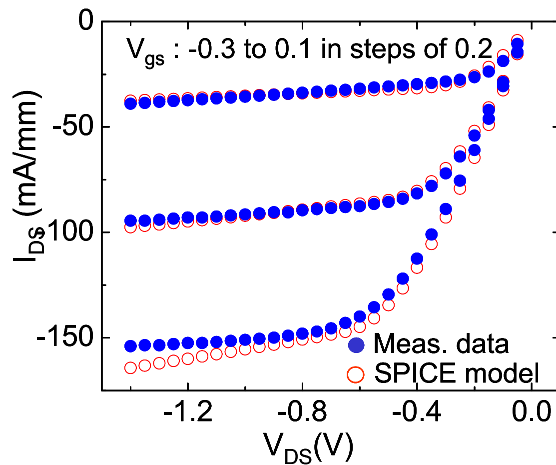


Fig. 51. Comparison of the measured output characteristics of a typical device with the output characteristics generated by the SPICE model.

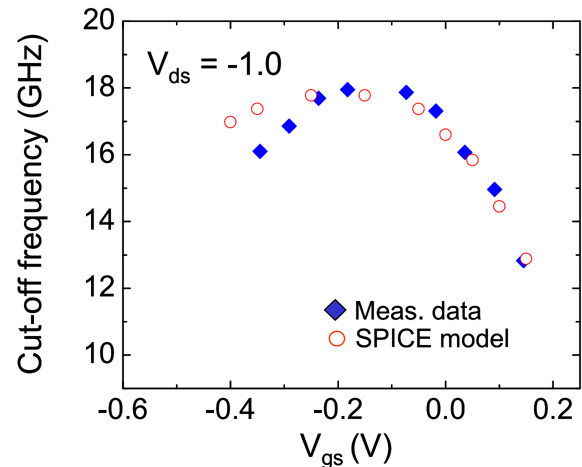


Fig. 52. Comparison of the measured *ft vs Vgs* dependence of a typical device after M2 processing and the *ft vs Vgs* dependence predicted by the SPICE model.

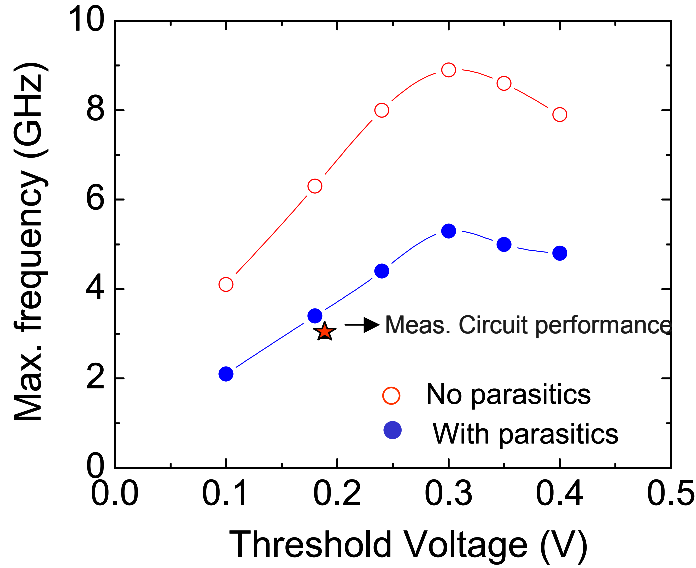


Fig. 53. SPICE simulations of divider circuit performance as a function of the threshold voltage (keeping other device characteristics the same). In order to estimate the impact of interconnect parasitics, simulations were performed with (solid circles) and without (open circles) the parasitic capacitances associated with interconnect wiring. The backend used in the current process was used to estimate the parasitics. Devices in this run have a threshold voltage of 0.18 V, and the *measured* divider circuit performance based on these devices is indicated by the start symbol.

Circuit performance is also affected by the threshold voltage of the device (keeping other device parameters the same). The circuits in this study were designed for devices which are more depletion mode (i.e. more positive threshold voltage) than the ones fabricated in this study, resulting in slower performance. Figure 53 illustrates the impact of threshold voltage on circuit performance (in the absence of parasitics). Clearly devices with a threshold voltage close to 0.3 V operate at much higher frequencies (~9 GHz). In the previous sections we have described pMODFET devices (L_g = 0.1µm) with better high frequency performance compared to the devices fabricated in this run. Divider circuits based on these devices are expected to operate at higher frequencies.

In order to assess the performance limits of pMODFET devices, we have used a device simulator MEDICI [25] to generate the electrical characteristics for pMODFETs with different gate lengths. The various material and layer structure parameters used in the simulator were calibrated using electrical data from pMODFETs published by Koester et al [23] but with a hole mobility of 1300 cm^2/Vs, the best ever reported for this layer structure [ref.]. Fig. 54 shows a plot of the calculated f_T as a function of the hole mobility for the parameters indicated on the figure. We see that values of f_T saturate; mobility values higher than about 900 cm^2/Vs result in only small increases in f_T.

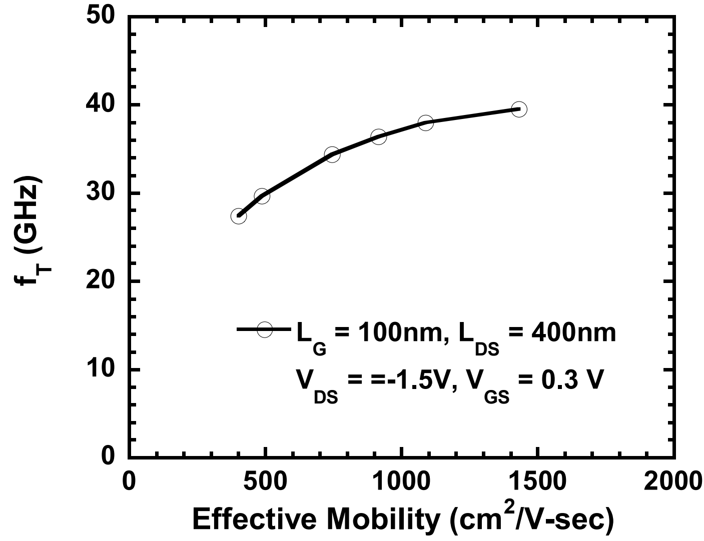


Fig. 54. Plot of simulated values of f_T vs hole mobility for the parameters indicated.

In order to minimize the parasitic capacitances in these devices we have assumed that the devices have been fabricated on thin SiGe on insulator (e.g. sapphire). The device design was scaled down to shorter gate lengths, keeping the device threshold voltage around 0.4V, for optimal circuit performance. SPICE simulations of the circuit performance vs. gate length, down to a gate length of 50 nm are shown in Fig. 55. The solid line assumes no interconnect parasitics while the dashed line assumes a backend process with 1μm of low κ dielectric (κ = 2.8) between the two levels of metal. In both cases, a sapphire substrate is assumed, thereby eliminating the capacitance between the interconnects and the substrate. Table VII summarizes the results of Fig. 55.

Another important factor that affects speed as well as circuit yield is variation in the electrical characteristics of individual devices that comprise the circuit. This distribution in device characteristics can arise due to non-uniformity in the layer structure, the presence of defects or process variations across the wafer. As discussed earlier an important parameter that impacts both circuit yield as well as maximum speed of operation is the threshold voltage, V_t. Since the V_{gs} values for peak f_t depend on V_t, a distribution in V_t will result in a slower response from some of the transistors, hus lowering the maximum operating frequency of the circuit. The impact of this on circuit performance clearly depends on whether the slower transistors lie in the critical path or not. In order to gain a better insight into the effect of V_t distribution on circuit performance, we have performed Monte Carlo simulations in which the transistors are randomly assigned a threshold voltage assuming a gaussian distribution which is centered

Table VII: Maximum frequency of circuit operation as a function of gate length under various assumptions for the interconnect parasitics.

Sample	L_g (μm)	f_t (GHz)	Maximum frequency of circuit operation (GHz)		
			No parasitics	Sapphire substrate M1-M2 1μm SICOH M1-subs 1μm SiO_2	Si substrate M1-M2 1μm SICOH M1-substrate 1μm SiO_2
66.10 (This run)	0.15	27	6.3	NA	NA
Koester devices	0.1	49	18	18	NA
Device based on MEDICI simulation	0.10	42	20	20	18
Device based on MEDICI simulation	0.075	55	27	25	19
Device based on MEDICI simulation	0.05	72	37	35	24

about the average V_t. The simulations are performed for 10 different configurations of divider circuits each with a randomly assigned set of V_t's. Results of the simulations for various values of the standard deviation, σ, are shown in fig. 58(a)-(c). SPICE models for a typical pMODFET device after M2 processing are used to perform the circuit simulations for an input frequency of 3 GHz. It is clear that for σ = 10 mV, all ten configurations function at 3 GHz, however for σ = 25 mV we see two failures out of the ten configurations, while for σ = 50 mV we observe four failures out of the ten configurations. Clearly a threshold voltage distribution with σ < 25 mV is desirable for high yield.

The modeling results based on the characteristics of the fabricated pMODFETs agree well with the measured performance of the divider circuit. Although f_t is a key parameter for circuit performance, the threshold voltage, V_t, and the uniformity of the threshold voltage are also clearly very important. The maximum predicted performance for this circuit for 0.1 μm pMODFETs is about ~20 GHz. These results also clearly show that sapphire substrates have a significant effect on circuit speed, especially for faster devices.

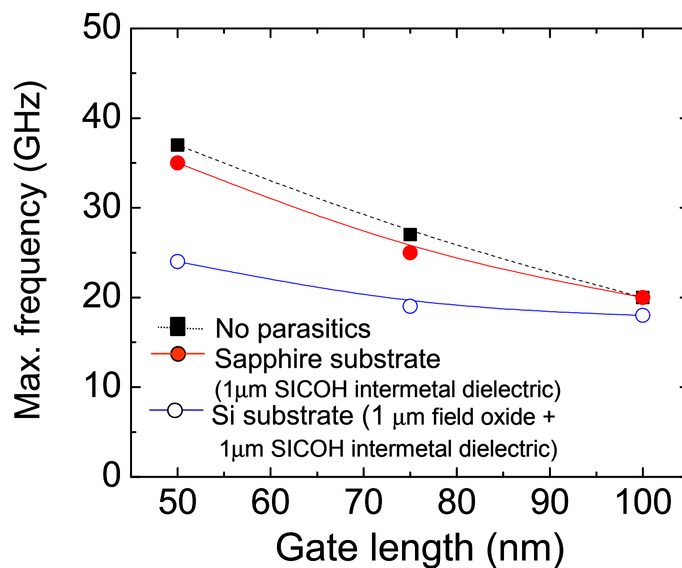


Fig. 55. SPICE simulations of divider circuit performance as a function of device scaling. The device simulator MEDICI was used to generate the device characteristics and care was taken to ensure a device threshold voltage of ~0.3-0.4 V to ensure good circuit performance. Simulations were performed assuming (a) no parasitics (closed squares), (b) a sapphire substrate and 1 μm intermetal dielectric comprising of SICOH (closed circles) and (c) a Si substrate with 1 μm field oxide and 1 μm intermetal dielectric comprising of SICOH (open circles).

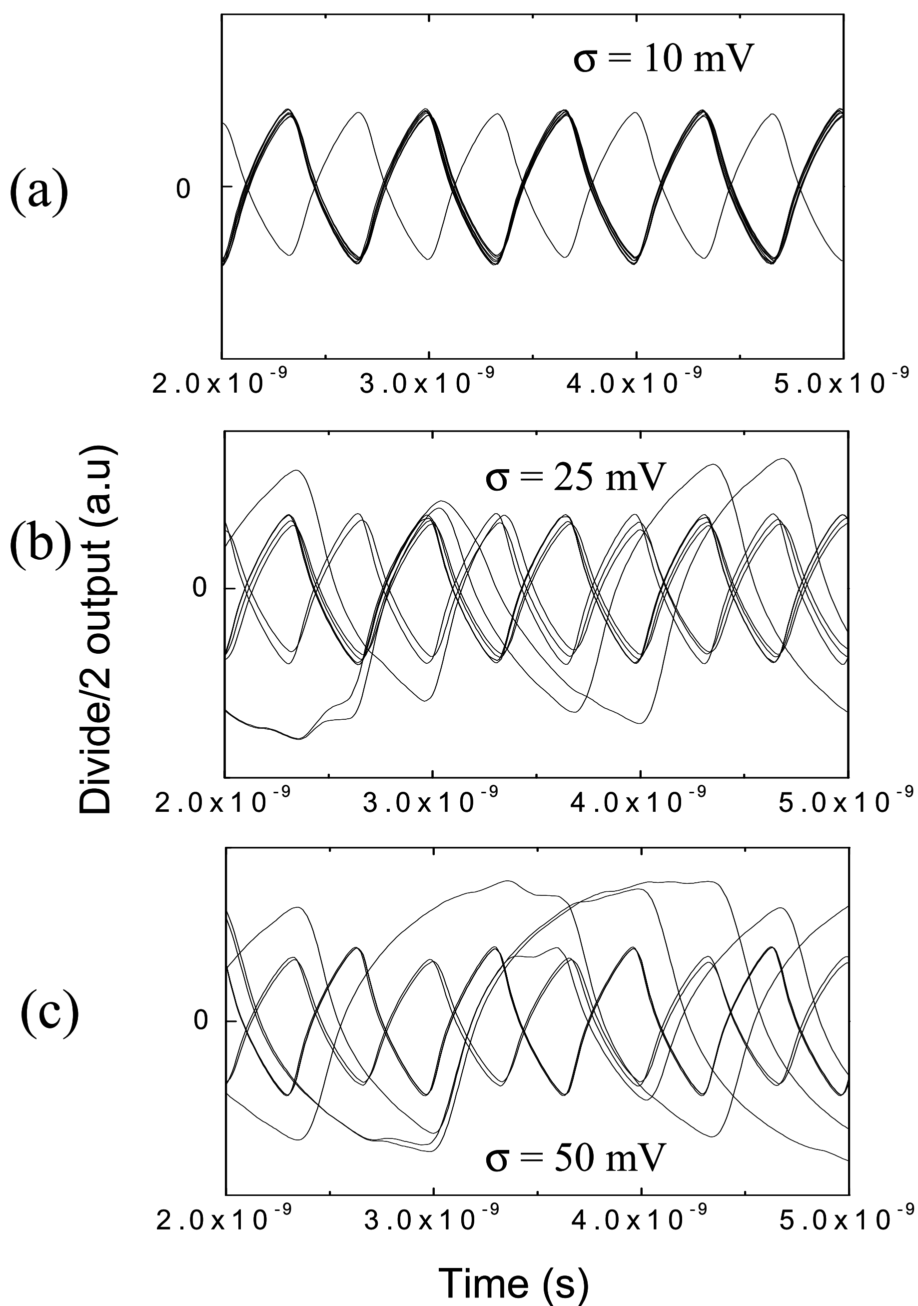


Fig. 56. Monte Carlo simulations of the divider circuit assuming a Gaussian distribution for the threshold voltage with a standard deviation of (a) 10mV, (b) 25mV and (c) 50mV

XI. Conclusions

During the last 42 months we have worked on problems related to the fabrication of a SiGe pMODFET static divider circuit on sappahire. We have fabricated SiGe pMODFET devices on silicon-on-sapphire with transconductances as high as 377 mS/mm, f_T = 50 GHz and f_{max} = 114 GHz. The latter is the highest reported value for a SiGe pMODFET. We have found that the device characteristics depend very sensitively on the epitaxial layer structure. Very small changes in the layer thickness or doping concentration result in a lower f_t and/or a shift in V_t, which can significantly reduce the maximum operating frequency of this circuit. To obtain sufficient device yield to achieve working circuits, choices were made in the fabrication processes that also reduced the operating frequency range of the circuits. Specifically, L_g was chosen to be 0.15 μm and the dielectric layer between M1 and M2 was relatively thin. Devices with a shorter gate length and a more optimal device layer structure would have a higher f_t, and a thicker dielectric layer would reduce the parasitic capacitances. The circuit we fabricated on bulk Si operated up to 3 GHz, with layer structures that had a hole mobility ~500 cm^2/V-s and devices with threshold voltages of 0.18V. Circuit modeling indicates that the maximum operating frequency for this circuit fabricated on a SGOS wafer, with high mobility devices having a gate length of 50 nm, higher effective mobilities and an optimized threshold voltage of ~0.3 V, would be about 25-35 GHz.

Early on we found that the quality of available epitaxial SOS wafers was not good enough for circuit fabrication. The work at UW has shown that bonded SOS wafers are very promising from a defect perspective. The fact that bonded SOS wafers are stable only up to temperatures of ~600 ^oC was not a problem for this project, since all fabrication steps are executed at much lower temperatures. Unfortunately, the SOS wafers from UW too late to be used for the final circuit fabrication run. In any case, to take advantage of the sapphire substrate, thin SiGe-on-sapphire substrates are required.
While a similar bonding process can be used to bond a relaxed SiGe buffer layers grown on SOI to sapphire, further work is necessary to obtain a reproducibly thin SiGe layer on sapphire. For other device and circuit applications, where fabrication steps must be implemented at temperatures above ~600 ^oC, a better approach would be to first fabricate the circuits on SOI or SGOI substrates, and afterwards transfer the device layer to sapphire using wafer bonding methods.

Recent IBM publications and conference presentations relevant to this project

"SiGe pMODFETs on Silicon-Sapphire Substrates with 116 GHz f_{max}", S.J. Koester, R. Hammond, J.O. Chu, P.M. Mooney, J.A. Ott, L. Perraud and K.A. Jenkins, IEEE Elect. Dev. Lett. **22**, 92 (2001).

"SiGe MOSFET Structures on Silicon-on-Sapphire Substrates Grown by Ultra-High Vacuum Chemical Vapor Deposition", P.M. Mooney, J.O. Chu and J.A. Ott, J. Electron. Mater. **29**, 921 (2000).

"High frequency noise performance of SiGe p-channel MODFETs", Koester, S.J. Chu, J.O. Webster, C.S., Electron. Lett. (UK) **36**, 674 (2000).

"Extremely high transconductance Ge/$Si_{0.4}Ge_{0.6}$ p-MODFET's grown by UHV/CVD", Koester, S.J. Hammond, R. Chu, J.O., IEEE Electron Device Lett. (USA) **21**, 110 (2000).

"High performance SiGe p-MODFETs grown by UHV/CVD", Koester, S.J. Hammond, R. Chu, J.O. Ott, J.A. Mooney, P.M. Perraud, L. Jenkins, K.A., *1999 Symposium on High Performance Electron Devices for Microwave and Optoelectr0onic Applications*, EDMO (Cat. No. 99TH8401) 1999, pp 27-32.

"RF Systems Based on Silicon-on-Sapphire Technology," I. Lagnado, P.R. de la Houssaye, W.B. Dubbelday, S.J. Koester, R. Hammond, J.O. Chu, J.A. Ott, P.M. Mooney, L. Perraud, K.A. Jenkins, *2000 IEEE International Silicon-on-Insulator (SOI) Conference*, Wakefield, MA, October 2-5, 2000.

"Low-noise SiGe pMODFETs on sapphire with 116 GHz f_{max}", S.J. Koester, R. Hammond, J.O. Chu, P.M. Mooney, C S. Webster, I. Lagnado, and P.R. de la Houssaye, *Proceedings of the 58th Annual Device Research Conference*, Denver, CO 2000, p. 31.

"Silicon on sapphire for RF Si systems 2000", Lagnado, I. de la Houssaye, P.R. Dubbelday, W.B. Koester, S.J. Hammond, R. Chu, J.O. Ott, J.A. Mooney, P.M. Perraud, L. Jenkins, K.A., *2000 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems. Digest of Papers* (Cat. No.00EX397) 2000, pp 79-82.

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