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Planar Double Gate MOSFETs with Thin Backgate Oxides

Erin C. Jones[1], Meikei Ieong[2], Thomas Kanarsky[2], Omer Dokumaci[2], Ronnen A. Roy[1], Leathen Shi[1], Toshiharu Furukawa[3], Robert J. Miller[1], H.-S. Philip Wong[1]

[1]IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

[2]IBM SRDC
Hopewell Junction, NY 12533

[3]IBM Microelectronics Division
Essex Junction, VT 05254

Research Division
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IBM T.J. Watson Research Center, Yorktown Heights, NY 10598

*IBM SRDC, Hopewell Junction, NY 12533

** IBM Microelectronics Division, Essex Junction, VT 05254

Abstract

Planar double gate CMOS devices with thin silicon channels and electrically separate polysilicon top and bottom gates are fabricated. NFETs with L_{poly}= 120nm and 1.3 mA/μm and PFETs with L_{poly}= 75nm and 400 μA/μm are achieved at V_{dd}=1.2V. This is the largest current yet reported in the literature for double gate NMOS devices. Electrical results show a high quality backgate oxide, the improvement of device short channel effect (SCE) using the backgate, and the importance of reducing external resistance in short channel devices.

I. Introduction

Double gate and back gate MOSFET device designs are promising for extending MOS device scaling into the ultimate 10-nm gate length regime [1]. Simulations show that double gate and ground plane MOS devices are more effective than single gate SOI or bulk silicon devices for controlling threshold voltage and short-channel effects (SCE), will have excellent rolloff characteristics, ideal subthreshold slopes, double drive current, and enable a lower minimum effective gate length for the same gate oxide thickness [2]. Although a number of processes for fabricating planar, vertical, and fin-type double gate devices have been reported [3][4][5][6], high DC performance has been elusive, especially for NFETs. A number of issues have been raised by simulation, such as what are the best strategies for controlling the threshold voltage in double gate MOSFETs [7][8], and what real performance gains that can be expected. These issues are still outstanding, pending confirmation of the simulations by hardware experiments. Many devices actually fabricated to date have relied on unusual process sequences and unique materials, making device results difficult to interpret. Here, a simple process for fabricating symmetric NFET and asymmetric PFET devices is developed using a standard logic process flow. Planar double gate devices with electrically separate top and bottom gates are made starting with a custom bonded wafer. Planar devices are of special interest as it is easiest to control and measure planar silicon channel films in the sub-10 nm regime, as required for continued device scaling [2]. Planar double gate devices are also easily benchmarked against conventional single-gate devices. The devices show improved SCE, subthreshold swing, and current drive as predicted for double gate mode.

II. Device Fabrication

Fig. 1a shows the structure of simplified double gate MOSFET devices fabricated to study double gate operation in the DC mode. Starting substrates consist of a thin silicon channel (average 43 nm thick, 40-47 nm range), with blanket layers of thin backgate oxide (3-4 nm), n^+ polysilicon backgate (350 nm) and buried oxide (400 nm) materials underneath. Substrates are prepared by wafer bonding, starting with an SOI wafer, growing gate oxide, depositing backgate material and low temperature oxide films, polishing until the film roughness is low enough for direct bonding, room temperature bonding of the wafer to a handle wafer, optimized high temperature annealing to increase the bonding strength [9], then grinding and etching away the backside and buried oxide of the original SOI wafer, similar to a method described previously [10]. The silicon channel was thinned by oxidation and removal, controlled by ellipsometer and x-ray dif-

fraction measurements [11]. Device processing follows a standard CMOS flow, including trench isolation, 2.4 nm gate oxide, n^+ and p^+ polysilicon gates (for NFET and PFET, respectively), spacers, separate source/drain extension and contact region implants, and thin cobalt silicide for contact to source/drain and gate. For the front and back channels to have similar effective channel length (L_{eff}), implant and anneal cycles for the source/drain extensions and contacts were designed to extend from the silicon surface to back interface, with minimal lateral diffusion or backgate oxide damage. The active device channel is undoped in the NFET; the PFET has strong halos to keep the lateral profile of the extensions sharp. A TEM cross section is shown in Fig. 1b. As the backgate is a blanket layer under the active region, the devices have high backgate to source/drain overlap capacitance which makes them inappropriate for high frequency use. As they are mainly useful for easy study of DC double gate operation, the devices herein have not been optimized to attain technologically relevant threshold voltages. It is assumed appropriate threshold voltages will be achieved in future using asymmetric or dual metal gate materials [7]. This work provides insight into the performance that can be expected of future planar double gate technologies.

III. Device Performance

Front and backgate oxide leakage currents were measured to gauge the impact of the bonding anneal and source/drain implants and anneals on the thin backgate oxide film. The front gate oxide exhibits about 1mA/cm^2 leakage current at 1.2V, and the slightly thicker backgate dielectric leakage about 4x10^{-5} A/cm^2 at 2V applied bias. This is a positive result, showing that a very thin buried oxide can be incorporated into a bonded substrate with long (> 2 hour), high temperature wafer bonding anneal, without causing damage to it [12]. As shown in the linear curves in Fig. 2, long channel (10 μm x 10 μm) double gate devices exhibit ideal double gate operation: saturation current is increased 130% over single gate operation in the symmetric NFET in double gate mode, the increase is 97% in the asymmetric PFET. Subthreshold swing is ideal in double gate mode, 60 mV/dec in both devices, better than front or back gate operation alone. In the logarithmic curves in Fig. 2, the undoped channel of the zero-V_t NFET exhibits backgate conduction under single gate operation, likely due to the thicker backgate oxide, but can be turned off in double-gate mode. This shows how effectively the channel geometry of a double gate device can control short channel effects. In the logarithmic PFET subthreshold curves in Fig. 2, strong halos in the PFET control short-channel effects, so only slight improvement is seen in the double-gate devices. In short channel devices, performance enhancements are not so large, but absolute device performance is very good. In Fig. 3, an L_{poly} =

120 nm NFET has saturation current about 1.3 mA/μm at V_{gs}=1.2V, the best double gate NFET performance reported to date. Double gate mode still exhibits improved DIBL and swing, but the drive current enhancement is only 54%. The increased importance of series resistance in short channel devices reduces the enhancement from the long channel case. Series resistance is high due to a thinning of the channel towards the source and drain (see Fig. 1b), and a larger L_{eff} in the back channel, due to the difficulty of optimizing source/drain extension profiles there. Driving the current of two channels through a single set of contacts exacerbates the problem. This illustrates the importance of ensuring silicided contacts have access to both top and bottom channels in a double gate device technology. As it was mentioned above that the performance of the backgate dielectric is high, there may be some room to be more aggressive in designing the source/drain profiles, perhaps adding a deeper extension implant to increase the sharpness of the backgate extension and reduce the effective channel length of the back channel. The PFET currents are also noteworthy: Fig. 3 shows IV characteristics of a L_{poly}= 75 nm PFET, with 400 μA/μm saturation current at V_{gs}=1.2V, a 25% performance enhancement over single gate operation.The smaller amount of enhancement may be due to the longer effective channel length of the back channel, the effect of which is heightened by the asymmetric gate operation. Since the top gate is p^+ and the bottom is n^+ poly, the bottom gate is not completely turned on in the double gate mode, and the backgate current path is never fully inverted. In this regime of Si channel thickness, top to bottom gate coupling is not expected to be strong enough for the asymmetric device to show very high performance [8]. Such results are shown in Fig. 4, which compares the device operated as an asymmetric double gate device, or biased with an additional -1V on the backgate so that both gates go into strong inversion when the device is turned on.

IV. Conclusion

Planar double gate MOSFETs with thin silicon channels and electrically separate top and bottom gates are demonstrated with drive current enhancements more than 100% in long channel devices. Enhancements over single gate operation are 25-54% in short channel devices, limited by series resistance. The best double gate NFET performance to date is reported, and excellent backgate oxide performance is achieved in a planar device. Double gate mode is seen to improve SCE, subthreshold swing and DIBL.

V. Acknowledgments

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Figure Captions

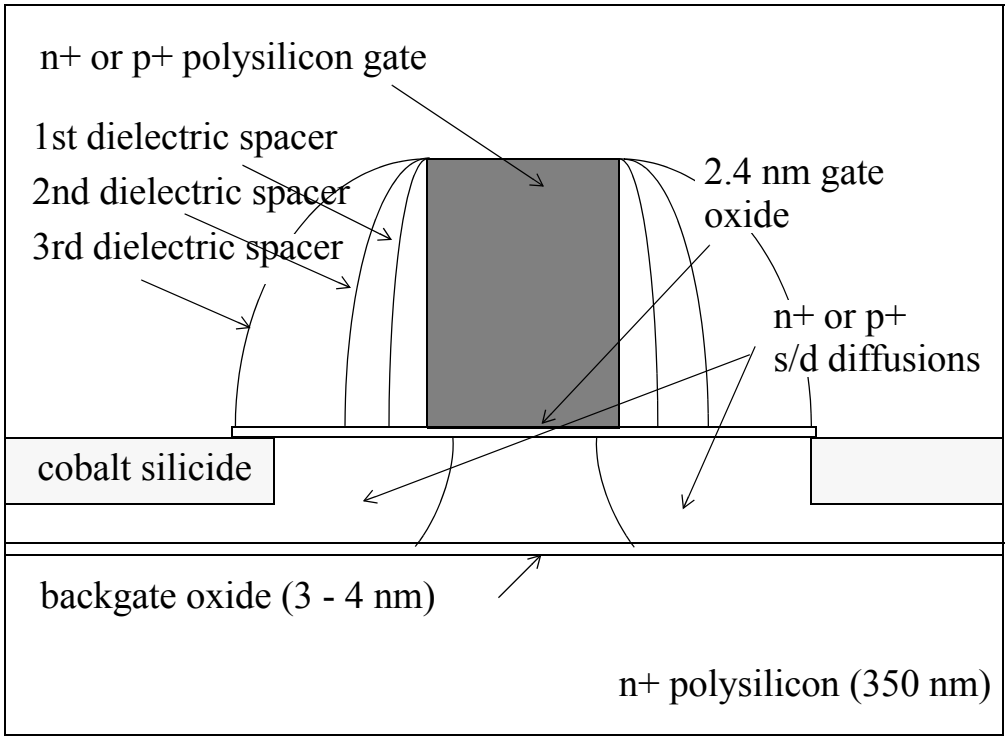
Figure 1a) Schematic of simplified double gate device. b) Transmission electron micrograph of device cross-section.

Figure 2. I_d-V_g characteristics of long channel (10 μm x 10 μm) symmetric NFET and asymmetric PFET devices. In linear plot (right axis), NFET shows current enhancement of 130% and PFET shows enhancement of 97% in double gate mode at V_{ds}=1.2V. Subthreshold characteristics of long channel symmetric NFET and asymmetric PFET are plotted on a log scale in reference to the left axis. Due to the low V_t of the NFET device, a clearer comparison between single and double gate modes is achieved by applying -500mV to turn off the backgate.

Figure 3. I_d-V_g characteristics of short channel (10 μm wide) symmetric NFET (L_{poly} = 120 nm) and asymmetric PFET (L_{poly} = 75 nm) devices.

Figure 4. Operation of short channel asymmetric PFET under double gate operation (V_{gs} applied to both gates simultaneously.) To show the performance of the device under quasi-symmetric operation, an additional -1V offset bias is applied to the backgate. L_{poly}=75nm, V_{ds}=1.2V, device width 10 μm.

Fig. 1.


n+ or p+ polysilicon gate
1st dielectric spacer
2nd dielectric spacer
3rd dielectric spacer
2.4 nm gate oxide
n+ or p+ s/d diffusions
cobalt silicide
backgate oxide (3 - 4 nm)
n+ polysilicon (350 nm)

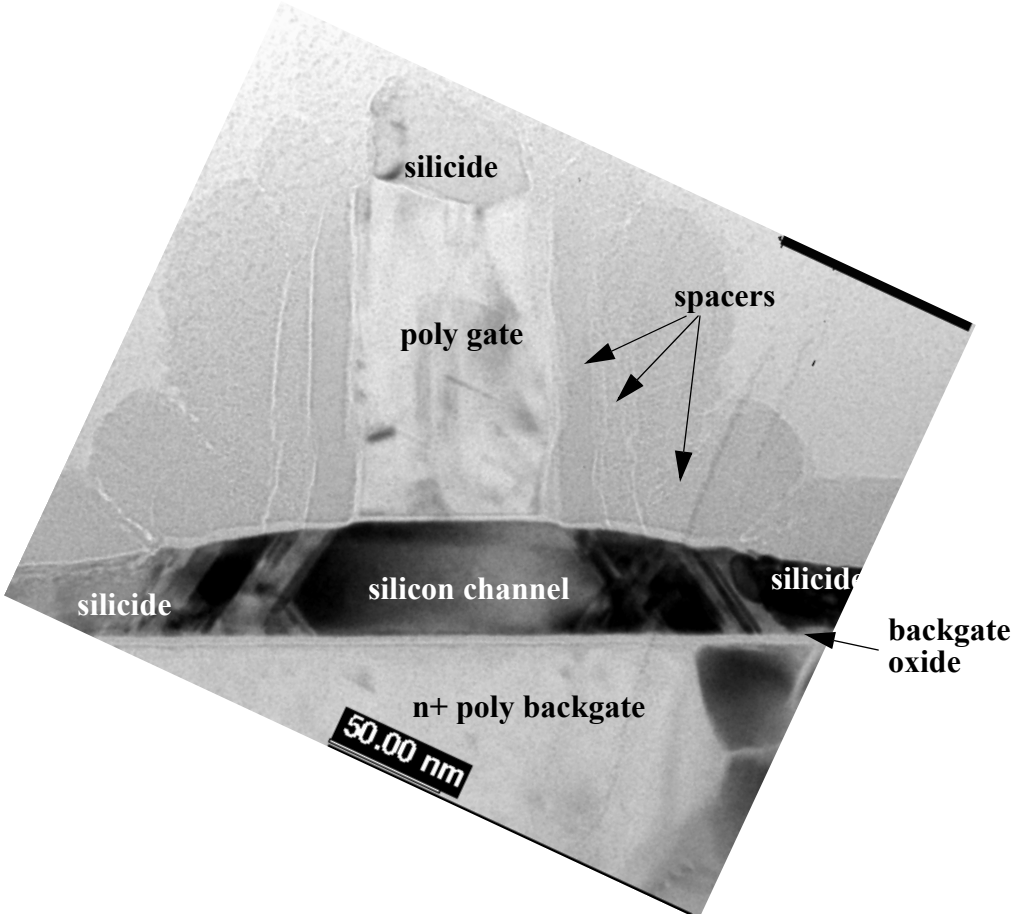

silicide
spacers
poly gate
silicon channel
silicide
silicide
backgate oxide
n+ poly backgate
50.00 nm

Fig. 2.

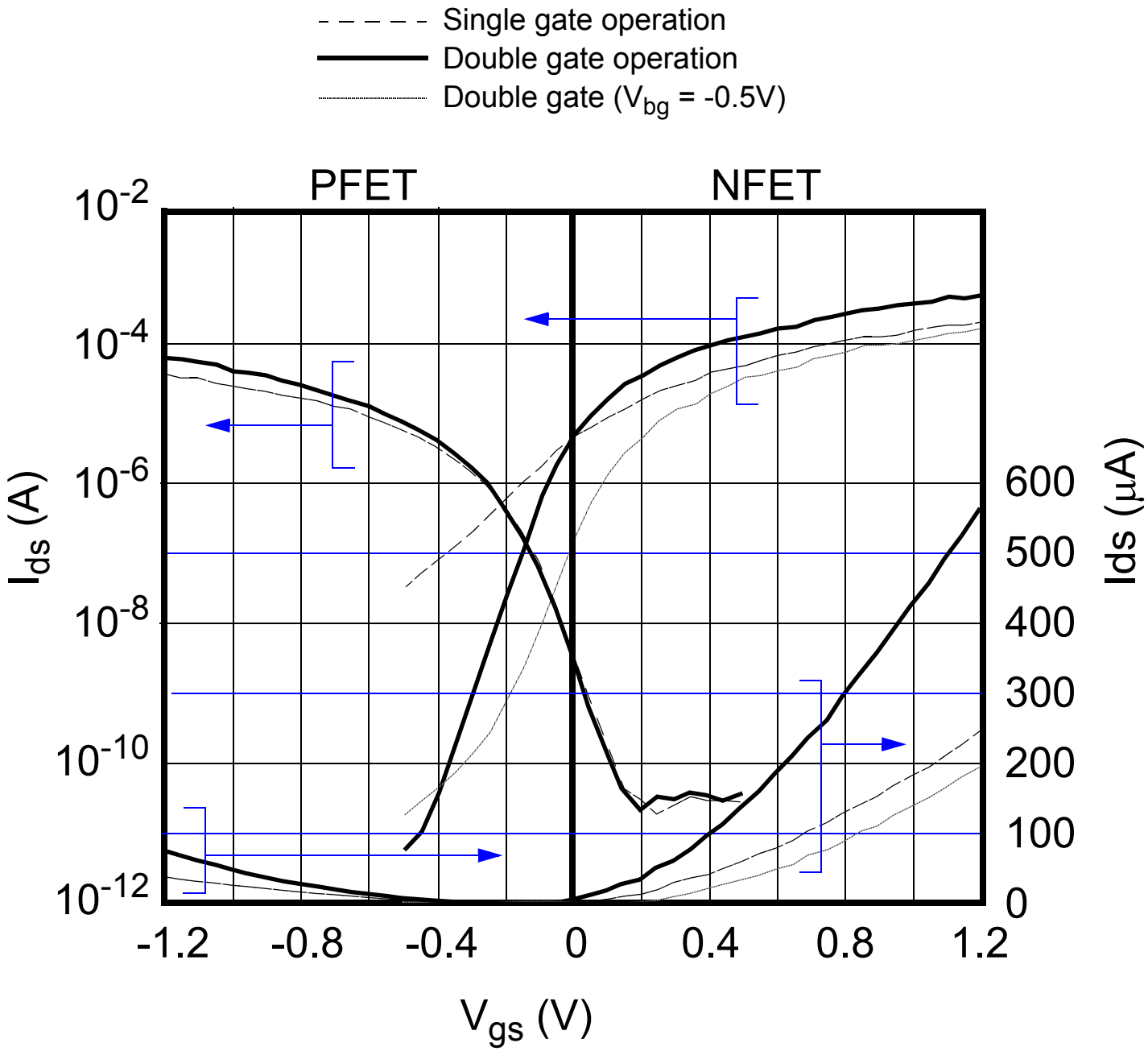

Single gate operation
Double gate operation
Double gate (V_{bg} = -0.5V)
PFET
NFET
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
I_{ds} (A)
600
500
400
300
200
100
0
Ids (μA)
-1.2
-0.8
-0.4
0
0.4
0.8
1.2
V_{gs} (V)

Fig. 3.

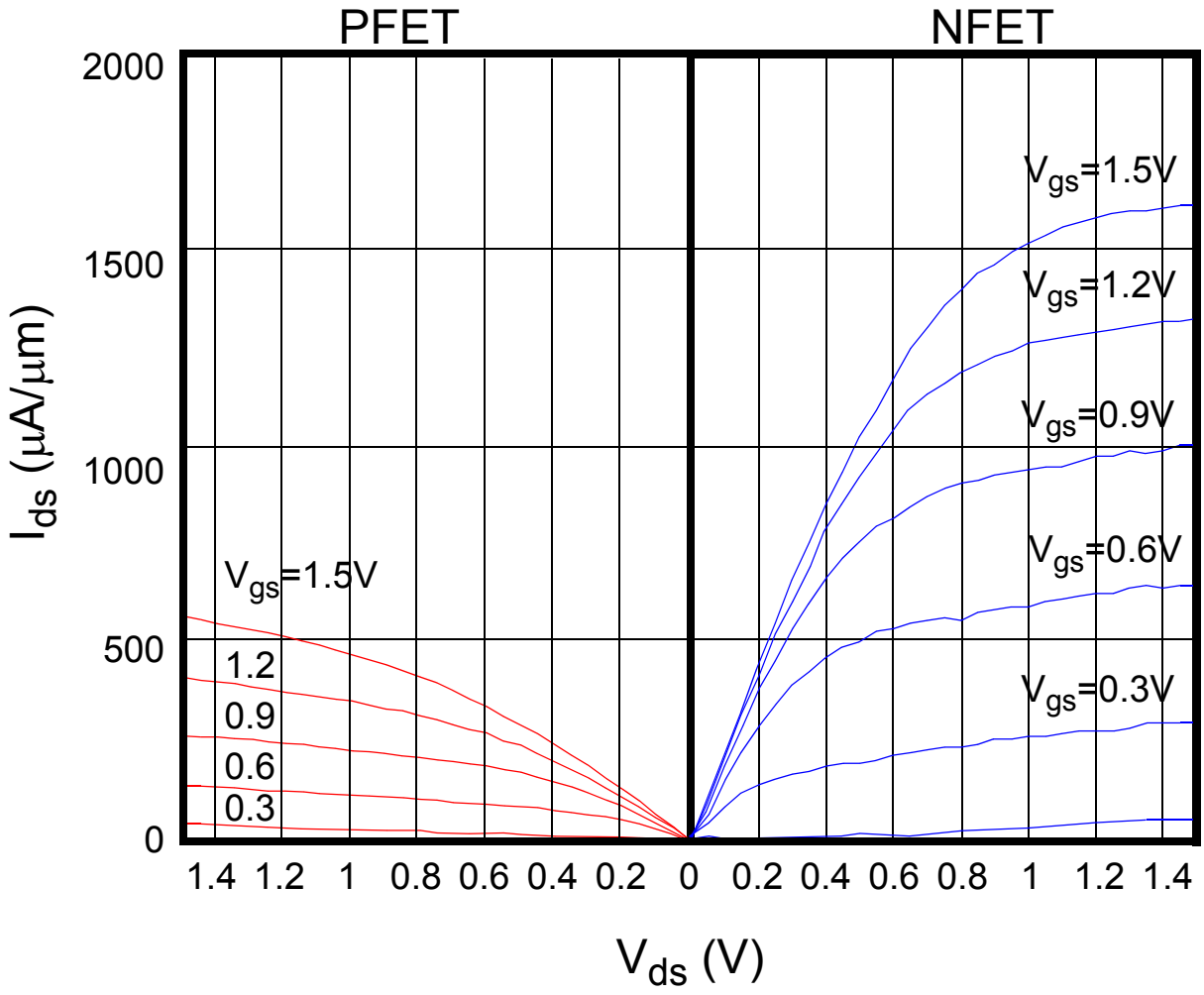
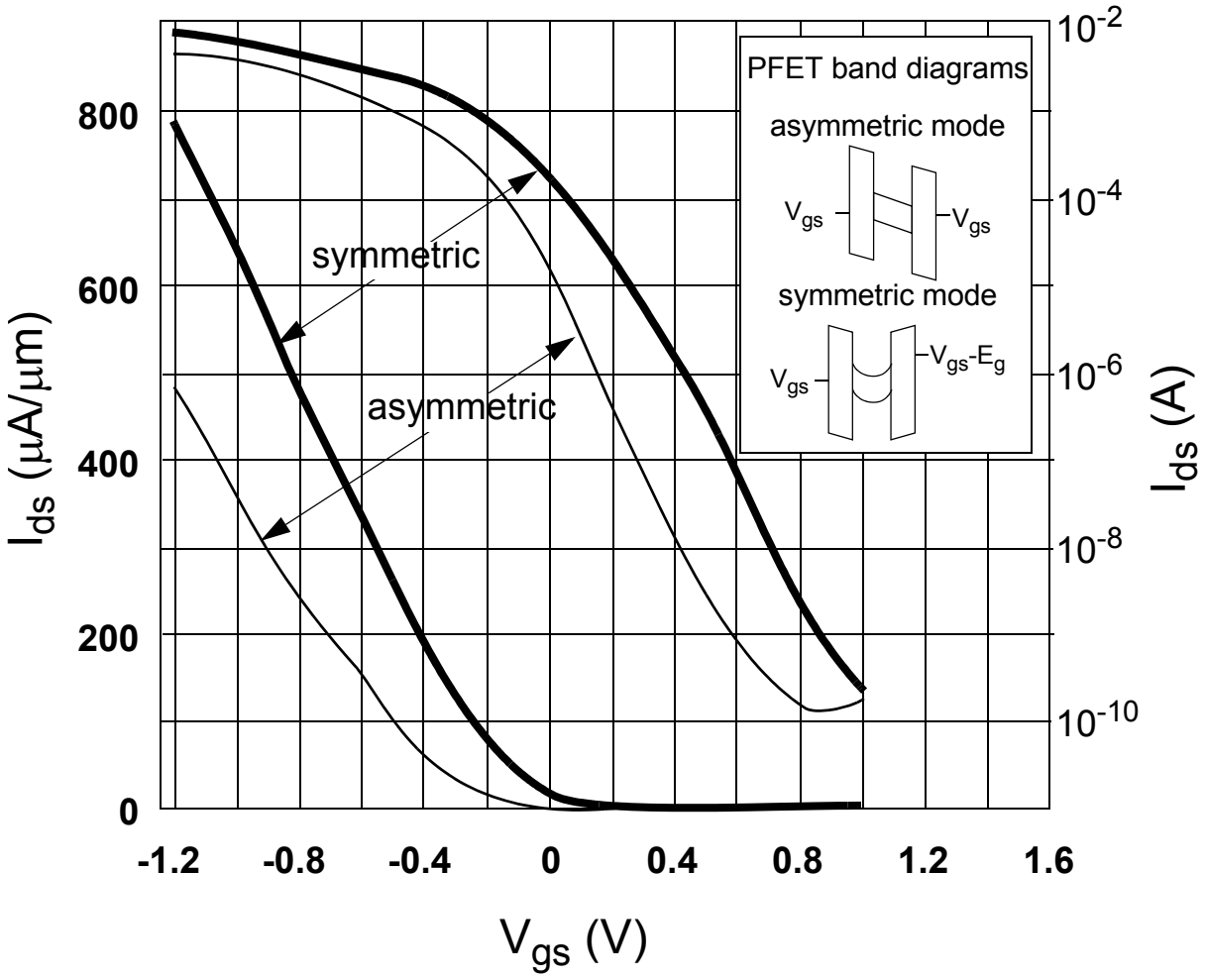

PFET
NFET
2000
1500
1000
500
0
I_{ds} (μA/μm)
V_{gs}=1.5V
1.2
0.9
0.6
0.3
V_{gs}=1.5V
V_{gs}=1.2V
V_{gs}=0.9V
V_{gs}=0.6V
V_{gs}=0.3V
1.4 1.2 1 0.8 0.6 0.4 0.2 0 0.2 0.4 0.6 0.8 1 1.2 1.4
V_{ds} (V)

Fig. 4.


PFET band diagrams
asymmetric mode
V_{gs}
V_{gs}
symmetric mode
V_{gs}
V_{gs}-E_g
symmetric
asymmetric
800
600
400
200
0
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
I_{ds} (μA/μm)
I_{ds} (A)
-1.2
-0.8
-0.4
0
0.4
0.8
1.2
1.6
V_{gs} (V)