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Evaluation Method and Metrics of Shielding/Spacing Approaches for Coupling Avoidance

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Evaluation Method and Metrics of Shielding/Spacing Approaches for Coupling Avoidance

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Abstract

It is common for designers to insert power and ground wires in parallel between signal wires to shield the signal wires from coupling effects. However, this results in an increase in chip area, routing complexity and power dissipation. On the other hand, reduction in coupling can be achieved by simply spacing the wires sufficiently far apart so that coupling effects are minimized and can be budgeted. In this paper, we present an effective decision making procedure with consideration of important performance parameters for choosing the proper coupling avoidance method. Our proposed approach employs a comprehensive analysis of the relative merits of shielding vs. spacing methods. Our experimental results conclude that, contrary to conventional wisdom, wire-spacing is a better option than inserting shields for many cases, particularly those with an initial strong coupling component.

Keywords- Physical design, Capacitive coupling, Signal integrity, Wire shielding, spacing, noise avoidance.

I. Introduction

Capacitive coupling is recognized as one of the most critical problems that designers need to address for deep submicron technologies. In order to reduce the increasing trend of wire resistance, metal wires are made taller and thinner which results in a substantial increase in lateral coupling between wires. The capacitive coupling adversely affects two major performance parameters: noise and delay. The impact of coupling on both parameters is well understood and addressed by many research papers. A sufficiently large noise on a signal line can result in a wrong value being latched at a flip-flop and hence causes erroneous circuit operation[1]. The coupling impact on delay refers to changes in delay of signal line due to switching activities on neighboring lines. At first order, static timing analysis (STA) accounts for coupling capacitance by a modified capacitance to ground, also known as the Miller capacitance[2].

Notwithstanding these analysis techniques, designers still treat crosstalk as an undesirable phenomenon. A variety of techniques is used to eliminate crosstalk at various stages of the design. Since capacitive crosstalk primarily occurs because of close proximity of signal lines, the first choice is to space them apart. But increasing the distance between wires conflicts with the goal of chip-area minimization. A commonly used alternative is to shield signal lines from each other by inserting power/ground lines in between them. Since power/ground lines are tied to constant voltages (namely Vdd and 0), they do not fluctuate (will not make great signal transitions) and hence cannot cause any noise on the signal lines. Approaches to shielding are presented in [3][6]. Although shielding practically eliminates a great deal of coupling between signal lines, it does result in increased area, as well as leads more complicated routing since the power/ground lines have to be connected to a power distribution network. Other approaches to avoid crosstalk at the physical design stage include net ordering[3] and buffer insertion [5]. Recently, [4] presented a method to reduce coupling using active shielding lines. In this approach, the shield, instead of being connected to a power line, is driven by the same driver as that of the signal.

In this paper, we present a comprehensive analysis approach to layout the decision making procedure for effective coupling avoidance. This procedure is primarily developed for a design engineer/ methodologist who is responsible to own physical design rules of high-performance microprocessors and application specific integrated circuits. We also present metrics and guidelines for choosing one avoidance method over the other. Our results demonstrate spacing as a viable and more effective option than shielding for many cases. Contrary to conventional wisdom, we show that especially for cases where coupling is strong, spacing works better than inserting shields.

The rest of the paper is organized as follows: in Section 2, we discuss some preliminaries. In Section 3, we describe the important design metrics and our analysis which form the proposed evaluation procedure. Section 4 presents an analysis of our results from experiments performed. We conclude in Section 5.

II. Preliminaries

Consider a metal interconnect line as shown in Fig. 1. The dimensions of the line are its length L, width W, band thickness T. The height of oxide between the ground plane and the metal line is H. The resistance of the metal line is given by

$$R = \rho L / (W T) \quad (1)$$

where ρ is the resistivity of the metal.

The capacitance value is dependent on the permittivity of the medium between the conductor and the ground plane, and the height H, besides the dimensions of the wire itself. Various methods exist for calculating the capacitance of the wire . In practice, it is usually obtained by detailed extraction or using explicit formula-based approaches. The total interconnect capacitance to ground C_{gnd} is comprised of two components, (i) fringing capacitance (C_f) and (ii) parallel plate capacitance (C_p).

When two or more wires run parallel to each other, the capacitance between the wires is treated as coupling capacitance, which can be also obtained using detailed extraction. The effect of coupling capacitance depends on the gates driving the wires and the switching activity in the vicinity. When line A (aggressor) switches and V (victim) is quiet, A injects noise on the victim through the

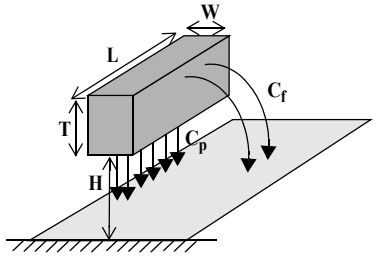

Fig. 1. Interconnect resistance and capacitance

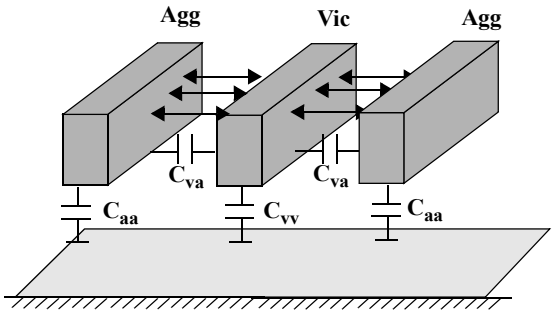

Fig. 2. Coupling and ground capacitances

coupling capacitance C_{va}. This noise can cause a failure by changing the logic value on V. On the other hand, when both V and A switch simultaneously the switching of A changes the effective capacitance loading of V and hence it's delay. For the configuration depicted in Fig. 2 with identical aggressors, the effective coupling capacitance, also known as the Miller capacitance can be treated as $k*C_{va}$, where k is the Miller factor. The total capacitance that is seen at the victim line will be:

$$C_{total} = C_{vv} + k*C_{va} + k*C_{va} \quad (2)$$

For same direction switching, the k value is less than unity, and for opposite direction switching it is greater than unity. The k value also depends on the relative strengths of the drivers. Designers have been using k values of 0 and 2 for early and late mode respectively. But this assumption does not give bounds on the delay, particularly if the strengths of the victim and aggressor lines are not the same. Under certain assumptions, the values of -1 and 3 have been shown to be bounds for the Miller factor [2].

II.A. Scaling effect on resistance and capacitance

In order to increase circuit performance, feature sizes are continuously scaled to smaller dimensions. When the length, width and thickness of a wire are scaled down by a value of α, it can be observed from (1) that the value of resistance is scaled up by a value of α. In order to prevent increase in interconnect resistance due to scaling, the thickness of the wires is scaled by a factor less than α, thereby increasing the aspect ratio (T/W), and hence the coupling between the lines. With decreasing feature sizes, the coupling capacitance is expected to become a larger portion of the total capacitance [7][11].

III. Coupling Avoidance Approaches

Inserting power/ground metal shields is a popular method proposed recently to avoid undesirable effects of trends in coupling capacitance. Signal isolation prevents both functional noise and increase in delay due to coupled lines switching. [8] proposes inserting a power or ground shield after every signal wire, resulting in a regular fabric-like structure. Though all signal wires are shielded from each other, the resulting complexity in routing and power distribution network design can make the chip unfeasible to design. It should be mentioned that inserting shield lines reduces inductive effects and hence has other benefits too. The inductance is reduced because of a closer return path to ground for the current flowing through signal wires. However, inserting shield wires between every pair of signal wires may result in an overkill and overdesign. Moreover, shield insertion significantly increases congestion and may require more metal layers, leading to an increase in mask production costs.

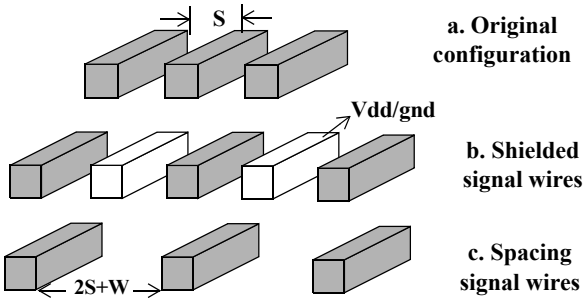

Fig. 3. Different wire configurations used in the paper

Buffer insertion and net ordering have also been proposed as alternative methods to negate the effect of coupling. Buffer insertion requires extra budgetting for psace and results in increased area. Net ordering involves selection of signals that cannot simultaneously switch in opposite directions and placing them adjacent to each other. This switching orthogonality is aimed to be achieved by temporal correlation[3]. However timing information available before the global routing phase is a crude approximation of the actual timing, leading to inaccurate results.

Alternatively the wires can be simply spaced to produce a similar solution. To our knowledge, there has been no thorough analysis or reported results on comparison between shielding and spacing approaches. However, an effective decision mechanism and detailed discussion of these approaches will help designers establish better methodologies which will better avoid the unwanted problems of coupling. This task requires the formulation of critical performance metrics and objective criteria to compare one approach vs. the other.

IV. Proposed Decision Making Approach

Consider the case of two signal wires as shown in Fig. 3. Fig. 3(a) shows the case when wires are unprotected, and strong coupling exists between neighboring wires. When shielding wires are inserted as shown in Fig. 3(b), the total capacitance of the victim wire V remains the same, but much of this will be to the neighboring shields. Instead of shielding, we can space the wires such that the same silicon area will be used. The spacing style is directly applicable to the design and does not require use of auxiliary optimization algorithms. If S is the planned distance between two wires (assuming it is also the distance between the signal and its shields), the distance between two spaced signal wires will be 2S+W, where W is the metal width. Note also that with the assumption of a 2S+W spacing, the number of routing tracks will remain the same as that of the shielding approach. Another important aspect is that the comparison of shielding over 2S+W spacing will display the real return of isolating signal lines over simply spacing the signal lines apart. Since the use of silicon area for the shielding and spacing approach would be the same, these configurations are excellent candidates for objective performance comparisons for making the optimal decision.

IV.A. Impact of spacing on coupling capacitance

The self and coupling capacitance values for the results of this paper are computed by two methods: (i) A formula-based approach, which we obtained from the Berkeley interconnect tools evaluation[10], (ii) An in-house capacitance extractor, which uses a boundary element method. The capacitance values from both methods correlate very well and both used in generating our results.

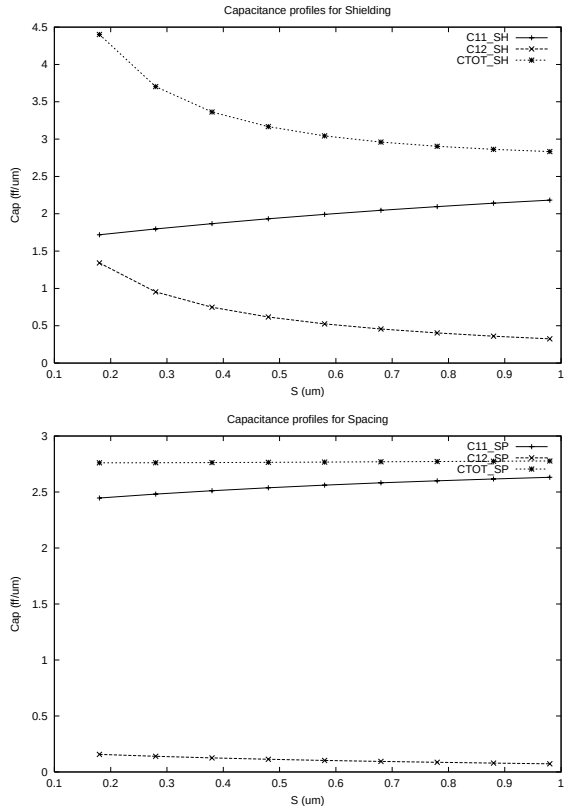

Fig. 4. Self and Coupling capacitance (C_{11}, C_{12}) along with the total capacitance as a function distance between wires. a) Shielding (original) configuration, b) Spacing configuration

With the configuration shown in Fig. 3, Fig. 4 shows plots of the ground capacitance (C_{vv}) and coupling capacitance (C_{va}) to the neighboring line per unit length, as a function of the distance S between the wires. The length, width, thickness and height from the ground are fixed. (L=1000μ, H=T=0.4μ, W=1.6μ). In Fig. 4(a) (the shielding case), the coupling capacitance is seen to decrease sharply with increasing distance. This is because the capacitance is calculated in a critical region where there is strong coupling between neighboring lines. The ground capacitance is observed to increase because of more fringing effects as lines are separated farther.

In Fig. 4(b), the self and coupling capacitance values are plotted as a funcion of S, when the wires are separated by a distance 2S+W. In circuit operation, the coupling capacitance is amplified if a neighboring line switches, and hence the effective total capacitance seen by the victim is higher than the sum of the coupling and ground capacitances. However, it can be observed from the figure that the coupling is almost an order of magnitude smaller than the case in shielding. This can again be explained by the almost-exponential decrease in coupling capacitance with increasing distance. Therefore, the rate of decrease in coupling-capacitance for 2S+W spacing is not as aggressive as shielding, but overall the capacitance value is much lower than the shielding (and the original) case. The capacitance plot shown here depends on other geometry parameters like thickness (T), width (W) and height (H) of the wire from the ground plane, though the trends in the curve with respect to spacing remain the same.

IV.B. Experimental setup and procedure

In order to investigate the effects of spacing and shielding on different performance metrics, we used the configurations depicted in Fig. 3 and used clock buffers to drive each line. All experiments were performed for 0.18μ static CMOS technology. The length of wires was limited to 1000μ for all cases. In fact, for wires longer than this value, buffer insertion would be applied resulting in a significant reduction in delay and preventing slew degradation. The wire widths were varied over a wide range of values to simulate fat as well as thin wires. In current practice, the wire width is typically increased in order to reduce the resistance of long wires. Note also that copper was chosen to be the metal of choice in keeping with current trends for interconnect. Since copper's resistivity is smaller than aluminum, the aspect ratio (T/W) can be smaller and the thickness need not be increased significantly to reduce resistance. However we chose a wide range of aspect ratios too in order to study it's impact on delay and noise performance of current and future circuits.

Even though the length of the interconnect is fixed, we used different driver sizes to simulate different loads. The effect of coupling on noise as well as on delay is a strong function of the driver resistance. Each interconnect line was driven by a clock buffer used in real high performance commercial processor designs. Seven different buffer sizes were used, with the strength of the buffers (W/L) ranging from 4X to 70X compared with a minimum sized buffer.

The minimum distance between wires is a function of the technology parameters. For our experiments, we considered the minimum value for S to be 0.18μ, and allowed it to vary up to 0.5μ. As mentioned above, the thickness was varied from 0.2μ to 1.2μ to simulate a range of aspect ratios. The height H above the ground plane does not have a significant impact on the nature of results and we used only two different H values.

In our experiments, the difference between best and worst-case delays was determined by a static approach. The Miller coefficients were varied between -1.0 and 3.0 to simulate same direction as well as opposite direction switching. For each data point, two aggressors and one victim were simulated, and the delay and noise values were obtained for both the shielding and the spacing case. The limiting cases are reported as the worst and best case results along with the nominal case which is the case of quiet aggressors (k=1.0).

To compute the noise on the victim, the victim line was held at a constant value (both 0 and Vdd) and the aggressor was switched in both directions and the worst-case noise was used. Different characteristics of the noise pulse - the shape of the waveform, pulsewidth or peak value - can be also considered. For simplicity, we observe the peak of the noise waveform, though any other metric can be used since we have the complete exact noise waveform available from circuit simulation.

V. Simulation Results

For each configuration in our experimental setup, detailed simulations were carried out using AS/X, an inhouse SPICE-like simulator. The interconnect was represented by a distributed RC line. The coupling capacitance extracted was also distributed along the lines. The input to all the clock buffers is a ramp waveform with a rise-time of 100ps. The slew at the output of the gate (which determines the current injected into the neighbor) is a strong function of the load, and a weaker function of the input slew. We consider four performance metrics: delay, slew, noise and power which are all critical for present day technologies. These metrics are evaluated under

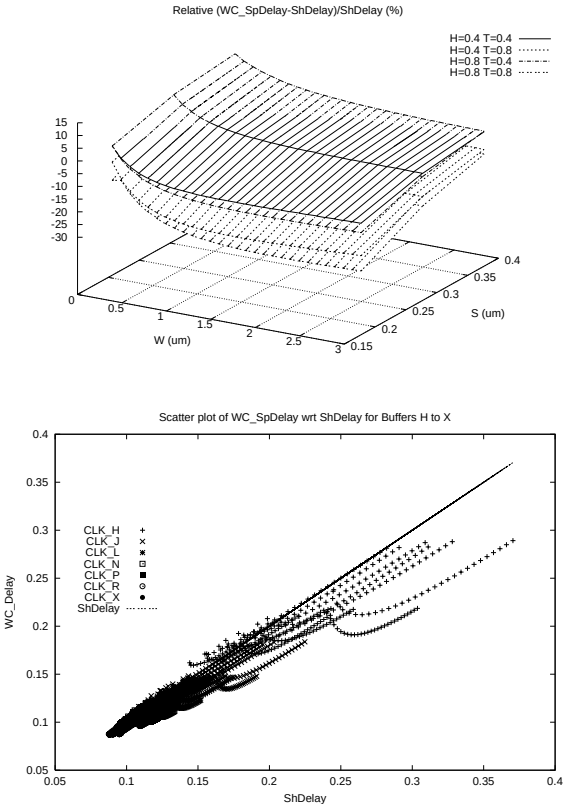

Fig. 5. Scaled delays for shielding and Worst-case spacing configuration for various (H,T) settings as a function of wire-width (W) and line spacing (S).

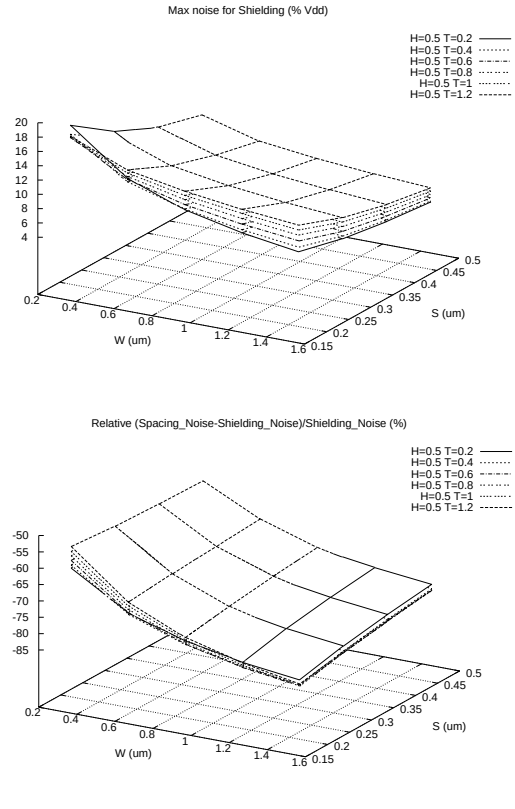

Fig. 6. a) Peak noise on victim scaled with Vdd for the original configuration, b) the relative reduction in peak noise from the 2S+W spacing as a function of W and S.

constant chip area, by way of our earlier choices for wire configurations.

V.A. Delay performance

Fig. 5 shows three dimensional plots of signal delay on the victim line as a function of distance between wires (S) and wirewidth (W). The delay includes both the gate and the interconnect component, decreases with distance and increases as a function of thickness. The delay for the shielding case tracks the behavior of the capacitance curve (Fig. 4(a)). For each case with shielding, the best- and worst-case delays with 2S+W distance were also computed.

In order to compare both approaches, the relative difference in delays between the spacing and shielding cases is plotted in Fig. 5(a). The figure illustrates that for a majority of cases, the worst-case delay (late-mode) for spacing configuration is smaller, as much as 30% less, than that obtained from shielding. Hence, with lesser metal area, and less complex routing procedures, designers can achieve the same objectives of minimizing delay impact. This result confirms our previous results for capacitance distribution shown in Fig. 4. In many of the cases (roughly 80%) shown in Fig. 5, coupling capacitance of shielding is far bigger than that of the 2S+W case, and dominates the total effective capacitance load on victim. Although the uncertainty in delay is eliminated, this results in a larger delay for the shielding configuration for these cases. We also notice that shielding actually eliminated the coupling impact and reduced the delay of the victim line for cases where wires are selected narrow and considerable spaced apart (low W and high S). For such cases, the approach of 2S+W spacing is not effective for delay performance.

We repeat the experiment with differently sized buffers, and obtain the scatter plot shown in Fig. 5(b). The results with different buffers result a similar 80% of the cases where the shielding results in larger delay values than the worst-case delay of the 2S+W spacing configuration. Nominal delays of the 2S+W spacing are found always smaller than those of the shielded case, between 5% and 40% lesser.

V.B. Slew performance

The slew on the victim line signal is also affected by the switching activities in the vicinity. Slew is an important metric since it affects noise and downstream delay and designers have constraints on the range of slew values possible for a signal wire. In our experiments, we found that the victim line slew performance closely tracks the delay. Hence the same decision criteria that are used to minimize delay can be applied to control slew degradation.

V.C. Noise performance

If coupling noise is sufficiently large in magnitude and duration, it may create functional errors by changing the value of the victim net or by creating a wrong state in the circuit. To evaluate the 2S+W spacing and shielding alternatives with respect to the noise performance, we followed a similar set of experiments performed for delay. The same interconnect geometry parameters were used along with a medium-size buffer. As mentioned in the previous section, we selected the peak noise value as the metric of interest.

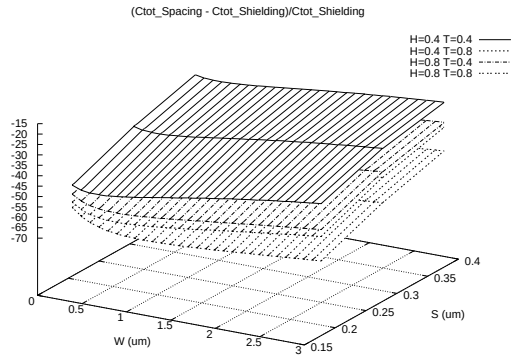

Fig. 7. Total capacitances for Shielding and 2S+W Spacing configurations. Total capacitance linearly relates to the total power consumption on the victim line.

In reality, shielding suppresses almost all of the coupling noise on the victim line, because the shields are held at constant levels during victim line's signal transition. Although there is a small parasitic coupling between the victim line and its farther neighbors, we will ignore it since such second-order coupling capacitors are really small compared to C_{vv} and C_{av} . Therefore, we can only compare the noise performance of the 2S+W spacing with the original circuit configuration, where the wires were spaced by S without shields. The comparison of noise performance explains how much of improvement the spacing can provide over the original choice of interconnect.

Fig. 6(a) shows the surface plots of peak noise for a number of circuit configurations drawn as a function of W and S. Fig. 6(b) shows the relative reduction in peak noise made by the 2S+W spacing over the original interconnect. From the plot we see that the original peak noise is reduced considerably, with a reductions of 50-90% in magnitude. Since some amount of noise well within the noise margin can be budgeted for the design process, a quantitative criterion can be chosen by the designer to determine where the noise reduction with 2S+W spacing is acceptable.

V.D. Power consumption

Since power dissipation is one of the most critical performance bottlenecks for future circuits, any solution addressing the coupling problem must be considered in conjunction with a power perspective. This metric is neglected in the proposal for shielding[8], and we will discuss the fundamental issues related to the power dissipation in the context of coupling avoidance.

Although architectural techniques are the most effective solutions for low-power design, circuit power can be greatly reduced by keeping the load capacitances as low as possible. Here we assume that the total power of a circuit is linearly related with the load capacitance it charges. Therefore, we compare the total capacitances for the shielding and the 2S+W spacing approaches assuming the aggressors are quiet.

Fig. 7(a) shows the relative difference between the total capacitance for the spacing and shielding approaches, again as a function of the wire geometries. The total capacitance, hence the expected power consumption is seen to be always smaller for the spacing case since we assume the aggressors are quiet. From the plot we see that for large S values, the total capacitance value difference between both approaches do not vary significantly, but for shorter S, spacing can result in much lesser capacitance and hence power.

Another item that needs to be mentioned here is the extra work shielding requires for power distribution network design and verification. Today's circuits operate at very low voltages to save power and to increase the speed of the operation. Therefore, the reliability of the power supply and ground distribution network is of utmost important than ever. Since the IR-drops and Ldi/dt noise may impact the circuit performance negatively, the power distribution network must be low-resistance and uniform accross the chip. With shielding approach, the power distribution network must be connected to the shield lines, using precious routing resources and metal area. Shielding will also increase the number of electrical elements in the power grid model and hence will complicate the analysis. Therefore, 2S+W spacing appears to be more favorable than shielding from a power perspective.

V.E. Other considerations

The approach taken for coupling avoidance approach may impact several other parameters important for current design technologies. One of the most critical items is that of inductance, due to the manner in which it affects signal delays and may cause ringing. In order to control inductance values on global nets, shielding is applied at a periodic basis to provide a shorter current return path. It has been previously proposed to use one shield line for every ten signal lines for optimal performance. Therefore, one needs to properly consider inductance effects in the evaluation of noise avoidance approaches.

Another important item that needs a careful consideration is the manufacturability of the design. In this perspective, we would like to mention that the 2S+W spacing will have a sufficiently large area between the metal lines that will dramatically reduce the defect density that may cause shorts and bridging faults. In contrary, since spacing will have low metal density, it may cause more nonuniform dielectric thicknesses with the application of chemical mechanical polishing process. Therefore the impact of the coupling avoidance approach can have critical implications for the manufacturability of the design.

VI. Optimal Decision Criterion

Our experimental results show that depending on the metric of consideration, shielding or 2S+W spacing approaches may yield different advantages and disadvantages. For better results, a comprehensive analysis and decision procedure must be employed by the designer for particular design goals. In the light of the results obtained, we propose two simple but effective decision criterions applicable in determining the proper coupling avoidance approach.

Fig. 8(a) shows a contour plot of the difference between shielding case delay and worst-case 2S+W spacing delay for the victim line. The case for H=T=0.8μ is considered, and the contour levels are plotted as functions of W and S. For a simple delay-centric criterion, one can choose the use of a seperator line on the (W,S) plane to prefer one approach over the other. Depending on the interconnect size, a quick comparison between the lines can determine the advisable avoidance method.

Another possible decision criterion between the methods discussed is the control of delay uncertainty. Fig. 8(b) shows the delay uncertainty for 2S+W approach computed from best and worst case delays as a percentage of nominal case delay. We must mention that a similar plot for original configuration resulted in more than 100% variability on some datapoints proving the importance of the coupling problem. Depending on the budget on the delay uncertainty,

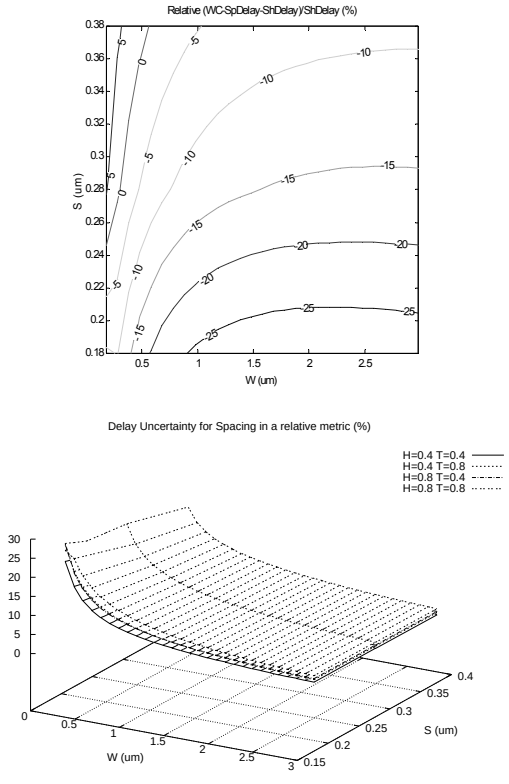

Fig. 8. Proposed criterions to perform decision making between shielding and 2S+W spacing approaches to overcome coupling effects and maintain high performance

the designer may choose to use 2S+W spacing approach over shielding which seems to be increasing the delays, total capacitance and power for most of the cases. Therefore, a threshold can be also used with a simple contraint on delay uncertainty which can be easily measured by the help of Miller factors.

Other criterions can be easily developed with the mixtures of power and noise performances, and inequality type constraints can be deployed to make the coupling avoidance decision. The primary contribution of this paper is the objective evaluation method of the coupling avoidance approaches with considerations of the impacts on many performance metrics. From the results obtained, it can be observed that the thicker the wires, the more the coupling and hence the more advantageous it is to space wires apart to achieve coupling avoidance. This is completely contrary to common knowledge that shielding is required particularly for lines that are more strongly coupled.

VII. Conclusions and Future Work

In this paper, we have presented a comprehensive analysis and decision making methodology to determine a coupling avoidance strategy. The impact of shielding and spacing approaches result in critical differences in a large design when applied on a general basis to overcome the coupling problem. Excessive (un-necessary) shielding may significantly increase the total capacitance of the signal line, which dissipates more dynamic power in operation. On the contrary, spacing retains a smaller capacitive coupling, implies some smaller delay uncertainty and would still requires coupling-aware design/analysis flows which are in common use today. However, it will not create extra congestion (burden) for routing and will not increase post-layout analysis complexity. Since, on average, spacing reduces the total capacitance, it will not increase the power consumption which seems to be the major performance metric of the future. Therefore, based on results obtained, we predict that spacing is a more viable option in many cases (although unexplored earlier) and will result in better, more verifiable design. However, because of increasing effects of inductance and inductive coupling, it is unavoidable to insert some shield wires, but this can be done with a very small ratio of shields to signal wires.

The critical contribution of this paper is establishment of important metrics and analysis methodology to determine the optimal noise and coupling avoidance strategy. We have studied performance trends with different interconnect sizes and configurations. By creating realistic experiments, the designer may apply the right approach to prevent the unwanted impact of capacitive coupling and will be able to shorten overall design turnaround time.

As future work, we plan to better evaluate the effect of inductance and inductive coupling and make a more thorough study of the power-grid disbtribution problem for different coupling avoidance approaches.

VIII. References

[1] K.L.Shepard, V.Narayanan and R.Rose, “Harmony: Static Noise Analysis of Deep Submicron Digital Integrated Circuits,” *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol.18, pp.1132-1150, August, 1999.

[2] P.Chen, D.A.Kirkpatrick and K.Keutzer, “Miller Factor for Gate-level Coupling Delay Calculation,” *Proc. IEEE/ACM Intl. Conf. on Computer-Aided Design*, 2000.

[3] J.Ma and L.He, “Formulae and Applications of Interconnect Estimation Considering Shield Insertion and Net Ordering,” *Proc. IEEE/ACM Intl. Conf. on Computer-Aided Design*, 2001.

[4] H.Kaul, D.Sylvester and D.Blaauw, “Active Shields: A New Approach to Shielding Global Wires,” *Proc. Great Lakes Symposium on VLSI*, pp. 112-117, April, 2002.

[5] C.J.Alpert, A.Devgan and S.T.Quay, “Buffer Insertion for Noise and Delay Optimization,” *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, pp.1633-1645, Nov., 1999.

[6] H.P.Tseng, L.Scheffer, C.Sechen, “Timing and Crosstalk Driven Area Routing,” *Proc. Design Automation Conference*, pp.378-381, 1998.

[7] International Technology Roadmap for Semiconductors, *http://public.itrs.net/Files/2001ITRS/Interconnect.pdf*

[8] S.Khatri, A.Mehrotra, R.K.Brayton, A.S.Vincentelli and R.H.J.M.Otten, “A novel VLSI Layout Fabric for Deep Submicron Applications,” *Proc. Design Automation Conference*, pp. 491-496, 1999.

[9] T.Xue and E.Kuh, “Post global-routing crosstalk synthesis,” *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol.16, pp. 1418-1430, Nov., 1997.

[10] Handy Interconnect Tools, www-device.eecs.berkeley.edu/~xuejue/interconnect.htm

[11] H.B.Bakoglu, “*Circuits, Interconnections and Packaging for VLSI*,” Addision-Wesley, 1990.