RC22641 (W0211-136) November 18, 2002
Electrical Engineering

IBM Research Report

A Model for Gate Oxide Breakdown in CMOS Inverters

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ABSTRACT

The effect of oxide breakdown on the performance of CMOS inverters has been investigated. The results show that the inverter performance can be affected by the breakdown in a different way depending on the stress polarity applied to the inverter input. In all the cases, the oxide breakdown conduction has been modeled as gate-to-diffusion leakage with a power law formula of the type $I= KV^p$ which was previously found to describe the breakdown in capacitor structures. This implies that the breakdown physics at oxide level is the same that at circuit level.

Index terms: Dielectric breakdown, oxide reliability, leakage currents, oxide breakdown, hard breakdown, CMOS.

I. INTRODUCTION

With the continued scaling in oxide dimensions the analysis of the oxide breakdown (BD) failure has acquired a great interest. Of the many papers in the literature on the breakdown of ultra-thin oxides, most have focused the study of this failure mechanism on simple MOS capacitors or transistors. However, the increasing importance to improve the reliability of circuits makes it necessary to investigate the effect of oxide BD on circuits [1].

Previous authors have claimed that the actual oxide reliability specifications can be relaxed on circuits, showing that even after several hard breakdowns (HBD) certain digital circuits can still remain functional [2]. To better understand the effect of BD on digital circuits we have analyzed the influence of BD on the performance of CMOS inverters, the building block of most digital circuits.

2. EXPERIMENTAL

The inverters used in this work were fabricated with 0.13μm /1.2V partially depleted SOI technology, with W=0.175 μm, L= 0.125μm, and t_{ox}= 1.5 nm, for both PFET and NFET [3]. Constant voltage stresses (positive or negative) were applied to the inverter input to provoke the oxide breakdown, with inverter output at ground and other terminals floating. The stress voltage was current-limited [4] in order to avoid reaching the final oxide HBD too quickly. In this way, progressive oxide wear out [5] can be induced and its effect on the circuit behavior can be studied. After the application of a constant stress until a determined current limit was reached, the I-V characteristics (applying a ramp voltage at the inverter input with the other terminals grounded) and the inverter transfer curve were measured. The BD location and conduction characteristics are obtained from the IV, and the effect on the inverter performance is monitored by the changes in the inverter transfer curve. The stress was continued by increasing the stress voltage or current limit to increase the oxide damage. This stress sequence was applied until the device was completely broken. In this paper, only oxide breakdown between inverter input and output was considered.

3. RESULTS

The performance and the oxide degradation of the inverter are affected differently depending on the stress polarity applied to the circuit input. For positive polarity stress, the evolution of the I-V characteristic (Fig 1a) shows that the leakage current through the NFET oxide is higher than through the PFET, which indicates that the NFET oxide is more damaged than the PFET oxide. Consequently a voltage increase of the lower part of the inverter transfer curve, V_{OL}, can be observed as the NFET oxide becomes more damaged (Fig. 2a), and the performance of the circuit becomes affected. However, for negative voltage stresses, the PFET oxide is mainly damaged (Fig.1b) and a voltage decrease of the higher part of the inverter transfer curve, V_{OH} (Fig. 2b) is produced. In addition, for positive (negative) voltage stress the transfer curves exhibit a shift to the right (left) due to a change in the threshold voltage (V_t) of the NFET (PFET), not related to the breakdown event itself.

In all the cases, the transfer curves after the different stresses can be fitted by a combination of a Vt shift and a leakage current between the inverter input and output. The leakage current follows the form of a power law formula as $I= KV^p$. This fitting coincides with the BD model proposed by some authors [6] and implies that the BD physics at oxide level and at circuit level are the same. Simple voltage dependent current sources between gate and drain or gate and source allow the oxide BD leakage current in a transistor to be modeled in a circuit simulation (Fig. 3). Similar voltage dependent current sources applied between source and drain have been used to simulate hot-carrier-induced degradation [7]. In our work a non-linear voltage dependent current source between gate and drain of the inverter transistors was used to model the oxide leakage current between the inverter input and output. We note in particular that linear (i.e. ohmic) breakdown resistance does not provide a good description of the experimental data. The ohmic model provides good results just for oxide HBD [8] but we have observed that the power law model simulates much better the oxide degradation prior to its final breakdown.

Different values of K factor or p are necessary depending on the degradation level of the oxide. The exponent p can vary from 5 to 2 as the degradation level increases. For both positive and negative stresses, the parameters of the transfer curve fittings are different for output high and output low (Table I). There is usually a difference of one order of magnitude between the K values between these two parts of the transfer curve, with a lower value of K for the more distorted portion of the transfer curve (output high for negative stresses and output low for positive stresses) (see table I). Just for the case that the oxide is strongly stressed close to its final breakdown, and consequently the transfer curve of the inverter is very modified, the leakage current through the oxide is fitted by the superposition of two currents, one of the quadratic form $I= KV^2$, in parallel with a linear resistance of $\approx$ 35 KΩ. Simulations using the leakage current parameters of Table I but without the V_t shift illustrate the influence of the oxide BD leakage current alone in the inverter transfer curve, to more accurately represent the effect of BD under circuit operation conditions (Fig. 4). In this case, the effect of the oxide leakage current in the inverter performance appears reduced, because without Vt degradation the transistor drive current is greater, so the BD leakage has a smaller influence.

CONCLUSIONS

The influence of oxide BD on the performance of CMOS inverters has been analyzed. The results show that the BD affects inverter performance in a different way depending on the polarity of the applied stress to the inverter input. For positive (negative) stress polarity the NFET (PFET) is mainly damaged. In all the cases, the oxide leakage currents have been modeled with a power law formula of the type $I= KV^p$, which implies that the BD physics at oxide level is the same that at circuit level. Different values of K and p parameters are necessary to fit the high and low part of the inverter transfer curve due to the different degradation level of the inverter transistor with the stress polarity.

ACKNOWLEDGEMENTS

R.Rodríguez is funded by a Fulbright Grant and the Ministry of Education, Culture and Sports, Spain.

REFERENCES

[1] R. Rodríguez, J. H. Stathis, B. P. Linder, S. Kowalczyk, C. T. Chuang, R. V. Joshi, G. Northrop, K. Berstein, A. J. Bhavnagarwala and S. Lombardo, " The impact of gate oxide breakdown on SRAM stability", accepted for publication in the *IEEE Electron Device Lett*., in September 2002.

[2] B. Kaczer, R. Degraeve, G. Groeseneken, M. Rasras, S. Kubicek, E. Vandamme and G. Badenes, "Impact of MOSFET oxide breakdown on digital circuit operation and reliability," in *IEDM Tech. Dig*., 2000, pp. 553-556.

[3] P. Smeys, *et al.,* "A high performance 0.13μm SOI CMOS technology with Cu interconnects and low-k BEOL dielectric," *VLSI Tech. Symp*., 2000, pp. 184-185.

[4] B. P. Linder, J. H. Stathis, R. A. Wachnik, E. Wu, S. A. Cohen, A. Ray and A. Vayshenker, "Gate oxide breakdown under current limited constant voltage stress", VLSI Technol. Symp. Dig., pp. 214-215, 2000.

[5] F. Monsieur, E. Vincent, D. Roy, S. Bruyere, J. C. Vildeuil, G. Pananakakis, G. Ghibaudo, " A thorough investigation of progressive breakdown in ultra-thin oxides. Physical understanding and application for industrial reliability assessment", IRPS Proc. 2002, pp. 45-54.

[6] E. Miranda, J. Suñé, R. Rodríguez, M. Nafría, and X. Aymerich, "A function-fit model for the soft breakdown failure mode," *IEEE Electron Device Lett*., vol. 20, pp. 265-267, 1999.

[7] K. N. Quader, C. C. Li, R. Tu, E. Rosenbaum, P. K. Ko, C. Hu, " A bi-directional NMOSFET current reduction model for simulation of hot-carrier induced circuit degradation", IEEE Trans. Electron Devices, vol. 40, No. 12, pp. 2245-2254, 1993.

[8] R. Degraeve, B. Kaczer, A. De Keersgieter, G. Groeseneken, "Relation between breakdown mode and breakdown location in short channel NMOSFETS and its impact on reliability specifications", IRPS Proc. 2001, pp. 360-366.

FIGURE CAPTIONS

Fig. 1. Post-BD IV characteristics of inverters. (a) positive stress on input, (b) negative.

Fig. 2. Transfer curves of inverters after breakdown to various levels. (a) positive stress on inverter input. (b) negative. Lines are experiment, symbols are model.

Fig. 3. Circuit to model the oxide breakdown leakage current from gate to drain or gate to source in a transistor.

Fig 4. Simulated inverter transfer curves with oxide leakage currents between the inverter input and output using the fitting parameters of table I, without taken into account the V_t transistor shift that is included in the transfer curve fittings of Fig.2. (a) positive stress on inverter input. (b) negative stress.

Table I. Fitting parameters of the oxide breakdown leakage current for the degradation levels shown in Fig. 2 using the power law formula $I=KV^P$. For positive voltage stress, to fit the last curve (open circles) was necessary to include a linear resistance in parallel with the power-law conductance.

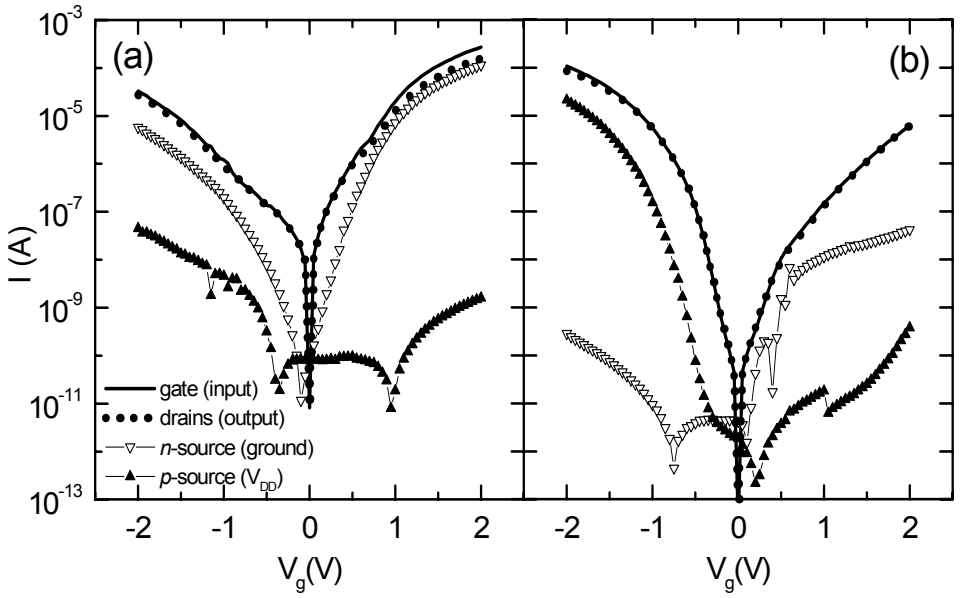

(a)
(b)
I (A)
10^{-3}
10^{-5}
10^{-7}
10^{-9}
10^{-11}
10^{-13}
gate (input)
drains (output)
n-source (ground)
p-source (V_{DD})
-2
-1
0
1
2
V_g(V)

Figure 1

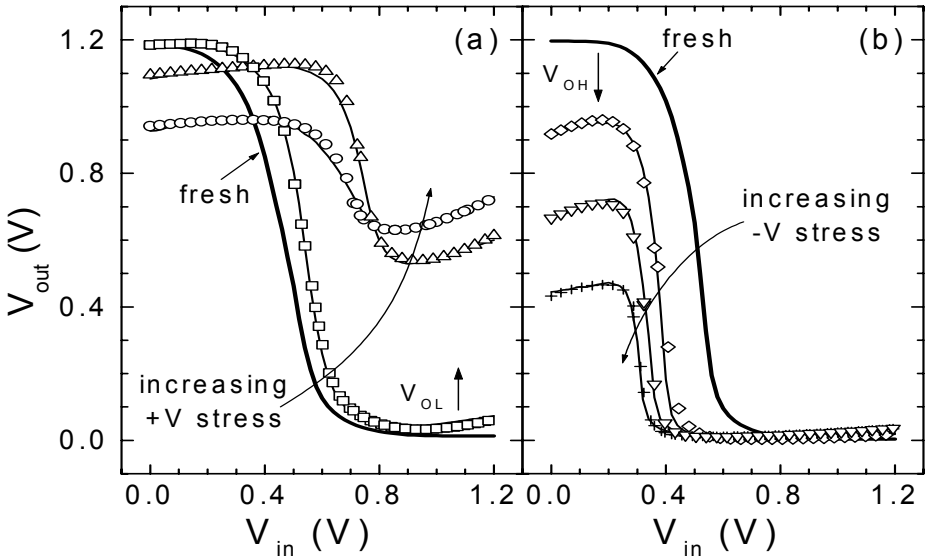
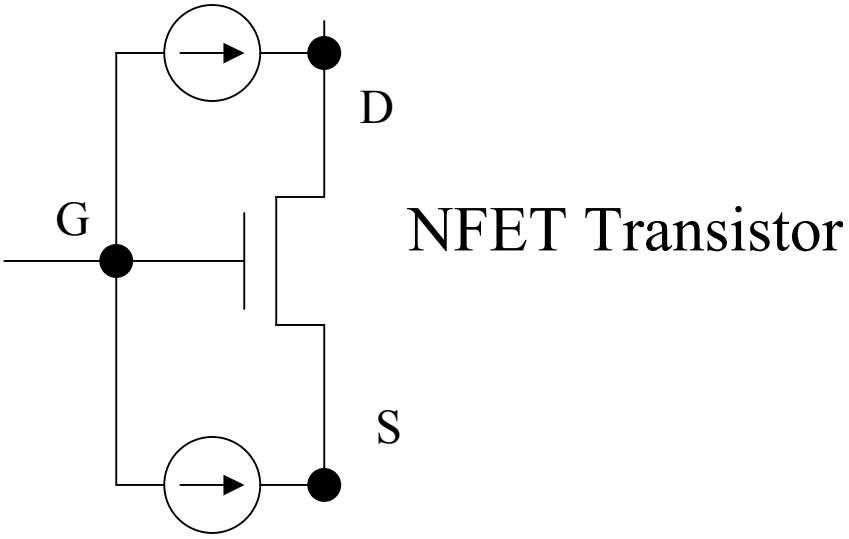

(a)
(b)
fresh
fresh
increasing
+V stress
increasing
-V stress
V_{OL}
V_{OH}
V_{out} (V)
V_{in} (V)
V_{in} (V)
0.0
0.4
0.8
1.2

Figure 2

$$\Delta I = K(V_{gd})^p$$



$$\Delta I = K(V_{gs})^p$$

Figure 3

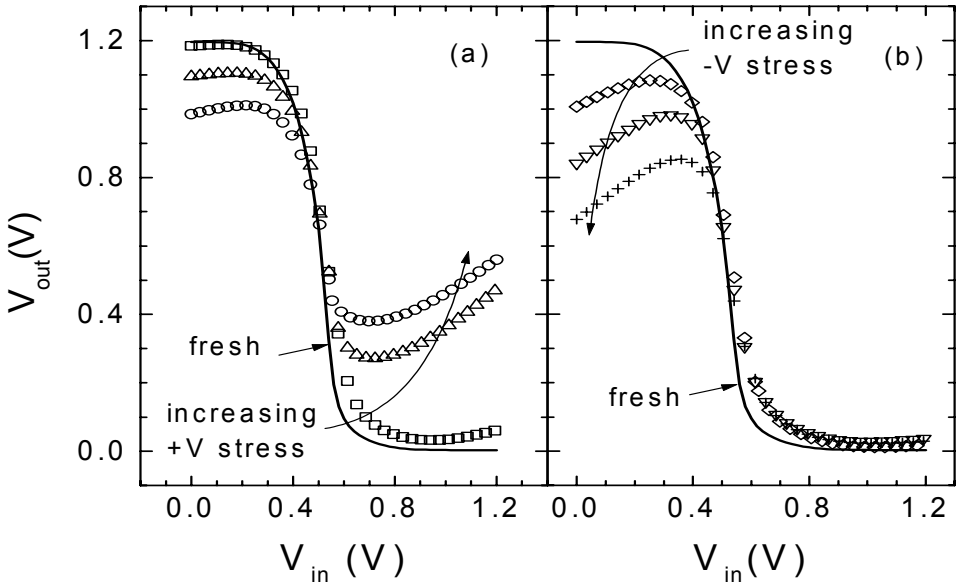

1.2
0.8
0.4
0.0
V_{out}(V)
(a)
fresh
increasing
+V stress
0.0
0.4
0.8
1.2
V_{in} (V)
increasing
-V stress
(b)
fresh
0.0
0.4
0.8
1.2
V_{in}(V)

Figure 4

Positive stress on inverter input						Negative stress on inverter input					
$I=K(V_{gd})^P$		Output High		Output Low		$I=K(V_{gd})^P$		Output High		Output Low	
		K	p	K	p			K	p	K	p
Increasing +V stress ↓	□	$1.2\cdot10^{-6}$	5	$1.2\cdot10^{-5}$	5	Increasing -V stress ↓	◇	$3\cdot10^{-5}$	5	$3\cdot10^{-6}$	5
	Δ	$1.5\cdot10^{-5}$	2	$3\cdot10^{-4}$	3		∇	$1.2\cdot10^{-4}$	5	$9\cdot10^{-6}$	3
	O	$3.5\cdot10^{-5}$ $2.8\cdot10^{-5}$	2 1	$3\cdot10^{-4}$	2		+	$3\cdot10^{-4}$	4	$7\cdot10^{-6}$	3

Table I