RC22657 (W0212-008) December 2, 2002
Electrical Engineering

IBM Research Report

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Alina Deutsch, [1] Howard Smith, Gerard V. Kopcsay, [2] Byron L. Krauter, Christopher W. Surovic, [2] David J. Widiger

IBM Research Division
T. J. Watson Research Center,
Yorktown Heights, NY 10598

[1] IBM System Development Laboratory,
Poughkeepsie, NY 12601

[2] IBM Microelectronics,
Austin, TX 78758

Research Division
Almaden - Austin - Beijing - Delhi - Haifa - India - T. J. Watson - Tokyo - Zurich

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IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598
[1]IBM System Development Laboratory, Poughkeepsie, NY 12601
[2]IBM Microelectronics, Austin, TX 78758
Phone: (914) 945-2858, Fax: (914) 945-2141, email: deutsch@us.ibm.com

Abstract

This paper discusses the effects of the frequency-dependent losses in the reference return path for wide, on-chip data buses, that must be understood in order to accurately predict the interaction and summation of crosstalk and common-mode noise signals. This interaction can generate excessive noise for on-chip global interconnections. Measured and simulated results are shown for representative 8-12 line couplings and circuit-synthesis techniques are shown to capture the correct *R(f)L(f)C* behavior of the reference series impedance.

Keywords: VLSI chip design, lossy, on-chip transmission-lines, common-mode noise

Introduction

Current-day and anticipated microprocessors have multi-GHz clock frequencies, and have large cache memories on the die. Communication between cache and CPU often requires 32-256-bit buses with data switching simultaneously on all these global on-chip interconnections. The high-level of integration afforded helps reduce the lengths of such paths, however, the increasingly larger caches are pushing the units farther apart. Typical lengths even for very large die sizes are in the order of 3-5 mm and most often use the topmost 2-4 layers in a hierarchical on-chip wiring structure as advocated for high-performance processors in [1]. The unbuffered lengths are restricted to 3-5 mm in order to achieve the multi-GHz clock frequencies on such low resistance interconnections (R < 100 Ω/cm, and $Z_{drv} < Z_o/2$, where Z_{drv} is the effective driver impedance). It has been shown in [1], that it is necessary to take frequency-dependent losses into account in order to accurately predict crosstalk, propagated risetime, and delay on such interconnections. The guidelines in [1] for less than 25% prediction error compared to simple distributed RC-circuit representation are as follows. For crosstalk, $Rl/2Z_o<1$ and lines driven by $Z_{drv} <1.5Z_o$; for risetime, $Rl/2Z_o < 1$ and $Z_{drv} < Z_o$; for delay, $Rl/2Z_o<0.5$ and $Z_{drv}<0.5Z_o$. The magnitude of the prediction error decreases from crosstalk, to risetime, and then to delay. Most researchers, however, address the issue of delay prediction as seen, for example, in [2]. Moreover, only inductive effects are primarily addressed. It has been shown in [1] that in order to accurately predict noise for global on-chip interconnections it is necessary to understand the frequency-dependence of both the resistance and inductance (or the series impedance $Z(w) = R(w) + jwL(w)$, where $w = 2pf$) of the reference path for these wiring. In [1], the frequency-dependent simulation methodology is explained for both crosstalk noise and noise on wide data buses and [3] shows a CAD-tool implementation.

This paper extends the analysis of common-mode noise in [1]. It further describes the frequency-dependent losses that need to be simulated and the circuit synthesis technique that can be used to capture this behavior. Measurement examples are shown to validate the design and analysis methodology. It is shown that while frequency-dependent losses are most important for crosstalk predictions (compared to risetime and delay), when both crosstalk and common mode noise are present, the noise amplitudes become excessive, and can cause costly product failures and redesign.

Why do we need both *R(f)* and *L(f)* variation ?

Reference [1] has explained in great detail the need for frequency-dependent *R(f)L(f)*C-circuit representation in order to accurately capture the crosstalk noise on wiring for which $Rl/2Z_o$ <1 and Z_{drv} $<1.5Z_o$. In all the previous work, the implicit assumption is that we are addressing on-chip interconnections for which the length is comparable to the signal wavelength λ, or propagation delay tl @ t_r. Moreover, in order to achieve GHz clock frequencies on such lossy transmission lines, these lines need to be driven by large devices that have low effective Z_{drv}, hence $Z_{drv} < Z_o$, and the lines have limited resistive losses such that an *LC* behavior dominates [1], and hence $Rl/2Z_o<1$. The following study then should not be applied to typical minimum-ground rule lines, for which distributed RC-circuit analysis is adequate. It is, however, shown in [1], that achieving multi-GHz frequencies, necessitates the use of low resistance lines, with very few repeaters, instead of the present practice of many small buffers and short resistive lines. The multi-GHz operation, as was explained in [1] and [3] also dictates the use of well-controlled transmission line structures for the medium length and global wiring. This implies an ample supply of V_{dd} and GND conductors that provide a low-resistance current return path. This methodology has to permeate to the design engineers, the chip layout, and the CAD tool methodologies.

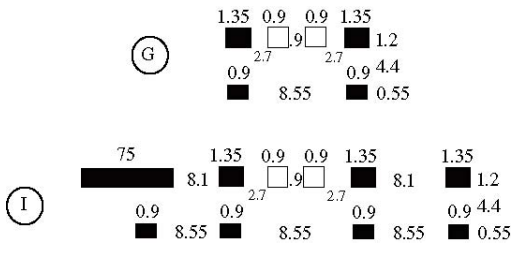

Fig. 1 Case G) One power-bay configuration, Case I) three power-bay configuration for the return current path around the two signal lines.

TABLE I
FREQUENCY VARIATION OF R(f) AND L(f) MATRICES FOR CASES G AND I OF FIG. 1

Case G

f (GHz)	L_{11}	L_{12} (nH/cm)	$L_{10}=L_{11}-L_{12}$	$R_{10}=R_{11}-R_{12}$ (Ω/cm)	R_{12}
0.001	5.636	2.915	2.721	188.9	50.4
10.00	5.572	2.953	2.619	194.2	51.7
∞	4.577	2.665	1.912	∞	∞

Case I

f (GHz)	L_{11}	L_{12} (nH/cm)	$L_{10}=L_{11}-L_{12}$	$R_{10}=R_{11}-R_{12}$ (Ω/cm)	R_{12}
0.001	10.323	7.683	2.640	188.9	2.10
10.00	5.525	2.906	2.619	193.9	33.5
∞	4.489	2.577	1.912	∞	∞

Two examples are shown in Figs.1a and b for two coupled lines on the topmost layer. The lines have R_{dc} = 189 Ω/cm and 0.9 μm width and space. They are placed centrally between a V_{dd} and GND power bay having GND conductors with width w = 1.35 μm and space = 2.7 x 2 + 0.9 x 3 = 8.1 μm. On the same layer, wide power buses of w = 75 μm, are also present to connect to solder balls or wire bonds as shown in Fig. 1b. Narrower and thinner ground lines, two layers below, are also shown and orthogonal wiring (not shown) is present one layer below. TABLE I shows the comparison of calculated *R(f)* and *L(f)* for the two cases for f = 0.001 and f = 10 GHz and infinite frequency. L_{10} and R_{10} are the signal line self-inductance and resistance while R_{12} refers to the effective resistance of the reference GND and V_{dd} conductors on the topmost layer and two layers below in Fig. 1. Note that $R_{12}(f)$ has a totally different behavior for Fig.1a from Fig. 1b where the effect of the low resistance 75-μm-wide power bus is taken into account and similarly the $L_{12}(f)$ variation and thus the inductive coupling. Fig. 1a does not capture the correct frequency-dependent current distribution in the return path that causes far-away conductors to affect the *R* and *L* values. At high-frequency, all the current crowds nearest to the signal lines due to proximity-effect, and only the case of Fig. 1a is needed in modeling.

a)

b)

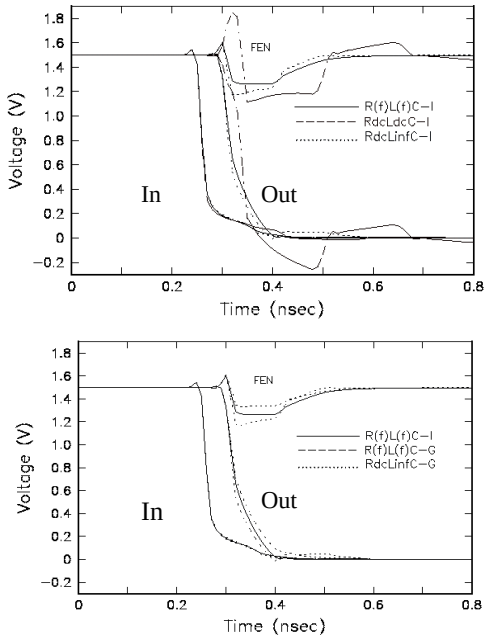

Fig. 2 Simulated waveforms for 5-mm-long lines, Z_{drv} = 25 Ω, showing input to the active line, at the end of the active line, and far-end crosstalk, FEN, on the quiet line for a) case I in Fig. 1 and b) cases I and G.

Simulated waveforms are shown in Fig.2 for the two cases of Fig. 1 for the two adjacent signal lines, for propagated signals, and for crosstalk monitored at the far-end of the quiet line. In Fig. 2a, simulations are shown for the Fig. 1b configuration. Notice that using R_{dc} with L_{dc} (in this case the 1MHz value of TABLE I) results in much higher line Z_o, larger delay, faster risetime, and thus much higher crosstalk prediction than the correct, broadband simulation. The use of R_{dc} and $L_{¥}$ predicts delay and risetime fairly well, however, over predicts crosstalk. In Fig. 2b, the correct simulation, namely, *R(f)L(f)C* for the case of Fig. 1a over-predicts risetime and delay and under-predicts noise, while R_{dc} and $L_{¥}$ for Fig. 1a, over-predicts crosstalk.

It is crucial to understand the implications for these different cases. There are several CAD tools available today that include "inductive" effects for on-chip interconnections. They either use the low-frequency inductance calculated with simple formulas, or attempt to include some simplified frequency-dependence but only for near-by, small radius power-grid extent unlike reference [3] where the correct, far-reaching reference and broadband analysis is performed.

Multi-line frequency-dependent simulation methodology

It has been shown in [1], that a distributed model using lumped-element circuit segments of a specific network topology can be created which is valid over a restricted frequency range. Fig. 3 shows such a model using dependent voltage sources that provides an efficient simulation methodology. This distributed network synthesizes the series impedance *Z(f)* and shunt admittance *Y(f)* behavior that is obtained using a three-dimensional field-solver that can extract the per unit length *R(f), L(f), C(f)*. Each of the self and mutual terms, $Z_{ii}(f)$ and $Z_{ij}(f)$ are synthesized using Foster-type, low-pass filters with cut-off frequencies $fc_i = R_i/2pL_i$. Fig. 3 shows only one such filter for the $Z_{11i}(f)$ term, for example. The terms $Z_{12i}(f)$ and $Z_{13i}(f)$ are represented by dependent voltage sources V_{12i} and $V_{13i.}$ The current through these voltage sources depends on the current flowing in conductors 2 and 3 or $V_{ij} = Z_{ij} I_i$. The terms $Z_{ij}(f)$ usually require 2-3 filters due to the larger frequency variations exemplified in TABLE I. Reference [1] shows validation examples for this circuit synthesis approach for four and six coupled lines, and for crosstalk noise and common-mode noise from far-away conductors. It is explained in [1], that common-mode noise is generated for on-chip, wide data-buses, switching in unison that have a finite impedance of the return current path through GND and V_{dd} conductors. At low frequencies, all the drivers switching simultaneously, will generate large current surge on the GND and V_{dd} lines. This is not to be confused with delta-I noise. It is assumed that enough decoupling capacitors are placed around these driver circuits so that they have the necessary initial charge and are able to switch with fast risetimes. This current that is set-up on the return path, will have a frequency-dependent distribution that will generate unusual propagation modes that are configuration dependent and hard to predict. Because of this, the frequency dependence of the mutual terms $R_{ij}(f)$ and $L_{ij}(f)$ can exhibit non-monotonic increase with frequency. The noise that is determined by this effective resistive "drop"

in the R_{ij} path will have a polarity opposite to the direction of switching of the signal on the active line. This common-mode-noise could therefore add or subtract to/from the traditional crosstalk noise from adjacent lines. This additional noise will be determined by far-reaching switching activity, unlike the capacitive coupling, and be directly affected by the supply of GND and V_{dd} lines.

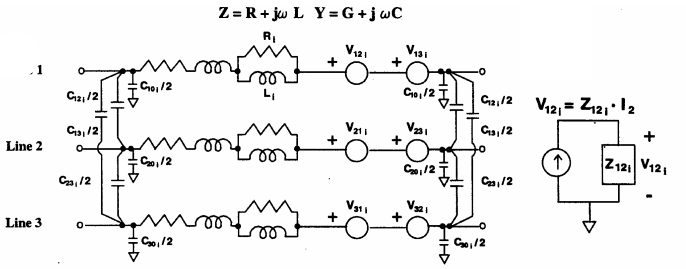

Fig. 3 One section of a distributed three coupled-line network. Each line series impedance *Z(w)* is represented by Z_{ii} terms in series with current dependent voltage sources V_{ij} as shown in detail for $V_{12i} = Z_{12i}I_2$ and synthesized using Foster filters.

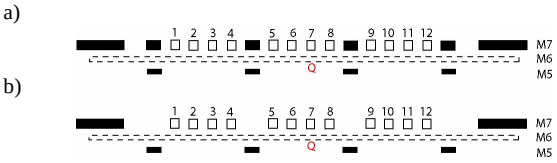

Fig. 4. Twelve coupled line data bus on topmost layer with reference GND and V_{dd} (dark) lines on topmost layer and two layers below of a seven-layer stack. Signal lines have R = 135 Ω/cm. Structures are shown with a) 1.26-µm GND lines and b) without.

An example is shown in Fig. 4a with twelve coupled lines on the topmost layer that have reference GND lines on the same layer and two layers below. Fig. 4b shows the same case without the narrow GND on the topmost layer. Fig. 5a plots the $R_{67}(f)$ and $R_{17}(f)$ for the two cases. Notice the much higher R_{17} and R_{67} values for the case without the narrow GND lines and the non-monotonic behavior for the $R_{17}(f)$ terms. Similarly the inductive $L_{ij}(f)$ will exhibit unusual modal behavior. In this case, as was shown in in-press [4], non-physical negative circuit elements *–R, -L* have to be used to synthesize the circuit of Fig. 3 as shown in Fig. 6a. It is shown in in-press [4], that a circuit transformation can be used to replace this configuration with a parallel *RC* circuit (Fig. 6b) such that the total R is positive. A parallel *RLC* circuit as shown in Fig. 6c can also be used. In all cases, the series impedance Z_{ij} is represented by a ratio of polynomials that fits the $Z_{ij}(f)$ calculated using a field–solver. The fit can be obtained by using the frequency domain Prony method and a least squares matrix linear equation solver as explained in in-press [4]. The solution using this circuit is valid for a limited frequency range but it is guaranteed to be stable and passive. It can be extended in frequency by adding more poles and it does not need to use complex model-order-reduction techniques.

Results and Discussion

Measurements were made on an eight-layer on-chip wiring stack with eight coupled lines having the cross section shown in Fig. 7.

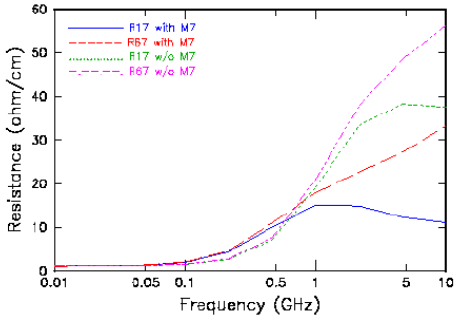

Fig. 5. Calculated $R_{17}(f)$, and $R_{67}(f)$ for the two cases of Fig. 4.

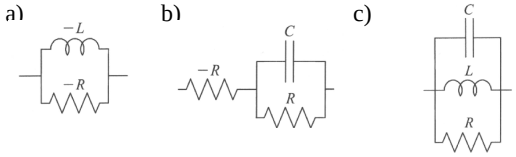

Fig. 6. a) Single-pole Foster filter *RL* circuit with negative elements, b) with negative resistance in series with single-pole *RC* circuit, and c) parallel *RLC* circuit.

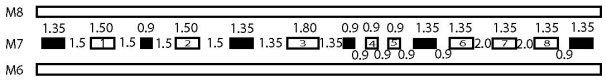

Fig. 7 Cross-section of eight coupled-line configuration on layer M7 of eight-layer stack. All lines are 1.2-µm thick.

TABLE II
MEASURED FAR-END CROSSTALK FOR LINES OF FIG. 7 IN PERCENTAGE OF INPUT SWING ON ACTIVE LINE.

Gnd 0 **I** 0 **Gnd** 0 **I** 00 **Gnd** A Q A **Gnd**	-3.7% / +12.0%
Gnd 0 **I** 0 **Gnd** 0 **I** 00 **Gnd** AQ 0 **Gnd**	-1.9% / +6.3%
Gnd 0 **I** 0 **Gnd** 0 **I** 0A **Gnd** 0 Q 0 **Gnd**	-2.0% / +0.7%
Gnd 0 **I** 0 **Gnd A I** 00 **Gnd** 0 Q 0 **Gnd**	-1.2% / +0.6%
Gnd 0 **I** 0 **Gnd 0 I** AQ **Gnd** 0 0 0 **Gnd**	-0.0% / +10.0%
Gnd 0 **I** 0 **Gnd A I** Q 0 **Gnd** 0 0 0 **Gnd**	-3.0% / +0.8%

Orthogonal wiring and ground conductors are placed above and below layer M7 and the power bay of 11.25-µm-pitch is repeated 23 times on both sides of the configuration shown. Each power bay, with 1.35-µm ground conductors, has additional interstitial ground lines, I, that are 0.9-um-wide and placed as shown. 250-mV-amplitude and 29-ps-risteime input step source was used on the active lines, A, and the noise was monitored at the far-end of the quiet line, Q. TABLE II shows some typical results. Several conclusions can be made. Crosstalk from adjacent lines is the highest, 10-12% shown. Common-mode noise decays extremely slowly with distance. It depends on the presence of ground conductors. This supply sets up the noise generation. The fewer the ground lines, the higher the common-mode noise. The interstitial ground lines only shield capacitively. The inductive contribution decays very slowly, and thus, even at a distance of 14 µm, the noise was still –1.2% for two lines (or –2.4% if we had 8 more lines to the right of Q). The least resistive active line, 1.8-µm-wide, generates the highest noise since it switches the fastest.

Simulations were also made with driver and receiver circuits for the 12-line configurations shown in Fig. 4a on the top most layer of a seven-layer stack. The lines are 1.26 µm-wide with 1.26 µm spacing, 1.2 µm thick. The power bay has 12-µm pitch with 1.26-µm-wide ground lines and 75-µm-

wide power lines on 396 µm pitch. V_{dd} in this case is 1.5V. Noise is once again monitored at the end of the quiet line Q and the driver impedance has an equivalent impedance of Z_{drv} = 25 Ω. TABLE III shows the results. Case A has the worst summation of far-end crosstalk and common-mode-noise. Case B shows a subtraction of the two contributions. Common-mode noise decays very slowly with distance as seen in Case C. Even at one and a half power bays away, or 15 µm from the center, the noise is still 3-5% of V_{dd}. The ratio of 4:1 of ground to signal lines is insufficient. Common-mode noise is proportional to length (Case D) and is substantial even for Z_{DRV} = 200 Ω (Case E). Common-mode noise increases by up to 321 mV for the case of Fig. 4b compared to Fig. 4a.

TABEL III
SIMULATED COMMON-MODE AND FEN CROSSTALK INTERACTION FOR THE STRUCTURE OF FIG. 4A

A.	---- -+Q+ ----	+771 mV / -171 mV	l = 5mm	Zdrv = 25 Ω	CMN+FEN
	0000 0+Q+ 0000	+362 mV / 0 mV	l = 5mm	Zdrv = 25 Ω	FEN
	---- -0Q0 ----	+493 mV / -205 mV	l = 5mm	Zdrv = 25 Ω	CMN
B.	---- --Q- ----	+313 mV / -270 mV	l = 5mm	Zdrv = 25 Ω	CMN-FEN
C.	000- 00Q0 -000	+162 mV / -72 mV	l = 5mm	Zdrv = 25 Ω	CMN
	0-00 00Q0 00-0	+74 mV / -47 mV	l = 5mm	Zdrv = 25 Ω	CMN
D.	---- -0Q0 ----	+401 mV / -217 mV	l = 3mm	Zdrv = 25 Ω	CMN
	---- -0Q0 ----	+171 mV / -172 mV	l = 1mm	Zdrv = 25 Ω	CMN
E.	---- -0Q0 ----	+370 mV / -125 mV	l = 5mm	Zdrv = 50 Ω	CMN
	---- -0Q0 ----	+204 mV / -58 mV	l = 5mm	Zdrv = 100 Ω	CMN
	---- -0Q0 ----	+100 mV / -40 mV	l = 5mm	Zdrv = 200 Ω	CMN

TABLE IV compares the results obtained by synthesizing a full twelve-line model with the pair-wise summation of noise. The full, twelve-line model required synthesis of 78 matrix elements. The pair-wise summation uses only two line circuit models and the waveforms are summed. The summation of all the noises is surprisingly linear in TABLE IV. If the polarities and timings of all the waveforms are summed correctly, the summation is very close to the group-synthesis result. All the lines are 5-mm-long and Z_{DRV} = 25 Ω. The error between pair-wise summation and group modeling exceeds 20% for a separation of 6.3 µm between active and quiet line.

TABLE IV
COMPARISON OF PAIRWISE SUMMATION VS. GROUP SYNTHESIS FOR THE LINES OF FIG. 4A

0000 0+Q0 0000	-133 mV / +195 mV			Pairwide synthesis
0000 00Q+ 0000	-46 mV / +152 mV			Pairwise synthesis
0000 -0Q0 0000	-39 mV / +178 mV			Pairwise synthesis
000- 00Q0 0000	-23 mV / +85 mV			Pairwise synthesis
0000 0+Q+ 0000	-55 mV / +361 mV	-----		Group synthesis
0000 0+Q+ 0000	-172 mV / +344 mV	-5%		Addition of pairs
0000 -+Q+ 0000	0 mV / +377 mV	-----		Group synthesis
0000 -+Q+ 0000	-55 mV / +394 mV	+5%		Addition of pairs
000- -+Q+ -000	-46 mV / +529 mV	-----		Group synthesis
000- -+Q0 -000	-70mV / +585 mV	+11%		Addition of pairs
00-- -+Q+ --00	-102 mV / +627 mV	-----		Group synthesis
00-- -+Q0 --00	-121 mV / +759 mV	+21%		Addition of pairs

This refers to the wide, in-phase portion of the noise. The narrow, out-of-phase peaks, tend to have larger discrepancies. In the case of near-end configuration, with the quiet receiver close to the driving end, the radius drops to 5 µm. Some representative waveforms are shown in Fig. 8.

a)

b)

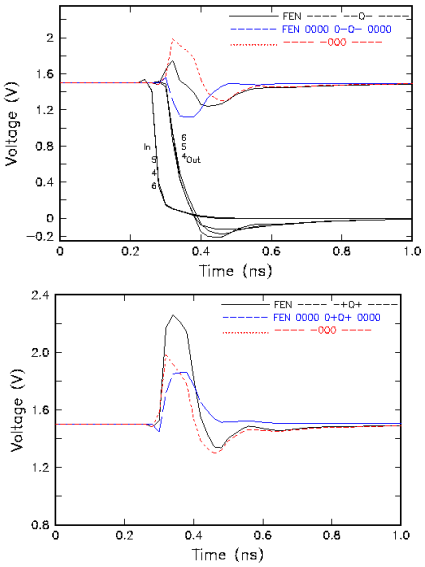

Fig. 8. Simulated waveforms for l = 5 mm, Z_{drv} = 25 Ω, for the lines of Fig. 4a, a) for Case B in TABLE III when noises subtract, and for b) Case A in TABLE III when noises add.

In conclusion, it is important to model the frequency-dependent behavior of the series impedance for the signal lines and their return path in order to accurately capture the interaction between crosstalk and common-mode noise on wide data buses. Such analysis shows that it is necessary to provide adequate ground and V_{dd} lines between the signal lines to reduce the inductive coupling and the effective resistive losses in the return path. For the cases shown and depending on the ratio of ground-to-signal lines, the common-mode noise was as high as 13-33% for far-end and 7-24% for near-end configurations. Far-switching lines can add 3-5% of noise even at a distance of 15 µm. Multi-line simulation is necessary for radii greater than 5-µm. While wide data-buses might have variable data patterns that reduce the summation of all the switching currents, the additional common-mode noise that is generated cannot be ignored. It can add significant contribution to crosstalk to exceed the available noise budget and cause logic failure. It is the contribution of the two noise sources that is the most worrisome. As buses become wider and risetimes are shorter, accurate noise prediction becomes imperative and CAD tools need to be extended to take into account the frequency-dependent losses for on-chip transmission lines. Simple "inductance" analysis needs to be expanded to *Z(f)* analysis for the series impedance of both the signal lines and their return path.

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