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Hot-Carrier Charge Trapping and Trap Generation in HfO_2 and Al_2O_3 Field-Effect Transistors

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Abstract

We present a comprehensive experimental study of hot-carrier trap generation and charging effects in high-κ dielectrics using field-effect transistors fabricated with HfO_2 and Al_2O_3 gate insulator stacks and poly-crystalline silicon gates. The experiments utilize substrate injection of hot carriers generated either optically or by direct injection in the dark from a forward-biased p-n junction. Comparison of charge-trapping measurements taken using these two techniques on nFETs and pFETs finds that enhanced charge trapping occurs when hot holes are present (in the light or in the dark in pFETs but only under illumination in nFETs). A fundamental understanding of the conditions for hot-carrier damage in nFETs is obtained by studying the dependence on light wavelength, temperature, and substrate bias. In particular, the wavelength dependence reveals that the hot-carrier damage depends on a combination of the electron and photon energies. Study of the time dependence of the gate current indicates the buildup of positive charge in the dielectric during stressing. The density of interface traps generated by hot-carrier stressing is estimated using the capacitance-voltage characteristic, and charge transfer experiments to probe the existence of slow states are performed. Finally, the experimental findings are discussed in the context of a speculative picture in which hot holes act as a precursor to damage in the oxide.

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I. INTRODUCTION

Hot-carrier effects and insulator degradation have been extensively studied in metal-oxide-semiconductor (MOS) devices to understand and predict device reliability [1, 2]. Continued scaling of device dimensions has led to greater emphasis on such issues, and indeed fundamental limits imposed by gate leakage and intrinsic reliability are expected to prevent reduction of the thickness of the SiO_2-based gate dielectric in MOS devices below $\sim$1.2 nm [2]. As a result, there is currently an intense effort to study alternative high-κ gate dielectrics in which the insulator physical thickness can be increased due to the higher static dielectric constant κ, reducing leakage while maintaining adequate gate control over the channel [3, 4]. Even though reduced energy band offsets are a well-known property of high-κ insulators (typically decreasing with increasing κ) [5], prompting concern that hot-carrier reliability could be a serious issue, to date only a preliminary study of hot-carrier effects has been carried out [6]. On the other hand, effects due to charge trapping of cold carriers (those injected by the gate insulator field), such as hysteresis in capacitance-voltage (C-V) characteristics, have been commonly observed in many studies of high-κ dielectrics [3],[7]-[13]. Together with experimentally observed fixed charges and reduced mobilities [3], both of which may be unavoidable [14, 15], they are among potential challenges to adoption of high-κ materials. In this work, we have chosen two high-κ gate dielectrics, Al_2O_3 and HfO_2, which have been widely investigated as potential SiO_2 replacements due to their relatively wide bandgaps, thermal stability, and high permittivity [3, 4], to carry out a comprehensive study of hot-carrier effects.

Trapping of positive charge in the oxide is thought to play a fundamental role in oxide degradation, but even in SiO_2 the origin of the positive charge remains subject to controversy [2]. Hydrogen release [1, 16] and trapped holes [17], both of which have been used in models of SiO_2 degradation, have both been invoked to explain findings in studies of high-κ dielectrics [7, 9, 12, 18]. In our earlier work [6], hot-carrier stressing was found to result in enhanced charge trapping in p-channel field effect transistors (pFETs), but similar effects were seen in n-channel field effect transistors (nFETs) only under illumination, when hot holes, in addition to hot electrons, are likely to be present. These findings suggest that holes play an important role in enhanced charge trapping under hot-carrier stress.

The purpose of this work is to obtain a fundamental understanding of when hot-carrier

effects occur in high-κ dielectrics and to gain some insight about the nature of the damage created. Section II describes our experimental setup and Sec. III presents the main experimental findings of this paper. Section IV is the discussion and Sec. V is the summary and conclusion.

II. EXPERIMENTAL SETUP

We characterize the charge trapping by plotting the shift in the flatband (ΔV_{fb}) or threshold voltage (ΔV_t) as a function of the fluence, or total charge injected into the gate, Q_{inj}. The shifts (ΔV_{fb}) and (ΔV_t) are obtained from measuring the high frequency capacitance-voltage (C-V) characteristic at preset interruptions of the constant voltage stress. In cold-carrier stressing, a substantial overdrive $|V_g - V_t|$ of the gate voltage V_g above the threshold voltage V_t results in carrier injection by the gate insulator field. The band diagram under stress from substrate hot electrons is shown in the inset of Fig. 1(a). The band bending, which determines the energy of the incident carriers, is set by a reverse bias to the substrate $V_x < 0$ while the condition $V_g \sim V_t$ insures that the channel is nearly equipotential. (Source/drain contacts are always kept at ground.) An essential feature of our hot-carrier stressing technique is that we have used both optical generation of electron-hole pairs [19] and direct injection of minority carriers from a nearby forward-biased p-n junction [20] in order to compare charge trapping in the light to that in the dark. In order to insure that hot carriers are dominant in hot-carrier stressing experiments, we require that the gate current due to cold carriers (i.e., with no substrate bias, illumination, and p-n injector bias) must be a small component (less than 20 per cent) of the total gate current [32].

Table 1 shows a summary of the samples used in this work. To understand more completely the effects discussed here we have used both HfO_2 and Al_2O_3 gate stack devices (Al_2O_3 pFETs were not available due to boron penetration [3]) with polysilicon (polycrystalline silicon) gates. Following atomic layer deposition [3] of either HfO_2 or Al_2O_3 on the same ultrathin oxynitride layer thermally pregrown on (100) Si substrates, polysilicon gate electrodes were deposited. Along with junction formation, the gate electrodes were degenerately (10^{20} cm^{-3}) doped (n^+ for nFETs; p^+ for pFETs), followed by dopant activation and first level of metal contact using a conventional CMOS process flow. Measurements were taken either on 100x100 μm^2 or 50x50 μm^2 FETs, and each new stressing measurement

was done on a fresh device.

III. EXPERIMENTAL RESULTS

An overview of this section is as follows. First, we show that illumination is essential to observation of enhanced charge trapping in nFETs, but not in pFETs. Second, having established the role of illumination in nFETs, we investigate the dependence of the charge trapping on wavelength by restricting the maximum photon energy of the light. Third, we examine the gate current, whose increase with time during hot-electron stressing suggests the buildup of positive charge in the dielectric. Fourth, we study the temperature and substrate bias dependences. Fifth, we consider an experimental test of whether the enhanced charge trapping seen after hot-hole stressing in a pFET represents a reversible filling of pre-existing trap states at high energies or, in fact, real damage in the gate insulator. Sixth, we look in detail at interface-state generation and conduct a charge transfer experiment in which charge is moved into and out of the created states by the application of appropriate gate bias. Finally, we consider whether the hot-carrier effects seen here can also be observed using cold carriers at high gate insulator fields.

A. Effect of illumination: nFETs *vs.* pFETs

Figure 1 summarizes the main results of our earlier study [6] using HfO_2 nFETs (Fig. 1(a)) and HfO_2 pFETs (Fig. 1(b)). The figures show plots of flatband voltage shift (obtained from 500 kHz C-V) as a function of injected charge, comparing trapping due to cold carriers, hot carriers generated by light, and hot carriers generated in the dark using the forward-biased p-n injector. In the cold stressing experiments (with no substrate bias), the stressing gate voltage was chosen to give approximately the same gate current as obtained under the hot stressing conditions so that comparable amounts of charge would be injected. Figure 1(a) also shows that under comparable hot stressing conditions, essentially no damage is observed in the SiO_2 control wafer (wafer S1).

The important features to note are:

(1) For pFETs, the flatband shifts are much larger for hot carriers than for cold carriers, independent of whether the hot carriers are generated by light or by direct injection in the

dark. The shifts under illumination are modestly smaller than those in the dark, possibly due to photo-detrapping.

(2) For nFETs, the enhanced charge trapping of hot carriers occurs *only when the carriers are generated by light*; the shifts obtained by hot-electron stressing in the dark are comparable to or even smaller than those due to cold carriers.

(3) For pFETs, there is a very strong dependence on substrate bias V_x, with markedly stronger charging at $V_x = 3$ V than at $V_x = 2$ V, using hot carriers in the dark. For nFETs, little difference is observed for hot carriers in the dark, even as the substrate bias is changed from V_x=-2 V to V_x=-6 V.

Each of the key features noted for HfO_2 nFETs has also been observed in Al_2O_3 nFETs, as shown in Ref. 6. Also, to check that illumination alone was not responsible for the enhanced trapping, no enhanced trapping was observed under cold-carrier stressing with the light on; this point is further discussed in Sec. III G.

B. Wavelength dependence in nFETs

The enhanced charge trapping in nFETs observed under illumination depends on the wavelength, or, equivalently, photon energy, of the light. We can restrict the maximum photon energy $h\nu_c$ by using Long Pass Schott colored glass filters which pass all incident wavelengths above a cut-on wavelength $\lambda_c = c/\nu_c$ [33]. A study of the wavelength dependence is complicated by the fact that more restrictive (higher λ_c) filters require higher source intensities to generate reasonable gate currents, but the charge trapping is a strong function of light intensity even when plotted versus injected charge to account for differences in gate current. In order to circumvent this dependence on source intensity, we utilize a novel technique in which the gate current at given substrate bias V_x is fixed by the p-n injector forward bias of 1 V. We then illuminate the device with light of sufficiently weak intensity that the gate current is independent of the λ_c of the filter used.

Figure 2(a-c) shows results for HfO_2 nFETs. The threshold voltage shift ΔV_t (measured from the C-V near weak inversion) is plotted as a function of injected charge Q_{inj} at different combinations of V_x and $h\nu_c$. Since the pulse times used were the same for all curves in Fig. 2 (7 pulses, doubling in time, starting from 20 sec), the lack of dependence of gate current on λ_c can be seen by the near alignment of the data points along the Q_{inj} axis. At V_x=-2.25 V,

enhanced charge trapping evolves from being clearly visible when $h\nu_c$=2.7 eV to being close to the curve taken in the dark when the maximum photon energy is reduced to $h\nu_c$=1.5 eV. As the electron energy is decreased by lowering $|V_x|$, the required photon energy to see enhanced charge trapping is correspondingly increased.

Figure 3(a) shows that similar results are obtained in Al_2O_3 nFETs, although the Q_{inj} scale where effects are observed is somewhat higher than in wafer H1. (As discussed in Sec. III F, $\Delta V_{fb} \approx \Delta V_t$ for Al_2O_3 nFETs.) Figure 3(b) shows the cutoff behavior in a slightly different way, by comparing curves taken using the same filter (λ_c=455 nm, or $h\nu_c$ =2.7 eV) at different substrate voltages.

In order to find an energy scale for the enhanced charge trapping phenomenon, we can characterize the data by empirical power-law fits of the form AQ_{inj}^{β}, as shown in Figs. 2-3. Figure 4 shows scatter plots of A and β (inset) as a function of some measure of total energy, $h\nu_c + eV_x$, for both HfO_2 and Al_2O_3 nFETs. For simplicity, we have neglected the voltage drop in the bulk which will reduce the energy of the incident hot electrons below eV_x and eventually limit it [1]. Also note that the units of the coefficient A depend on β, a complication we ignore here since β changes only weakly. The HfO_2 nFETs show a clear turn-on behavior in A at around $E_{tot} \approx 3.8$ eV while β also shows a weak trend to increase. A weak increase in A is also observed for Al_2O_3 nFETs, but the scale of A is small compared to that for HfO_2 nFETs.

C. Gate current as a probe of gate insulator charge in HfO_2 nFETs

The inset of Fig. 2(b) plots the mean gate current during each of the 7 stressing pulses for three different wavelengths. The enhanced charge trapping is accompanied by an increase in the gate current with time which can also be suppressed by restricting the maximum photon energy. Figure 5 compares the typical behavior of the gate current with time in a HfO_2 nFET during a stress consisting of several pulses under cold (V_g=1.75 V in the dark) and hot (V_x=-4 V in the light) stressing conditions. The discontinuities correspond to interruptions of the stress to perform a C-V measurement. Under cold stressing conditions, electrons which get trapped in pre-existing sites repel further incident electrons, resulting in a weak decrease of the gate current with time. In contrast, under hot stressing conditions, the gate current increases strongly with time. We interpret this increase as corresponding

to the buildup of positive charge in the dielectric during hot-electron stressing.

In contrast to the steep increase in the hot-electron gate current during stress, the tunneling gate current I_g^{cold} as a function of gate voltage V_g is almost unchanged. This is shown in the inset of Fig. 5 which plots I_g^{cold} as a function of V_g before and after the hot-electron stress used in the upper inset. The absence of change in the tunnneling gate current is consistent with the observation that the hot-electron gate current restarts at a much lower value following each interruption for a C-V measurement, suggesting that most of the positive charge exits the dielectric when the stress is removed. This dip in the hot-electron current after each interruption also helps us deem as unlikely another possible explanation for the increasing gate current: the formation of a defect chain, for which we would expect the current to resume its previous value following each interruption in the stress.

D. Temperature and substrate bias dependence in HfO_2 *n*FETs

Figure 6 (open symbols) shows the temperature dependence of charge trapping under hot stressing conditions (in the light) for HfO_2 nFETs. As a function of injected charge, the V_t shift decreases as the temperature is increased. Under cold tunneling conditions (in the dark), shown in the inset, a similar decrease of the charge trapping with increasing temperature is observed. Note also that the Q_{inj} scale is larger while the ΔV_t scale is smaller, reflecting the weaker trapping under cold stressing. Two simple explanations for the observed temperature dependence are thermal detrapping and the lowering of the electron temperature with increasing lattice temperature.

Figure 6 also shows the substrate bias dependence of charge trapping under hot stressing conditions for HfO_2 nFETs. The charge trapping shows a sharp increase as the substrate bias, and thus the energy of the incident electrons, is increased. This strong dependence under illumination is to be contrasted with the weak dependence found in the dark (see Fig. 1(a)), confirming that light appears to be essential for enhanced charge trapping.

As the substrate voltage is increased to V_x=-3 V, Fig. 6 shows that a clear saturation in ΔV_t is observed at high Q_{inj}. As suggested in Ref. 13, we find that the data can be empirically fit to a stretched exponential function of the form $\Delta V_t = \Delta V_{tm}[1 - \exp(-(\sigma_0 Q_{inj}/e)^{\beta})]$, with three fitting parameters whose values are shown in Table II. (Note from Fig. 1(a) that the saturation behavior observed in ΔV_t is not observed in ΔV_{fb} even at V_x=-6 V.)

In Ref. 13, which studied filling of pre-existing traps by cold carriers, ΔV_{tm} is interpreted as the saturation V_t shift, σ_0 as the average capture cross section, and β as an exponent which characterizes the distribution in capture cross sections. Note that in the limit of weak injection $\sigma_0 Q_{inj}/e \ll 1$, the stretched exponential with three fitting parameters reduces to the power law expression used above with $A = \Delta V_{tm}(\sigma_0/e)^{\beta}$. We emphasize that we only use the fits to characterize empirically our curves and remark that the physical interpretation may be different from that in Ref. 13 since we are dealing with trap generation, not just filling of pre-existing traps. As shown in Table II, we find that σ_0 is an increasing function of temperature at V_x=-3 V and a decreasing function of $|V_x|$ at 25 C.

E. Trap creation in a stressed *p*FET

We now consider an experimental test of whether the enhanced charge trapping seen in *p*FETs represents a reversible filling of pre-existing trap states at high energies or, in fact, real damage in the gate insulator. We choose to use *p*FETs here because we can controllably introduce hot holes into the insulator and then probe the damage by studying electron trapping in accumulation. In our earlier work [6] it was found that the flatband voltage of a *p*FET which had undergone hot-hole stressing in the dark could be restored to close to its unstressed value by shining light on it. This observation suggests that the existence of persistent damage done by hot-hole stressing can be tested by comparing electron trapping in accumulation on an unstressed *p*FET to that in a *p*FET which has undergone hot-hole stressing followed by restoration of the flatband voltage using light.

Figure 7 shows the results of two such experiments, carried out on two slightly different wafers, H2 and H2', and under slightly different conditions. In the first experiment (open symbols), the charge trapping in accumulation was measured on two different devices: an unstressed device and a device which had been first subjected to hot-hole stressing. The results show clearly that the charge trapping in accumulation is worse on a device subjected to hot hole stressing (open circles) than on a fresh sample (open stars). In the second experiment (solid symbols), the *same* device was used both before and after hot-hole stressing to convincingly verify the increased damage after stress. (The inset shows the charging during hot-hole stressing followed by the restoration using light.) As in the first experiment, increased trapping is apparent after stressing. Also noteworthy is that on wafer H2, positive

flatband shifts, to the right of the initial flatband, were commonly observed, clearly signifying new damage; however, on wafer H2', the flatband was not observed to shift to the right of the initial flatband, even after long-term (48 hour) measurement. Thus both experiments suggest increased electron trapping following hot-hole stressing, although the exact nature of the damage created is not clear.

F. Generation of interface states in nFETs

Stretchout of the high frequency C-V characteristic is a signature of the generation of states at or near the Si-gate insulator interface [21]. To quantify the stretchout, Fig. 8 plots the flatband and threshold voltage shifts as a function of substrate bias for HfO_2 and Al_2O_3 nFETs before and after hot-electron stressing (using light), with the stressing times chosen such that the injected charge is very approximately the same for each material. The two insets compare typical high-frequency (100 kHz) C-V's for the dielectric stacks of the two materials. In HfO_2 nFETs, a clear stretchout of the C-V curve is observed, with the left side near flatband essentially unchanged after stress and a large shift on the right side near threshold. The stretchout shows a pronounced increase with increasing $|V_x|$. In contrast, Al_2O_3 nFETs show a shift on both sides with much weaker stretchout apparent only at higher $|V_x|$.

Having clearly established the generation of interface states in HfO_2 nFETs by the pronounced stretchout, we use the combined high-low frequency capacitance method [21] to estimate the interface trap density D_{it} before stressing as well as the change ΔD_{it} resulting from hot-electron stressing [34]. Although our chosen low frequency (100 Hz) and high frequency (100 kHz) will exclude some trap states outside this range, we can nonetheless obtain a lower-bound estimate of the interface trap density D_{it}. Figure 9 shows $D_{it}(E)$ as a function of position in the gap E-E_i (E_i is the intrinsic level at the interface). The trap density is found to peak near the band edges, with a steep increase toward the conduction band edge. Errors in the capacitance in accumulation C_{acc} can lead to considerable uncertainty in $D_{it}(E)$, as indicated by the error bars in Fig. 9 which show the effect of changing C_{acc} by $\pm 3\%$ resulting in a $\pm 5\%$ change in the Si band gap from our base measured value of 1.19 eV. The inset shows the net change in D_{it} following hot-electron stressing (in the light at V_x=-4 V for 200 sec). The generated states are mostly within 60 meV of the conduction

band edge and have an integrated density of $(1.3{\pm}0.2){\times}10^{12}$ cm^{-2}, where the error estimate reflects the uncertainty in C_{acc}.

In general, the interface states can be loosely catagorized as "fast" states, which can quickly follow the applied voltage, and "slow" states, which give rise to hysteresis under long-duration bias but do not cause distortion of the C-V characteristic [22]. We perform a charge transfer experiment [22] to probe the existence of slow states, which have been associated with "anomalous positive charge" [22–24]. We begin with an Al_2O_3 nFET where hot-electron stressing (V_x=-6 V, 200 s, in the light) results in both a weak stretchout and a shift of the C-V characteristic. We then apply a non-destructive negative bias (which causes no damage by itself) to slowly depopulate the created states, perform a forward C-V sweep to a non-destructive positive bias, wait at the positive bias allowing some repopulation of the slow states, and do a reverse C-V sweep. We repeat this procedure, allowing charge to be transferred in and out of the slow states. We use a fixed charging hold time of 10 s at the positive bias (V_g=0.7 V), but progressively double the discharging time at the negative bias (V_g=-1.1 V), starting from 250 s and going up to 256000 s. Figure 10 shows the flatband and threshold voltage shifts during both the forward and reverse C-V sweeps as a function of the total discharging time. For easy comparison to the initial flatband shift ΔV_{fb}^0 created from hot-electron stressing, we normalize all voltage shifts to ΔV_{fb}^0=74 mV. First, we note that the normalized threshold voltage shifts start above unity, signifying stretchout. Second, we see that the separation between forward and reverse sweeps increases with time for both flatband and threshold. Third, at long detrapping times, the flatband shift becomes negative, which could arise from the created states becoming positively charged. However, it must be noted that at such long times, the detrapping voltage of -1.1 V was found to cause some shifting in a virgin sample comparable to that seen in the stressed sample. Thus, although we can clearly see the population and depopulation of the slow states by electrons, we unfortunately cannot determine whether the defects, once emptied, can also assume a positive charge state [22–24].

We have also tried similar charge transfer experiments using HfO_2 nFETs. Interestingly, we find that the flatband and threshold voltages remain nearly fixed at their values following hot-electron stressing (i.e., $\Delta V_{fb} \approx 0$ and ΔV_t large). Thus, in contrast to Al_2O_3 nFETs, the existence of slow states (or perhaps their time constants) remains an open question in HfO_2 nFETs.

G. Bias and polarity dependence in the cold tunneling regime in nFETs

We devote this final subsection on experimental results to test whether enhanced charge trapping can also be observed using cold electrons, injected by the gate insulator field. Some evidence for trap creation under cold stressing conditions is suggested both by the strong dependence of the V_t or V_{fb} shift on stressing gate voltage for the same Q_{inj} [13] and by our observation of stretchout in the C-V characteristic. Figure 11(a) shows the charge trapping in the cold tunneling regime at gate biases close to $V_{fb} + 1.1$ V for wafer H1 (V_{fb}=-0.75 V) and wafer A1 (V_{fb}=-0.55 V). It is seen for both HfO_2 and Al_2O_3 nFETs that the onset of charge trapping, which has a clear gate voltage dependence, is indeed close to an energy corresponding to a Si bandgap above flatband. As discussed further in Sec. IV, this voltage onset would correspond to the bare minimum energy required for an incident cold electron to create an electron-hole pair in the polysilicon gate by impact ionization.

In addition to a bias dependence, a polarity dependence has also been observed in Al_2O_3 [10] and ZrO_2 [7] gate stacks. Typically a smaller shift is observed for gate injection ($V_g < 0$) than for substrate injection ($V_g > 0$). In Fig. 11(b) we show the polarity dependence for HfO_2, taken at gate biases which are chosen to be symmetric about the flatband voltage V_{fb}=-0.75 V. Again, the charge trapping is seen to be stronger for substrate injection than for gate injection, which would be consistent with the larger energy barrier for holes entering from the substrate to the oxynitride.

However, in contrast to the results for hot electrons in nFETs, shining light on the sample causes no enhancement of the charge trapping under cold stressing conditions. As the gate voltage is increased, a negative current (positive flowing out of the contact) is measured at the substrate (see inset of Fig. 11(b)), as reported previously for SiO_2 [25]. If indeed this current consists of generated holes [25], one might expect the charge trapping to show an enhancement with light at such a bias; however, no such correlation between substrate current and charge trapping in the cold tunneling regime was seen even when the substrate current was significant. Thus we conclude that charge trapping under cold stressing conditions is probably dominated by the filling of pre-existing traps rather than by trap generation.

IV. DISCUSSION

We explain our results using a tentative, qualitative picture of the chain of processes which lead to the degradation of the high-κ stack. Considering that even in the case of SiO_2 – an insulator whose hot-carrier degradation behavior has been studied for over three decades – the anode hole injection [17] and the hydrogen-release [1, 16] models are still debated [2], "tentative" and "speculative" are adjectives which must necessarily accompany the discussion presented here.

We begin by recapping the key experimental observations in HfO_2 nFETs for hot-electron stressing under illumination. First, during hot-electron stressing, the hot-electron gate current increases, which we attribute to the buildup of positive charge. Second, the C-V characteristics show little flatband shift after stressing, implying charge neutrality near flatband. Third, the C-V characteristics are stretched out and show a large threshold shift after stressing, implying created interface states with trapped negative charge. Fourth, the tunneling gate current is essentially unchanged after stressing, again suggesting charge neutrality.

Figure 12 illustrates a speculative picture of how hot-electron stressing may be inducing damage using hot holes as a precursor for the case of HfO_2 nFETs. Figure 12(a) illustrates hot-hole injection from the polysilicon gate into the gate dielectric during hot-electron stressing. After a hot electron traverses the gate insulator stack to the gate electrode, it can generate an electron-hole pair either by impact ionization or by excitation of a surface plasmon [26]. Assisted by a photon, a hole from the gate can be injected back into the high-κ dielectric where it causes damage. Alternately, the incident hot electron can absorb a photon, enabling it to generate a high-energy hole. Figure 12(b-c) shows newly created trap states which are charge neutral near flatband and negatively charged (filled with electrons) near threshold. In Fig. 12(d) it is shown how these trap states can be emptied under high fields in strong inversion.

We now discuss this speculative picture in greater detail. First, we consider the creation of electron-hole pairs by hot electrons entering the anode by impact ionization. Indeed, the energy barrier seen by holes injected from the anode is calculated to be 3.4 eV in bulk HfO_2 and 4.9 eV in bulk Al_2O_3 [5] (although measured as low as 3 eV in thin films of Al_2O_3 [18]) compared to 5 eV in SiO_2 [21]. A second possibility for hole generation is via a process mediated by Si/high-κ interface plasmons for which the energy of excitation decreases with

dielectric constant κ as $(\kappa+1)^{-1/2}$ [26]. Although we are hesitant to draw conclusions based only on comparing results from single wafers of HfO_2 and Al_2O_3, we note that the turn-on behavior of the power-law coefficient A at lower energies in HfO_2 compared to Al_2O_3 (Fig. 4) is consistent with our expectations based on the lower valence band offset and higher dielectric constant of HfO_2. Also, the estimated threshold energy of $E_{tot} \approx 3.8$ eV for hot-electron damage in HfO_2 should be contrasted with the 5 eV threshold for damage in SiO_2 [1]. Finally, we note that the smaller valence band offset and higher dielectric constant on the anode side of the gate insulator stack may also be related to the polarity dependence observed here and in Refs. [7, 10], but the inability to see enhanced charge trapping effects under cold stressing conditions leaves this relationship inconclusive.

Next, we consider the nature of the damage by hot holes. Hot holes in SiO_2 have been widely studied as a possible precursor for damage in SiO_2 [17]. In this picture, a hot hole recombines with an electron, and the resultant energy release breaks bonds in the SiO_2, generating positive charge centers – also called "slow states" or "anomalous positive charge" [22–24] – on which electrons are trapped. Although we might expect from this previous work that hot-hole induced damage occurs in the oxynitride underlayer, damage at the internal (oxynitride-high-κ) interface is also possible as is damage in the high-κ dielectric itself. Indeed, Afanas'ev and Stesmans [18] have recently reported that optical injection of electron-hole pairs in Al_2O_3 and ZrO_2 results in positive charging, suggesting trapping of holes.

In order to further test the hot-hole hypothesis, we can ask whether the amount of positive charge required to cause the increase in the gate current correlates roughly with the negative charge in the created electron traps giving rise to the positive threshold shift ΔV_t. To do this, we convert the hypothesized positive charge to an equivalent gate voltage shift, ΔV_{geq}, by finding the change in gate voltage required under cold stressing conditions (with all other electrodes at ground) to effect the same increase in gate current seen under hot stressing conditions. A comparison of these two voltages, ΔV_{geq} and ΔV_t, can help us verify the correlation between the positive charge and the created electron traps. The case $\Delta V_{geq} \leq \Delta V_t$ would suggest a correlation whereas the case $\Delta V_{geq} \ll \Delta V_t$ would imply too little positive charge to account for the traps required to create the observed threshold shift. Figure 13 shows the results of plotting the equivalent gate voltage shift as a function of the measured threshold voltage for 23 various hot-carrier stress experiments on wafer H1, with

substrate voltages ranging from V_x=-1.5 V to V_x=-6 V. Here the equivalent gate voltage shift ΔV_{geq} has been computed from the ratio of final to initial gate current I_{gf}/I_{gi} using the experimentally obtained relation ΔV_{geq}=(0.13 V) $\ln(I_{gf}/I_{gi})$, valid for currents in the range of interest. The cluster of single points near the origin correspond to low substrate bias ($V_x \leq -2.25$ V, as in the wavelength-dependent experiments) while the lines connect points from experiments at higher substrate bias with large threshold shifts measured at several intervals. We see that the voltage ratio $\Delta V_{geq}/\Delta V_t$ varies from approximately unity near the origin (weak stressing) to roughly 0.3-0.5 under higher stressing conditions, showing that a correlation between the positive charge and the electron traps is indeed reasonable.

We thus summarize the observations which we believe constitute strong "circumstantial evidence" that the damage consists of defects whose origin stems from the presence of holes in the dielectric and whose nature is similar to the nature of the slow states observed in SiO_2 films [22–24]:

(i) the sharp increase of the gate current;

(ii) the generation of interface traps at the Si/oxynitride interface, indicated by the C-V stretchout;

(iii) the possibility of altering quasi-reversibly the occupation of at least a fraction of the generated defects, testified by the hysteresis experiments on Al_2O_3 nFETs (Fig. 10);

(iv) the fact that the amount of the positive charge deduced by the shift ΔV_{geq} is quantitatively of the same order of magnitude as the negative charge deduced from the threshold voltage shift; and

(v) the similarity of the damage observed after hot-hole stressing in pFETs.

As mentioned earlier, our inability to clearly observe charge transfer in HfO_2 nFETs at long time scales may indicate a difference in the nature of the slow states in HfO_2 compared to those in Al_2O_3 and SiO_2.

Two further aspects of the nature of the damage merit discussion. First, previous studies of hot-hole damage in SiO_2 point to the generation of electron neutral traps [27, 28]. Although we are cautious about the physical interpretation of the fitting parameter σ_0 used here as a capture cross section, we note that its 10^{-16} cm^2 range is consistent with previous studies of neutral traps [29] and their generation by hot holes [27], [28]. Second, based on Fig. 12, we can speculate the existence of an amphoteric defect which is filled with an electron near threshold, is empty and thus neutral near flatband, and can be filled with a hole (devoid

of an electron) during stress when high-energy holes are available. Alternately, a more complicated picture is that electron and hole traps are independently generated. Unfortunately, our charge transfer experiments have not yielded enough information to distinguish between these two possibilities.

Finally, we comment on the failure to observe enhanced charge trapping in the presence of light using cold electrons. This may be because in cold-electron injection, the strong polar interaction of low-energy electrons with longitudinal-optical (LO) phonons in the high-κ film can prevent the carriers from acquiring significant kinetic energy, except at very high electric fields. In contrast, hot electrons enter the dielectric in the regime in which scattering with LO-phonons is already reduced (because of its $E^{-1/2}$-dependence on the electron energy E [30]) and thus may undergo quasi-ballistic transport – as seen in SiO_2 [31] – and reach the anode with significant kinetic energy. Therefore, at the anode, the small high-κ/Si barrier height and the quasi-thermal electron energy in the high-κ insulator will result in a small electron kinetic energy in the polysilicon gate, thus effectively suppressing the pair-generation process. This is the regime investigated by Zafar et al [13]: Only a weak C-V stretchout is observed, and the gate current decreases gently with time, so that filling of pre-existing traps dominates over filling of any traps created. Thus, although contrary to our initial expectations, it is perhaps not surprising that the enhanced charge trapping with light is not observed even at high gate insulator fields.

V. CONCLUSION

In conclusion, we believe that a strong case has been made for hot-carrier degradation in which hot holes act as a precursor for creating damage in high-κ dielectric stacks. This damage appears to be qualitatively different from, and potentially more severe than, the charge-trapping effects frequently seen in experiments using cold-carrier injection, which are dominated by filling of pre-existing traps. We expect these effects to be of more pressing importance in pFETs, where hot holes can be generated under normal biasing conditions. In nFETs, careful consideration to the the supply of hot holes should be given. Of particular interest for future work will be a comparison of the results obtained here to those in metal-gated samples where anode holes should originate only from surface plasmons and not from impact ionization.

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[32] This condition sometimes requires the gate voltage to be chosen slightly below threshold during hot-carrier stressing.

[33] The intensity of the halogen lamp source varies smoothly in the visible range used for the filter cut-on wavelengths.

[34] The transistor source and drain are grounded during the measurement, providing a source of minority carriers in inversion.

FIG. 1: Summary of previous results on HfO_2 (a) nFETs and (b) pFETs. The inset of (a) shows a band diagram in which hot electrons are injected from the substrate.

FIG. 2: Charge trapping in HfO_2 nFETs at different maximum photon energies for substrate voltages of (a) -2.25 V, (b) -2 V, and (c) -1.75 V . The inset of (b) shows the mean gate current during each stressing pulse.

FIG. 3: Charge trapping in Al_2O_3 nFETs (a) at different maximum photon energies and the same substrate bias and (b) at different substrate biases and the same maximum photon energy.

FIG. 4: Scatter plots of power law coefficient A and exponent β (inset) as a function of total energy extracted for HfO_2 and Al_2O_3 nFETs.

FIG. 5: Time dependence of gate current under cold and hot stressing conditions. Inset: Tunneling gate current as a function of gate voltage before and after the hot-carrier stress.

FIG. 6: Temperature dependence of charge trapping in HfO_2 nFETs under hot and cold (inset) stressing conditions, and substrate bias dependence under hot stressing conditions.

FIG. 7: Comparison of electron trapping in unstressed and hot-hole stressed HfO_2 pFETs. Inset: Charge trapping during hot-hole stressing followed by restoration of flatband by illumination.

FIG. 8: Flatband and threshold voltage shifts in HfO_2 Al_2O_3 nFETs. Insets show typical C-V characteristics for each dielectric.

FIG. 9: Density of interface traps in unstressed HfO_2 nFET. Inset: Change in interface trap density resulting from hot-carrier stressing.

FIG. 10: Results of charge transfer experiment on Al_2O_3 nFET illustrating filling and emptying of interface states. following hot-electron stressing.

FIG. 11: (a) Bias dependence under cold stressing conditions near $V_g = V_{fb} + 1.1$ V. (b) Polarity dependence under cold stressing conditions. Inset: Substrate current (positive out of contact).

FIG. 12: Band diagram showing schematically (a) positive charge trapping during hot-electron stressing; (b) created interface states which are unoccupied (neutral) at flatband; (c) interface states being filled by electrons near threshold; and (d) emptying of interface states at high insulator field.

FIG. 13: Equivalent gate voltage shift due to positive charge deduced from increase in hot-carrier gate current as a function of measured threshold voltage shift for 23 experiments on HfO_2 nFETs.

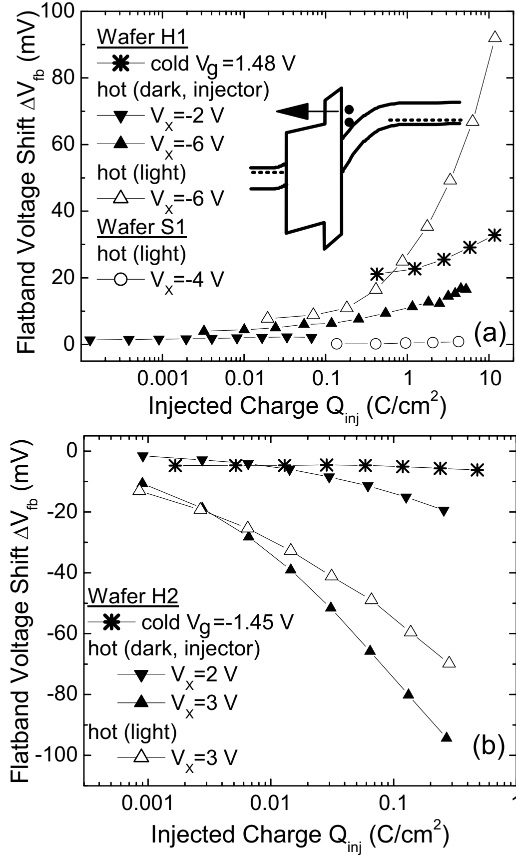
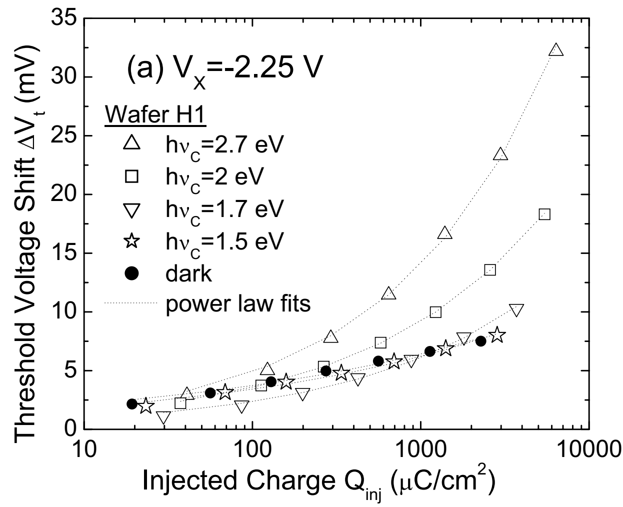
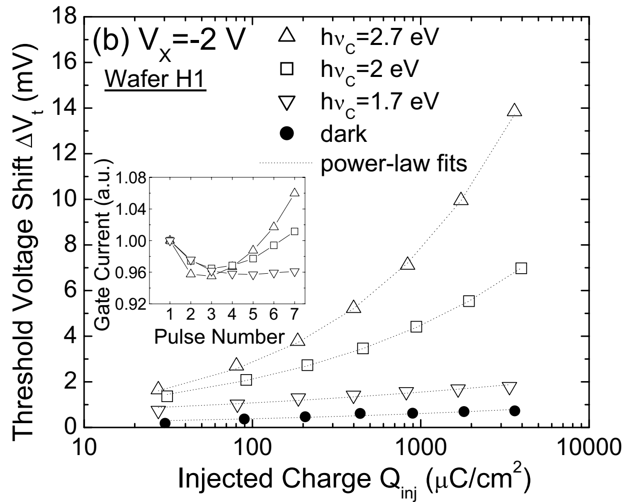


FIG. 1:

TABLE I: Characteristics of wafers used in this study. All high-κ dielectrics are deposited on top of a thin oxynitride layer.

Wafer	gate dielectric	type	V_{fb} (V)	V_t (V)
H1	3 nm HfO_2	nFET	-0.75	0.50
H2,H2'	3 nm HfO_2	pFET	0.40	-0.90
A1	3 nm Al_2O_3	nFET	-0.55	0.85
S1	2.2 nm SiO_2	nFET	-1	0.24





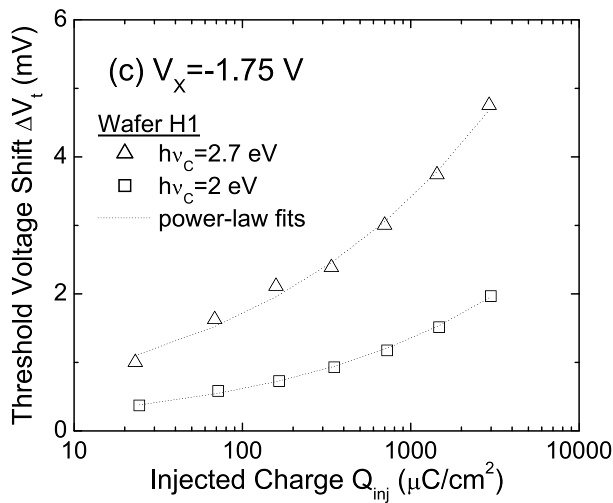


FIG. 2:

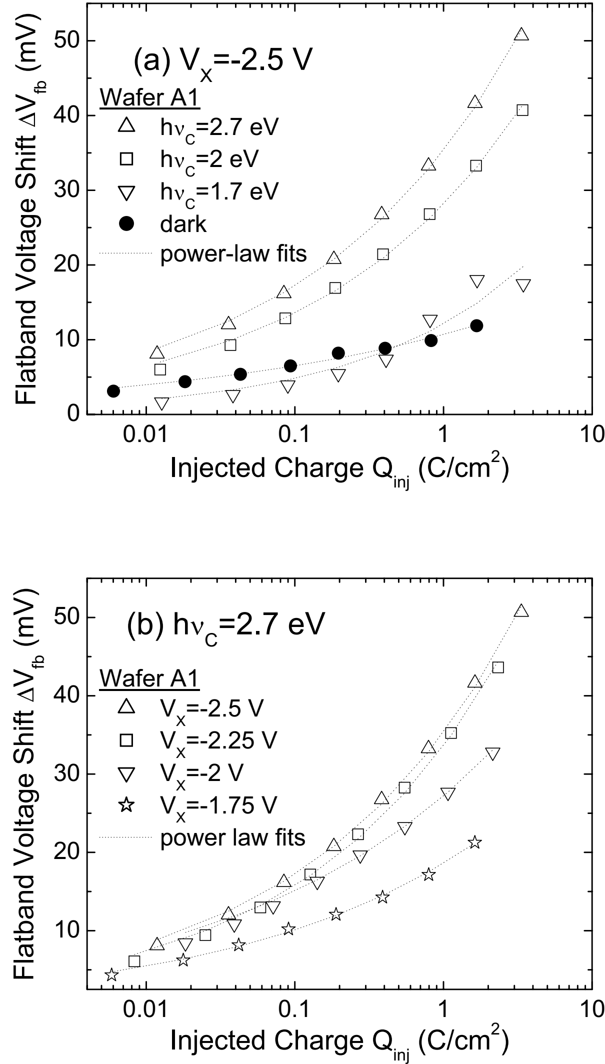


FIG. 3:

TABLE II: Parameters of stretched exponential fit at various temperatures for wafer H1 with $V_x = -3$ V under hot stressing conditions. Uncertainties represent quality of fit to data.

Temperature	V_x (V)	$\Delta V_{tm}(V)$	σ_0 (cm^2)	β
25 C	-3	$0.314 \pm .002$	$(1.04 \pm 0.05) \times 10^{-16}$	$0.43 \pm .01$
75 C	-3	$0.182 \pm .002$	$(2.01 \pm 0.13) \times 10^{-16}$	$0.52 \pm .02$
120 C	-3	$0.099 \pm .001$	$(6.12 \pm 0.40) \times 10^{-16}$	$0.53 \pm .02$
25 C	-4	$0.477 \pm .004$	$(8.05 \pm 0.62) \times 10^{-17}$	$0.35 \pm .01$
25 C	-5	$0.609 \pm .008$	$(2.91 \pm 0.38) \times 10^{-17}$	$0.26 \pm .01$

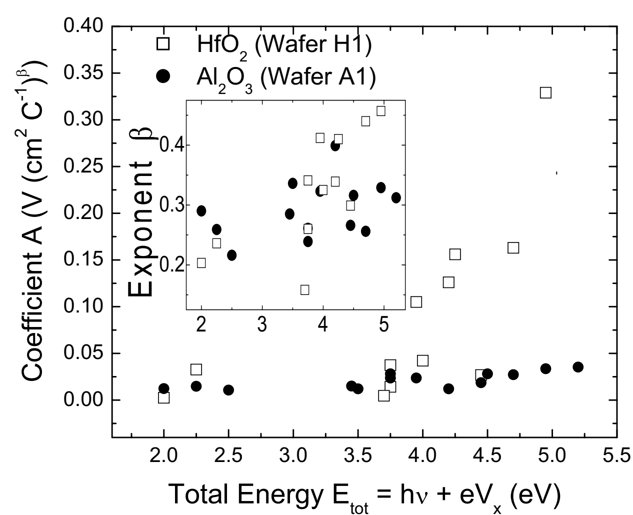
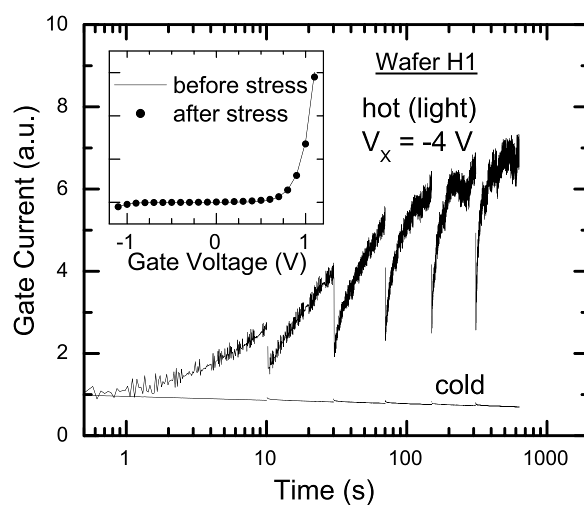


FIG. 4:



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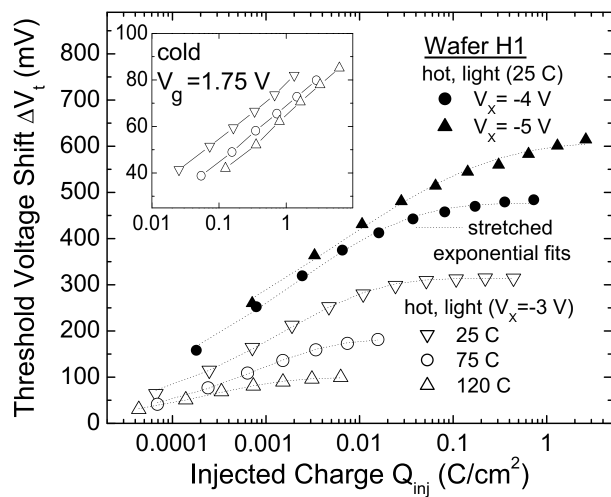

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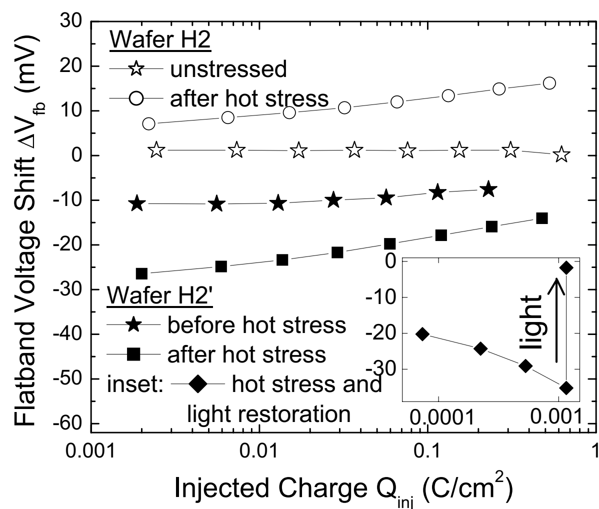


FIG. 7:

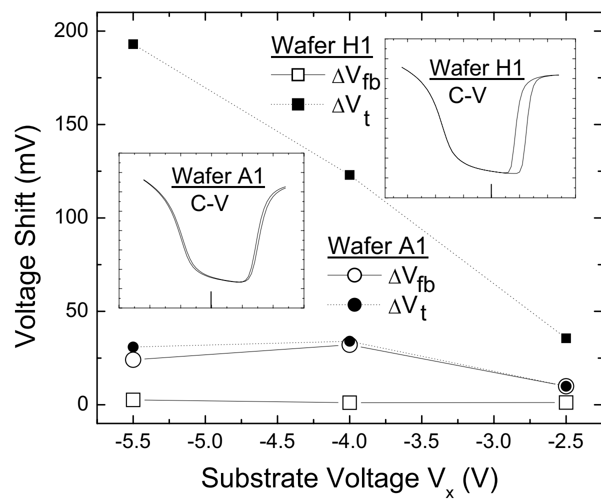


FIG. 8:

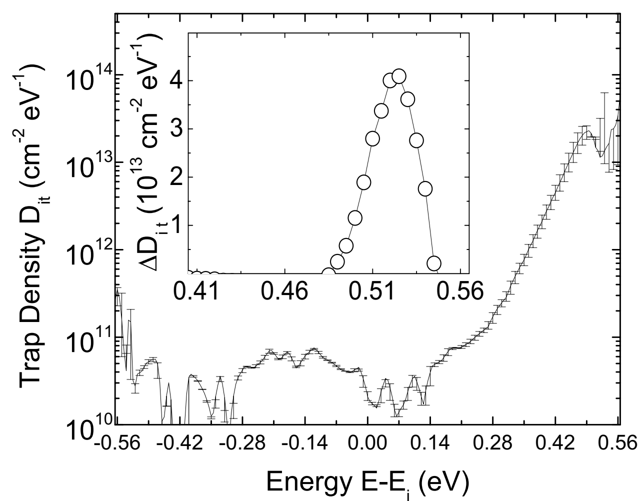


FIG. 9:

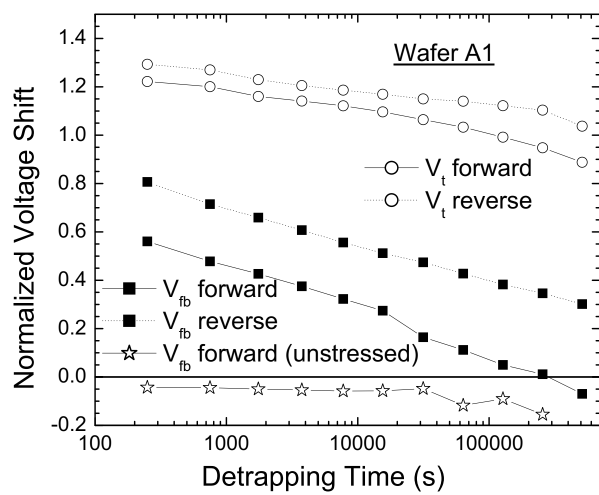
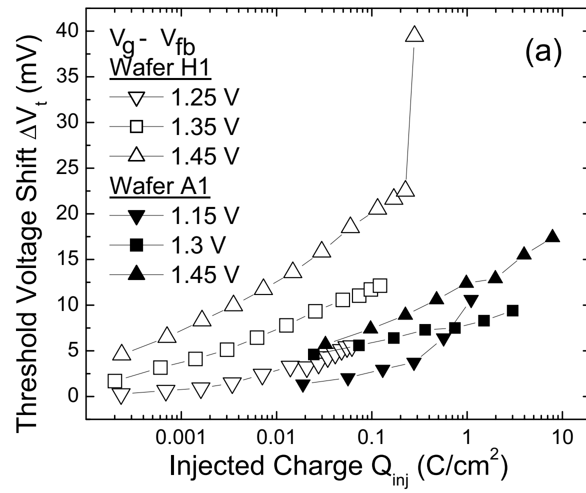
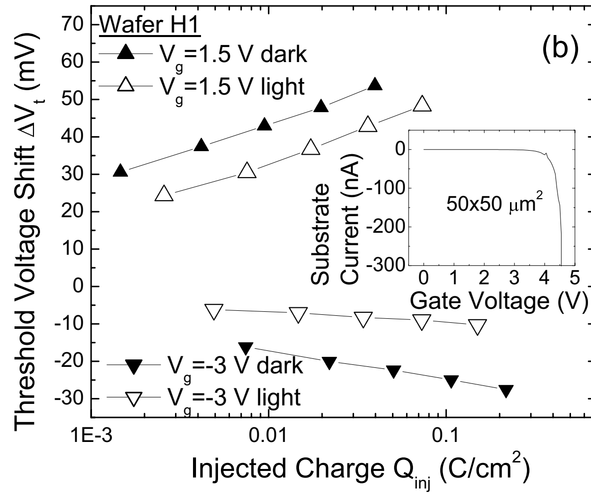


FIG. 10:





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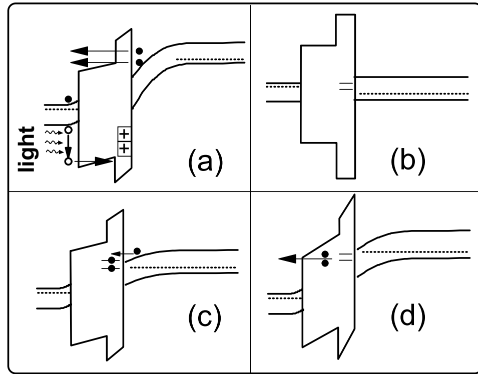

FIG. 12:

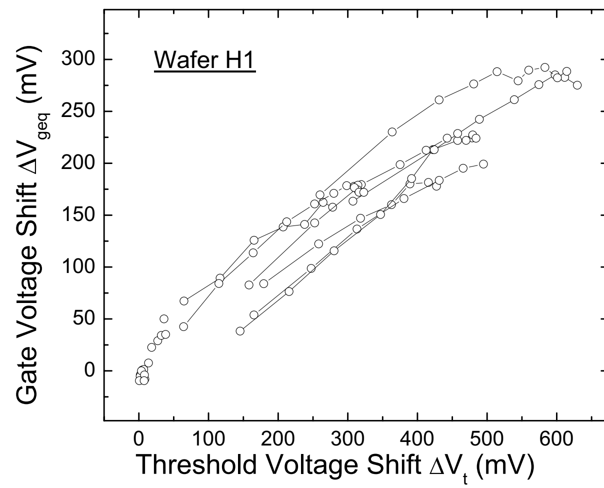

FIG. 13: