RC22797 (W0305-061) May 12, 2003
Electrical Engineering

IBM Research Report

Single SiGe Transistor Power Output Limits at Frequencies Greater than 31 Ghz Based upon Published Journal Data and Theoretical Approximations.

Ullrich Pfeiffer, Brian P. Gaucher, Modest M. Oprysko, Mehmet Soyuer
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

Research Division
Almaden - Austin - Beijing - Delhi - Haifa - India - T. J. Watson - Tokyo - Zurich

LIMITED DISTRIBUTION NOTICE: This report has been submitted for publication outside of IBM and will probably be copyrighted if accepted for publication. It has been issued as a Research Report for early dissemination of its contents. In view of the transfer of copyright to the outside publisher, its distribution outside of IBM prior to publication should be limited to peer communications and specific requests. After outside publication, requests should be filled only by reprints or legally obtained copies of the article (e.g. , payment of royalties). Copies may be requested from IBM T. J. Watson Research Center ,
P. O. Box 218, Yorktown Heights, NY 10598 USA (email: reports@us.ibm.com). Some reports are available on the internet at http://domino.watson.ibm.com/library/CyberDig.nsf/home .

Single SiGe transistor power output limits at frequencies greater than 31 GHz based upon published journal data and theoretical approximations.

U. R. Pfeiffer, B. P. Gaucher, M. M. Oprysko, M. Soyuer

Introduction

In this paper, we will show that today's SiGe transistor technologies can reasonable reach power levels of a few hundred milli-Watts, in a millimeter wave (MMW) regime above 31 GHz. This is done in two parts. First, published SiGe transistor output powers at MMW frequencies are presented. Second, a Figures of Merit (FoM) is discussed to draw conclusions on performance values of power amplifiers (PAs). Based on this, we show that reasonable output power levels of **100's of milli-Watts are possible** today with further improvements expected in the future.

Published results

A paper published in 2000, discusses SiGe RF devices that output **20mW at 47 GHz** [1]. Papers that were published in 2002 and 2003 in SiGe 7HP 0.18um technology, discuss wire line limiting and driver amplifiers operating at >40Gbps data rates, while delivering >30mW into 50 ohms, which clearly have third harmonic spectra, required of square waves, in the millimeter wave band [2, 3]. See Table 1 for a summary.

Table 1 Published results

Paper Title	Date published	SiGe Technology	Device Type	Frequency GHz	Power mW	Gain dB	Load Ohms
Wireless Technologies and Information Networks (1)	Jul-00	SiGe	6 finger emitter	47 GHz	20	-	50
40-Gb/s Circuits Built from 120GHz ft SiGe Technology (2)	Sep-02	SiGe 7HP, 120GHz ft	HBT, mod driver amp	48Gbps	>30	-	50
SiGe BiCMOS Integrated Circuits for High-speed serial communication links (3)	May-03	SiGe 7HP, 120GHz ft	HBT, limiting amp	40Gbps	>2.5	7	50

Technology Trend and Figure of Merit

The most cited and recognized prediction of future technology trends in the semiconductor industry today is the 2001 International Technology Roadmap for Semiconductors (ITRS). We start our discussion on transistor output power limits with a Figure of Merit for power amplifiers (FoM_{PA}) derived from the System Drivers Section of the ITRS document [4], [5]. Based on today's device parameters we can then extrapolate this FoM_{PA} to future performance values.

In basic power amplifier circuits the main parameters are output power (P_{out}), power gain (G), carrier frequency (f), linearity (in terms of IIP3), and power-added efficiency (PAE). Unfortunately, linearity strongly depends on the amplifier's operating class. To be independent of the design approach, the FoM_{PA} is given for linear operated Class-A amplifiers only, where the linearity parameter can be omitted from the FoM (see eq1).

$$FoM_{PA} \propto P_{out} \times G \times PAE \times f^2 \qquad \text{-eq1}$$

To compensate for the high-frequency roll-off of the PA's RF gain, a factor of f^2 is included. The published literature indicates that e.g. Class-A PAE can be seen as essentially constant across technologies (e.g. 10%). To build a useful device with some reasonable gain, one typically operates the device at f= f_{max}/(3 to 10), making the gain G reasonably constant across technologies. Our parameter of interest in this equation is the transistor output power P_{out}. This power is independent from the operating frequency and its value for a single transistor is theoretically unlimited. For example, the output power of a multi-finger device can be doubled by adding twice as many fingers to the device. This can be understood as a power combining technique, where the power at a given frequency f, only scales with the total length of the transistor. This suggests that there is no limit to the output power at frequencies greater than 31 GHz, as long as the

transistor can operate in that frequency range. But there are practical matching limitations one faces, which limit the maximum available power for a given technology.

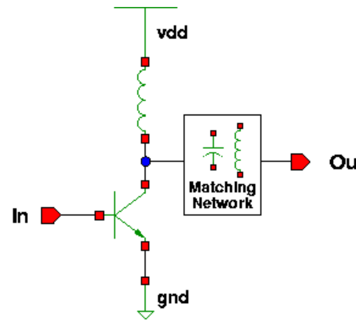

Figure 1:Schematic of a Class-A SiGe power amplifier.

In the following, we restrict our considerations to the Class-A operation shown in Fig. 1. From that figure, the power delivered to a load can be calculated from the maximum available voltage swing across the transistors load impedance. P_{out} can be estimated as:

$$P_{out} \propto BV_{ceo}^{2} / Z_{Load} , \qquad \text{-eq2}$$

where Z_{LOAD} is the input impedance of the matching network, and BV_{ceo} is the breakdown voltage limit of the device. In access of higher output powers, and as we add more and more fingers to the device, the input and output impedance of the transistor is reduced substantially. The power combining technique is reaching its fundamental design limit when the input and output impedance of the transistor is of the same order as the loss of the input and output matching network. At this point, the total transistor output power is reduced because the efficiency decreases as the number of fingers is increased. Hence, at higher frequencies, the Q of the matching elements becomes more of a design challenge. From the ITRS roadmap the Q-factor of passive inductors in a silicon process is expected to increase from 12 to 20 in the near term [6]. For example, at a carrier frequency of 31 GHz an inductor of 0.15 nH and a Q of 20 has a resistive loss of wL/Q=1.5 Ohm. This impedance is the fundamental limit which we will use in the following to calculate the maximum transistor output power limit for a given technology node based on equation eq2. It is important to note at this point, that f_{max} is not directly part of the equation, but is inferred, i.e. we've assumed that one has designed their transistor at f_{max}/(3 to 10). A higher f_{max} will simply move the operation frequency of the transistor higher into our frequency band of interest (> 31 GHz). But of course, the price one has to pay is the slightly lower device breakdown voltage BV_{ceo}.

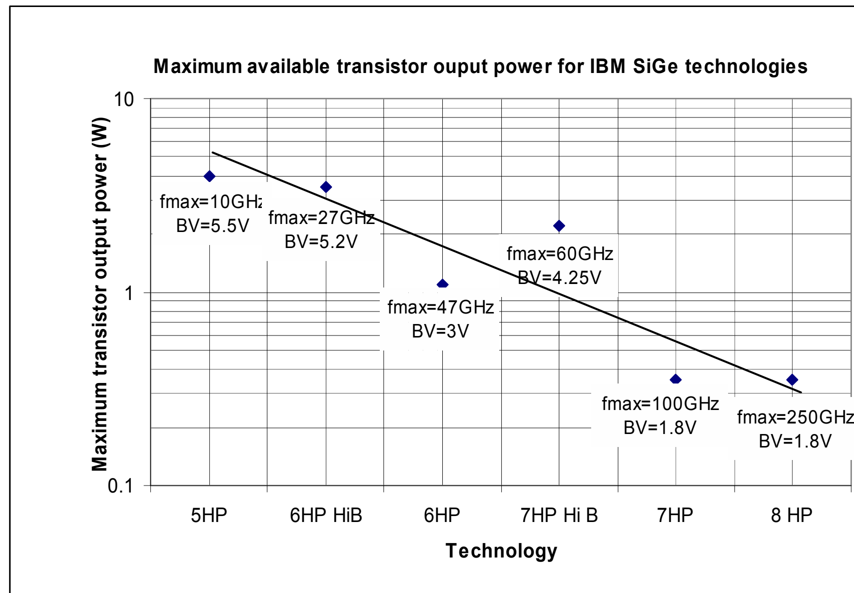

Figure 2: Maximum available transistor output power for IBM SiGe technologies

(HiB stands for High Breakdown voltage transistor)

Figure 2 shows the extrapolation of the transistor power for IBM SiGe based PA's based on the discussion above and assumes a load impedance of 1.5 ohms corresponding to 0.15 nH and a Q of 20. Figure 2 also assumes that the breakdown voltage can be safely exceeded by about 30% [7]. The knee voltage V_{knee} is at the transistor saturation region is assumed to be about 0.3 V. This is used across all data points. Thus a simplified view of how each point is calculated is given in eq-4.

$$((BV_{CEO} + 30\%) - V_{Knee})/(2\sqrt{2}))^2 / R_{Load} \qquad \text{-eq4}$$
$$((5.5 + 30\% - 0.3)/(2\sqrt{2}))^2 / 1.5 = 3.9W$$

Each technology family has many possible transistors to choose from, but we've limited this to a maximum of two per technology; the high performance and the high breakdown voltage transistors. As can be seen, there is a roughly linear decrease in output power at the maximum useable frequency with each increase in technology. If one were to force a linear fit as looks to be the case, then the possible extrapolation that could be made is that the maximum available output power P_{out} drops at approximately a factor of 2.5 per technology generation. At the same time the operation frequency moves up by a factor of 2-3. Table 2 below uses the data of Figure 2 and assumes a frequency of operation of $f_{max}/3$ to provide an upper bound on possible performance.

Table 2 Output power and frequency operation for a given technology

Technology	**5HP**	**6HP HiB**	**6 HP**	**7HP HiB**	**7HP**	**8HP**
F=fmax/3 (GHz)	3.3	9.0	15.7	20.0	33.3	83.3
Power out (W)	4	3.5	1.1	2.1	0.33	0.33

Conclusion:

Based upon published and calculated results, RF transistors with **output powers greater 20mW have been demonstrated** several years ago and as **shown here, output powers greater than 100mW are possible at MMW frequencies** today and this is expected to be improved in the future.

References:

1. Ephremides, T. Itoh, R. Pickholtz, M Iskander, L. Katehi, R. Rao, W. Stark, J. Winters, "WTEC panel report on Wireless Technologies and Information Networks," International Technology Research Institute, July 2000

2. G. Freeman, et-al, "40-Gb/s Circuits Built from 120GHz ft SiGe Technology," IEEE Journal of Solid State Circuits Vo. 37, No.9 Sept 2002 pg 1106-1114

3. D. Friedman et-al, "SiGe BiCMOS Integrated Circuits for High-speed serial communication links," IBM Journal of Research and Development vol. 47, No.2/3 March/May 2003, to be published.

4. R. Brederlow et-al, "A Mixed Signal Design Roadmap," IEEE Design & Test of Computers, 2001

5. International Technology Roadmap for Semiconductors (ITRS), 2001 Edition, Section System Drivers

6. International Technology Roadmap for Semiconductors (ITRS), 2001 Edition, Section Process Integration, Devices, and Structures and Emerging Research Devices

7. Arira Inoue, Shigenori Nakatsuka, Ryo Hattori and Yoshio Matsuda, "The Maximum Operating Region in SiGe HBT's for RF Power Amplifiers", IEEE MTT-S, Seattle, Washington, June 2-7 2002, Volume 2, pg 1023