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Leakage and Leakage Sensitivity Computation for Combinational Circuits

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ABSTRACT

Leakage power is emerging as a new critical challenge in the design of high performance integrated circuits. It has been shown in many reports that leakage is increasing dramatically with each technology generation and is expected to dominate total system power. Motivated by the need for accurate estimation of the leakage power, this paper describes a static (i.e input independent) technique for efficient and accurate leakage estimation on combinational circuits. A probabilistic technique is employed to compute the average leakage of combinational circuits under all possible input patterns. We also show that the input dependency of the leakage for large combinational circuits is fairly small due to an averaging effect. The proposed technique gives very accurate results with an average error of only 2% for the ISCAS circuit benchmarks. We also extend the proposed technique to predict the leakage power components separately, by predicting the subthreshold and gate leakage components of the circuit. Furthermore, the leakage sensitivities of the circuit with respect to environmental and process variables can be also predicted by the proposed method. We demonstrate the application of predicted sensitivities in building practical compact models of leakage power. The leakage sensitivities can be employed in a wide range of applications including in optimizing the circuit performance, manufacturing yield and product quality.

1. INTRODUCTION

Technology scaling is causing a drastic increase in both subthreshold and gate leakage currents and therefore in the leakage current [1][2]. Leakage power accounts for about 10-20% of the total chip power in current technologies, and is already important for the standby operation and battery life for low-power devices. With new technologies, threshold voltage and gate oxide scaling are causing leakage to dominate the total chip power. Leakage is emerging as one of the key variables in the design process along with timing, noise and dynamic power[2]. Accurate and efficient estimation of leakage is required for both power estimation and circuit optimization.

Early work on leakage estimation mainly focused on subthreshold leakage and the dependence of leakage on the state (or the input pattern) of the circuit. Typically, CMOS circuits were macromodeled by transistor stacks for which leakage is computed using analytical expressions. In [4][9], simple analytical expressions are derived for the leakage current of a transistor stack. A statistical approach to discover low leakage patterns was presented in [10]. The authors of [5] proposed both branch-and-bound and heuristic algorithms to find leakage power bounds. Most recently, [6] proposed an automatic test pattern generation based approach to find leakage power bounds and associated input patterns. For full-chip total leakage power estimation, regression models based on gate and transistor counts are presented in [11]. However, the accuracy of simple regression models are generally difficult to control. Furthermore, this technique ignores the dependence of leakage on circuit topology. A more accurate approach [8] estimates total leakage power after an effective stacking approximation. The effective stacking estimates for each cell are weighted by their usage counts. However, even in this model circuit functionality is not considered. Furthermore, macromodeling each cell by a transistor stack can produce undesirable errors. More recently, [7] described an estimation method based on a concept of dominant leakage states. By ignoring low leakage states, the authors proposed a graph-based approach to partition the design into individual components. The average leakage of each partition is then computed via DC analysis with Newton-Raphson iterations.

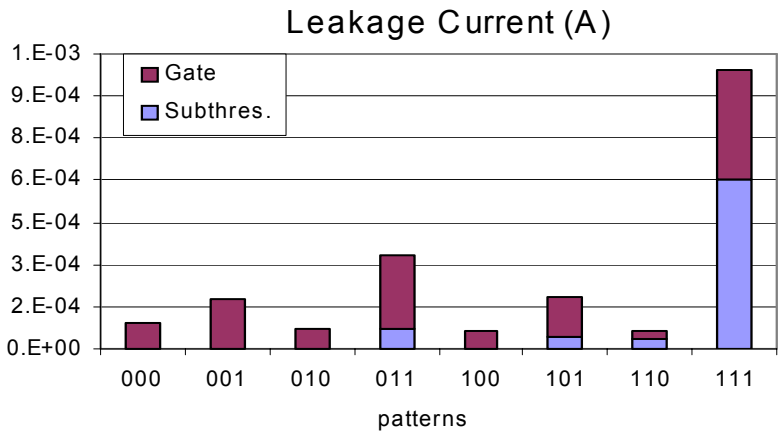


Figure 1. Total leakage current for a 3-input nand gate for 8 possible states.

Leakage has been predicted either by detailed input-dependent analysis or by higher-level models based on total transistor width or gate count. There is an urgent need for more efficient but accurate leakage power estimation for proper design and optimization. Hence, we propose an efficient static (i.e. input-independent) analysis technique for leakage estimation. We do want to mention that dynamic (input-dependent) techniques may be needed in evaluating special circuit topologies for leakage mitigation, however for most common combinational circuits, static methods are highly applicable. Note that, the proposed static technique accurately accounts for circuit topology.

Leakage current depends on many key circuit variables such as input vectors, device characteristics (threshold voltage, gate oxide thickness, channel length) and operating conditions (VDD and temperature). But let us first investigate the input dependence of leakage for a basic logic gate designed under a leading process technology. The total leakage currents of a 3-input nand gate for all possible inputs are shown in Figure 1. It is clear from the figure that there is a significant input dependency of leakage. The pattern (111) creates 10 times more leakage than the pattern (000). However, as the size of the combinational circuit increases, this input-dependency becomes weaker. This is mainly due to an averaging effect in the circuit that balances out high and low leakage

Circuit	*# cells*	*# inputs*	I_{max}*(mA)*	I_{min} *(mA)*	*cv.*
c432	*187*	*36*	*0.073899*	*0.0597*	*0.0237*
c499	*222*	*41*	*0.21463*	*0.153863*	*0.0337*
c880	*383*	*60*	*0.132035*	*0.095789*	*0.0335*
c1355	*566*	*41*	*0.173451*	*0.127854*	*0.0301*
c1908	*996*	*33*	*0.312824*	*0.210898*	*0.0610*
c2670	*1255*	*233*	*0.427436*	*0.325011*	*0.0363*
c5311	*2485*	*178*	*0.842406*	*0.670118*	*0.0279*
c7752	*3692*	*270*	*0.713998*	*0.665011*	*0.0483*

Table 1: The dependency of leakage currents on input vectors for various ISCAS benchmark circuits. The results show about 15% variability in total leakage power. (cv denotes the coefficient of variation which is the ratio of std. deviation over mean)

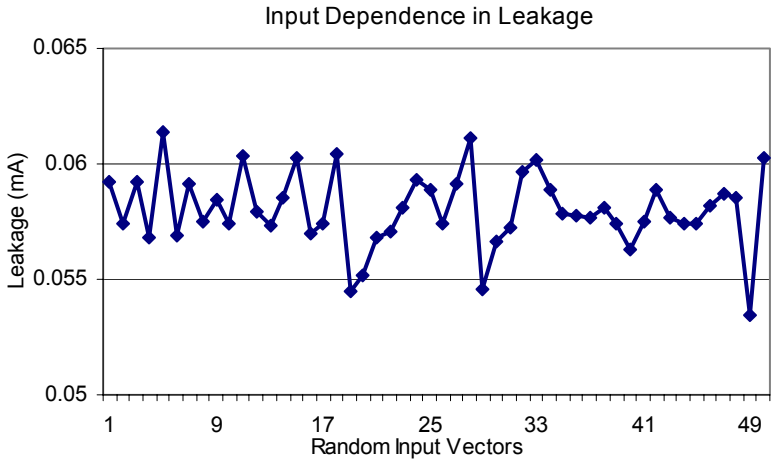


Figure 2. Dependency of total leakage on input vectors for ISCAS benchmark circuit c432.

states. To illustrate this, the total leakage for the ISCAS circuit C432 is shown in Figure 2 for many random input vectors. The circuit is synthesized with a typical gate library satisfying pre-specified delay targets. Input dependence of total leakage for other circuits is summarized in Table 1. For each benchmark circuit, the extreme statistics and coefficient of variation (standard deviation/mean) of leakage currents with 10000 random input patterns are reported. From the table, we see that total leakage varies by about 15% with the input applied to the circuit.For larger size circuits, a similar trend is observed.

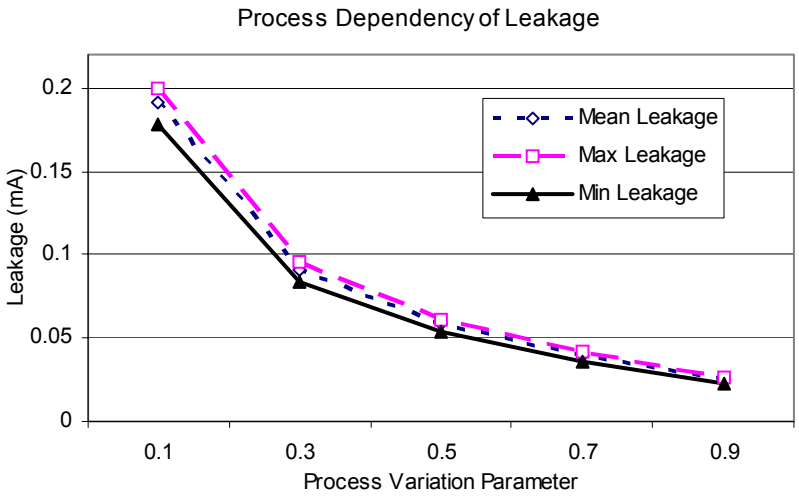


Figure 3. Impact of process variations on leakage for c432. To display input-patter dependency, min and max leakage observed from 10000 input patterns are also plotted.

Leakage dependency on input vectors can still be significant, but we believe that it is much less than the effect of environmental variables (Vdd, temperature) and process variations (Leff, Vth, tox). The impact of process variations on leakage is summarized in Figure 3. This figure shows how leakage current varies with different process conditions. A normalized process parameter is used to model the process conditions between the "fast" and "slow" corners. 0.5 represents the nominal conditions. At each process point, the variation of leakage due to input vectors is also shown by the maximum, average and minimum leakage obtained for a large sample of inputs. As seen from the figure, leakage varies much more with the process parameter than with input variations. Similarly, Figure 4 shows the dependence of leakage on temperature for circuit C432. The maximum, average and minimum leakage for different input vectors at each temperature are also plotted. Just like the process variation parameter, the leakage varies much more due to temperature compared to input vectors. A similar trend is also observed for leakage dependency on VDD.

In light of these observations, we can say that while the input dependence remains important and needs to be captured in some cases (e.g. for the standby mode), but the leakage dependence on process parameters, tempera-

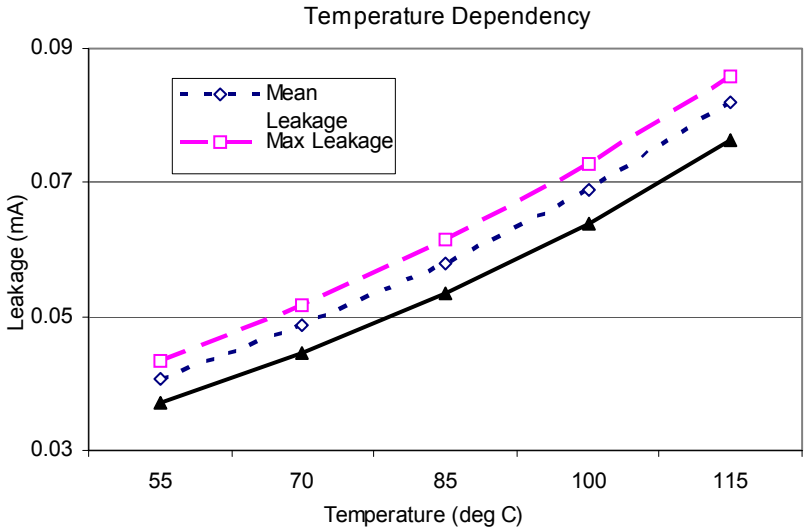


Figure 4. Impact of temperature variations on leakage for c432.

ture and VDD is far more important in an effective leakage estimation methodology. Therefore, it is desirable to develop a static (input-independent) method for predicting the average leakage power under possible input conditions. By dropping the variability on input, the effects of temperature, power supply and process variations can be more readily and efficiently accounted for. This static approach will accurately account for average leakage power for all possible input patterns, realizing an overall assessment of the leakage for a considerably long operation time.

In this paper, we also extend our estimation method for leakage sensitivity to environmental and process parameters. Leakage sensitivities can be very instrumental in design optimization and planning. With little additional effort, the sensitivities of average leakage with respect to a designated parameter can be computed along with the static estimate. Furthermore, we briefly show ways to utilize this sensitivity information to model the parameter dependence of leakage. The efficacy of the proposed methods will be important for future technologies which display significant within-die power supply, temperature and device model parameter fluctuations.

The techniques presented in this paper are generally applicable for combinational circuits. We assume that

other elements of an integrated circuit, including memory and clocking system elements (caches, registers and latches) can be modeled directly because they are more regularly structured, heavily reused and easier to pre-characterize. Hence, we focus on leakage power of general combinational circuits, which have more irregularity and variability.

The remaining part of the paper is organized as follows. Section 2 describes the proposed static leakage estimation technique. Experimental results are presented in Section 3. Section 4 describes the method for estimating the leakage sensitivity and we present some results in Section 5. We conclude our findings in Section 6.

2. STATIC LEAKAGE ESTIMATION

This section presents a static estimation technique for average total leakage of a combinational circuit. The proposed technique exploits circuit topology and properly accounts for the embedded circuit connectivity.

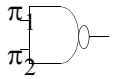
2.1 Background

Combinational logic circuits are generally partitioned into smaller cells, in the form of gates, channel-connected regions or other primitive structures. The node variables at the cell boundaries are assumed to hold full logic values (VDD or 0). Total leakage power dissipation is basically the sum of the leakage dissipated in each cell. Let us assume that the leakage power for each cell is pre-characterized for all circuit input states. This can be done via accurate circuit simulation during library generation. Let us denote by $L_i(x_i)$ the leakage power for cell i for input vector x_i; the total leakage power for a given input vector will be:

$$L_{tot} = \sum_i L_i(x_i) \tag{1}$$

Note that the current state of the circuit, i.e. the inputs for each cell, will depend on the connectivity and functionality implemented in the circuit.

We now introduce the concept of occurrence probabilities to compute the average leakage power of a circuit. Previous probabilistic approaches were reported in [3][13][14][15] and were applied for switching power estima-



$$\pi_1(1-\pi_2) + (1-\pi_1)\pi_2 + (1-\pi_1)(1-\pi_2)$$

$$= 1 - \pi_1\pi_2$$

State	*Gate Leakage*	*Subthres. Leakage*	*Total Leakage*	*State Occur. Prob.*
00	G_{00}	S_{00}	$L_{00}=G_{00}+S_{00}$	$(1-\pi_1)(1-\pi_2)$
01	G_{01}	S_{01}	$L_{01}=G_{01}+S_{01}$	$(1-\pi_1)\pi_2$
10	G_{10}	S_{10}	$L_{10}=G_{10}+S_{10}$	$\pi_1(1-\pi_2)$
11	G_{11}	S_{11}	$L_{11}=G_{11}+S_{11}$	$\pi_1\pi_2$

Figure 5. Calculating output node occurrence probability with independence assumption and the table of pre-characterized leakage components for a 2-input nand gate.

tion but these approaches do not model the temporal (or delay) dependency of switching power. Leakage, however is delay-independent and hence *more suitable* for a probabilistic approach.

Node Occurrence Probability: Let us assume that node *n* is either a primary input or an output of a particular cell, and holds a full logic value. We define the *node occurrence probability* of *n* as the likelihood of observing the node *n* at logic value 1: $\pi_n = Pr(n = 1)$. Hence, the probability of observing *n* at 0 would be $1 - \pi_n$.

State Occurrence Probability: We define the state occurrence probability $\Pi_i(x)$, as the probability of observing the cell *i* at the state uniquely imposed by input *x*. State occurrence probability can be referred to as the joint probability of the input nodes of cell *i*. If the cell inputs are independent, computation of $\Pi_i(x)$ is simply the multiplication of the associated node occurrence probabilities. An example is given in Figure 5 for a 2-input nand gate.

Average Leakage Power: The true probabilistic mean of the total leakage power $\mu_{L_{tot}}$ is the weighted sum of the leakage for all cells in each state. The weights are simply the state occurrence probabilities:

$$\mu_{L_{tot}} = \sum_i \mu_{L_i(x_i)} = \sum_i \sum_{x_i} \Pi_i(x_i) L_i(x_i) \quad (2)$$

Note that $L_i(x_i)$'s are available for each cell from library pre-characterization. Hence, the exact computation of (2) requires the true state occurrence probabilities, $\Pi_i(x_i)$, for each cell and state. However, the exact computation for $\Pi_i(x_i)$ for combinational circuits is shown to be a NP-hard problem [17].

2.2 Static Probabilistic (SP) Method

We propose a practical approach to predict the state occurrence probabilities using circuit and input information. Like [3], we will ignore spatial dependencies within the circuit for the sake of simplicity and efficiency. The results will later demonstrate that spatial dependencies do not contribute greatly to average leakage estimation, since the estimates are already very accurate. Furthermore, this approach can exploit input probabilities if they are specified.

Consider the cell *C* with an input vector $x = x_1 x_2 \ldots x_n$ and the output node *o*. Under the spatial independence assumption, the node occurrence probability for the output node *o* will be defined as:

$$\pi_o = Pr(x_1, x_2 \ldots | st \;\; O(x) = 1) = \sum_{o_i \in m(o)} Pr(x = o_i) \quad (3)$$

where *O(x)* denotes the logic function and *m(o)* is the set of minterms for *o* in terms of inputs x_i. With the independence assumption, the state occurrence probability for *C* becomes the multiplication of node occurrence probabilities of all its inputs:

$$\Pi_i(x) = \Pi_i(x_1 x_2 \ldots x_n) = \pi_{x_1} \pi_{x_2} \ldots \pi_{x_n} \quad (4)$$

Moreover, once the state occurrence probabilities are computed, they can be separately used for calculations involving the leakage components (i.e. gate and subthreshold). These values must be computed during pre-characterization step as shown in Figure 5.

Based on the estimates of $\hat{\Pi}_i(x_i)$ under the spatial independence assumption, the Static Probabilistic (SP) method estimates the average leakage power as:

$$\hat{\mu}_{SP,\,L_{tot}} = \sum_{i}\sum_{x_i} \Pi_i(x_i) L_i(x_i)\,. \tag{5}$$

The spatial independence assumption guarantees that node and state occurrence probabilities can be computed simultaneously via a level-order traversal of the circuit in linear time. Hence, its runtime complexity grows with the depth of the circuit and the number of cell inputs. In comparison to switching probability, the described approach can easily solve circuits with feedback. But the effects of reconvergent fanout or existing primary input correlation will be ignored by the spatial independence assumption.

The SP method can be also used to estimate the variance of the leakage power of a combinational circuit. With the spatial independence assumption, the variance of the total leakage, $\sigma^2_{L_{tot}}$, would be the sum of each cell's leakage variance which is expressed in terms of state occurrence probabilities of that particular cell. Following that, the variance estimate of the total leakage is:

$$\hat{\sigma}^2_{SP,\,L_{tot}} = \sum_{i}\sum_{x_i} \left\{ \hat{\Pi}_i(x_i) L_i^2(x_i) - \left(\sum_{x_i} \hat{\Pi}_i(x_i) L_i(x_i) \right)^2 \right\}. \tag{6}$$

The variance estimate predicts the amount of variability of leakage due to input variations, and can be used as an indicator of input dependencies. In an integrated analysis framework, this may trigger a dynamic estimation of a particular circuit that display significantly large input dependencies.

The SP method provides an added accuracy in leakage power estimation over simple device-count based methods, since it exploits more information on the circuit including topology and connectivity. If better accuracy is desired, sophisticated methods [15][16][17] can be implemented to account for spatial correlations. But this may significantly increase the overall runtime complexity and is not observed to improve much accuracy.

3. LEAKAGE ESTIMATION RESULTS

This section presents some experimental results with ISCAS circuits. The combinational ISCAS circuits were synthesized using a library of basic gates with delay constraints. A state-of-art process technology is used. The total leakage of each circuit for a given input vector is estimated via an in-house circuit simulator under nominal

Circuit	*Ave. Leakage (W)*	*SP Method (W)*	*Rel. Error (%)*
c432	*0.06599*	*0.06800*	*3.056*
c499	*0.17885*	*0.17786*	*-0.556*
c880	*0.10857*	*0.10927*	*0.643*
c1355	*0.13828*	*0.14236*	*2.950*
c1908	*0.22508*	*0.21437*	*-4.758*
c2670	*0.34197*	*0.34638*	*1.290*
c5315	*0.70782*	*0.71171*	*0.549*
c7552	*0.99772*	*0.97618*	*-2.158*

Table 2: Average leakage power estimates with SP method.

conditions. For each circuit, we evaluated total leakage current for a sample of 10000 randomly generated input vectors. Each primary input is assumed to have binary node occurrence probability of 0.5. The average leakage is computed simply by taking the arithmetic mean. We observed that 10000 samples are sufficient for an accurate estimation.

Then we ran a small C-program that calculates the SP estimate for average leakage. Table 2 shows the results obtained with the SP method. Note the excellent agreement between the actual results and SP estimates, as the average relative error is about 2%. For these circuits, the SP estimate is calculated many orders of magnitude faster than running circuit simulation with even a single input vector. This illustrates the computational advantages of using the static approach in leakage estimation.

In previous section, we mentioned that the SP method can be used to predict different leakage components. Figure 6 shows gate and subthreshold leakage power estimates separately. The figure shows that the SP method can provide reasonably accurate and efficient estimates for critical leakage components. It is worth mentioning that these results can be performed at other process and environmental conditions if desired.

Normally for digital circuits, size and logic depth greatly impact the significance of spatial dependencies. Typically, one would expect more significant spatial dependencies for shallower circuits. Since the notion of the

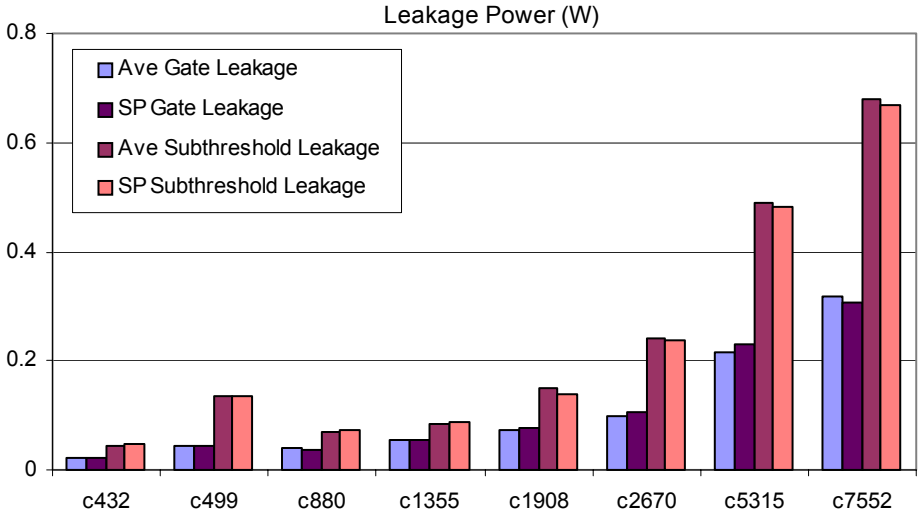


Figure 6. Estimation for leakage power components.

spatial dependency is hard to quantify and test, we performed a simple analysis on the robustness of the SP method with circuits of varying sizes and logic depths. By doing that, we see the behavior of the SP estimate at various levels of spatial correlation. We took c5315, which is originally implemented in 50 logic levels. By extracting the cells between the primary inputs and specified logic-depths, we can extract many sub-circuits with varying logic depths. These circuits will have different spatial dependencies although they share the same inputs. Figure 7 shows that the accuracy of the SP method is fairly consistent for different logic levels, hence the independence assumption is justified.

We now demonstrate an important feature of the SP method: handling given input probabilities. To illustrate this, we varied the node occurrence probability for the first four inputs of c1908 from 0.1 to 0.9 with 0.1 increments. Other inputs have an occurrence probability of 0.5. With these occurrence probabilities, we generated 10000 random input samples and calculated the average leakage using the circuit simulation. The results in Figure 8 show good agreement with the SP estimate and simulation results. The relative error is well bounded and is less than 5% at each datapoint. The special handling of the input probabilities is more useful when the

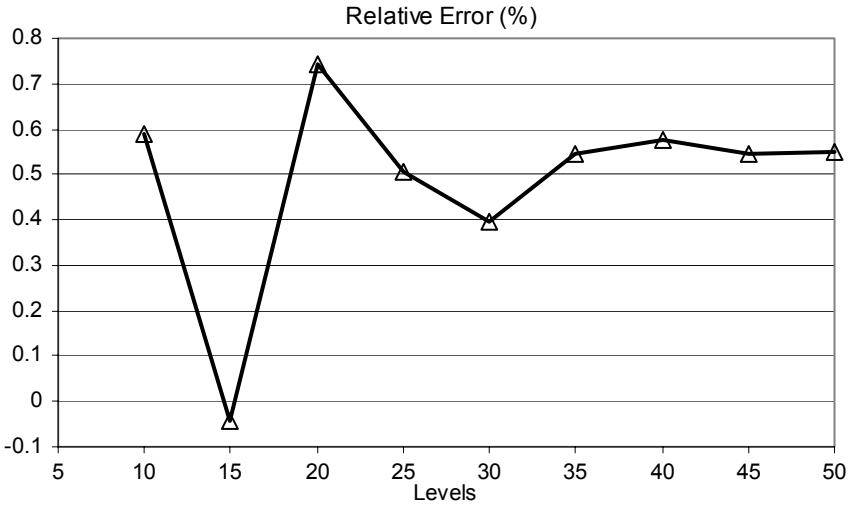


Figure 7. The relative error of the SP method for circuits with varying levels generated from C5315.

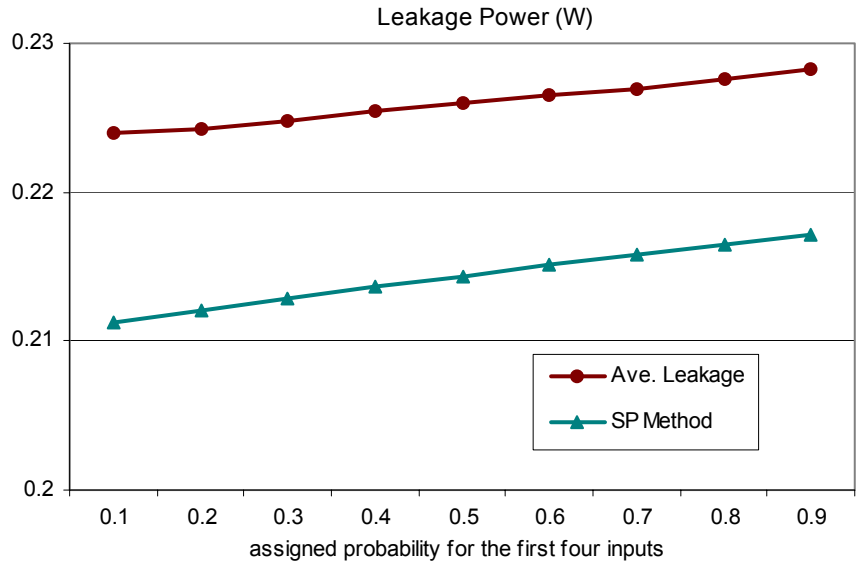


Figure 8. The SP estimate and average leakage for the case of specified occurrence probabilities for c1908.

occurence probabilities of a circuit (or a macro) are obtained from a higher-level analysis and simulation tool, possibly from a behavioral or architectural level analysis.

4. LEAKAGE SENSITIVITY

In Section 1, we showed that leakage is heavily dependent on key process and environmental parameters.

Hence, a thorough analysis framework must take into account dependencies on such key parameters. In doing so, designers would be able to assess leakage performance more reliably at nominal, favorable and adverse operating conditions.

One approach to assess the dependency of leakage on a particular process/environmental parameter, p, is to estimate the average leakage at different p's. This requires the design components (gates) to be pre-characterized for all p's and leakage estimates to be calculated using different tables. An alternative for modeling the parametric dependency is estimating the sensitivity of average leakage with respect to p.

We assume that the sensitivities of the total leakage for a gate at each input, i.e. $d(L_i(x_i))/dp$'s, are available in the pre-characterized library. This is fairly straightforward in library pre-characterization step. Moreover, we assume that the variation in p does not change the logical state of the circuit. This assumption is fairly valid due to the assumed robustness of logic functionality with respect to process/environmental conditions. This would imply that state occurrence probabilities are independent of p. Therefore, the estimate for the average leakage sensitivity to p can be written in the same manner as the nominal estimate (5) as:

$$\frac{d\hat{\mu}_{SP,\,L_{tot}}}{dp} = \sum_i \sum_{x_i} \hat{\Pi}_i(x_i) \frac{dL_i(x_i)}{dp}. \tag{7}$$

Similarly, higher order sensitivities would be:

$$\frac{d^n \hat{\mu}_{SP,\,L_{tot}}}{dp^n} = \sum_i \sum_{x_i} \hat{\Pi}_i(x_i) \frac{d^n L_i(x_i)}{dp^n} \tag{8}$$

The sensitivities of average leakage to process and environmental parameters are essential to making realistic design decisions and optimization. In a power-aware methodology, the sensitivity to a controllable design parameter (e.g. threshold voltage or oxide thickness) is key to minimizing total power dissipation.

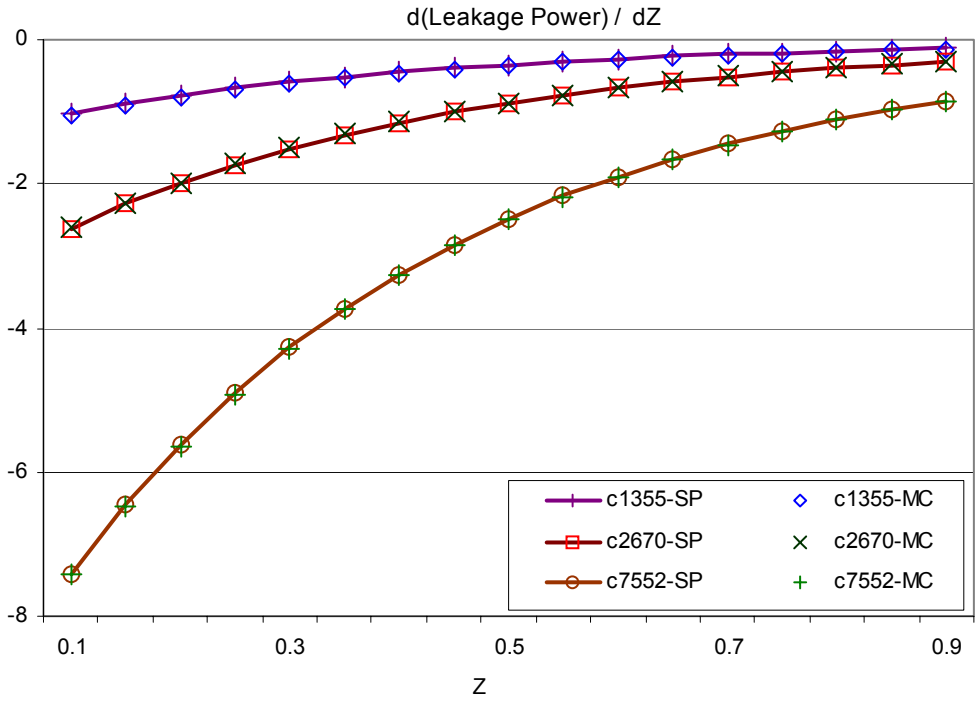


Figure 9. The sensitivity of average leakage to Z. MC refers to simulation results, SP for the proposed estimate

5. SENSITIVITY ESTIMATION RESULTS

This section presents experimental results for leakage sensitivity estimation. We investigated the leakage dependency of the ISCAS circuits on *Z*, a key process parameter. *Z* is a standardized parameter that represents process conditions between the best and worst case delay corners. The nominal process corresponds to *Z*=0.5. We calculated the leakage sensitivites of ISCAS circuits at different *Z* values using our circuit simulator. We also pre-characterized the leakage of the library elements (gates) at each input pattern and process conditions. The leakage sensitivities to *Z* for each gate and pattern are also available in the library.

Figure 9 shows the first order leakage sensitivities to *Z* for the ISCAS circuits, estimated both with the SP method (annotated with SP) and obtained from simulation results using 10000 random inputs (annotated with

Circuit	$\frac{d\hat{\mu}_{SP,L_{tot}}}{dZ}$			$\frac{d^2\hat{\mu}_{SP,L_{tot}}}{dZ^2}$		
	Actual	*SP method*	*rel. error (%)*	*Actual*	*SP method*	*rel. error (%)*
c432	*-9.40e-2*	*-9.32e-2*	*-0.68*	*2.43e-1*	*2.42e-1*	*-0.28*
c499	*-6.85e-2*	*-6.59e-2*	*-3.76*	*1.78e-1*	*1.72e-1*	*-3.12*
c880	*-2.74e-1*	*-2.74e-1*	*0.05*	*7.33e-1*	*7.33e-1*	*0.07*
c1355	*-3.59e-1*	*-3.48e-1*	*-2.9*	*9.56e-1*	*9.19e-1*	*-3.86*
c1908	*-5.29e-1*	*-5.30e-1*	*0.22*	*1.42e0*	*1.42e0*	*0.00*
c2670	*-8.75e-1*	*-8.81e-1*	*0.68*	*2.37e0*	*2.37e0*	*0.33*
c5315	*-1.76e0*	*-1.78e0*	*1.16*	*4.74e0*	*4.79e0*	*0.88*
c7552	*-2.49e0*	*-2.48e0*	*-0.28*	*6.73e0*	*6.71e0*	*-0.27*

Table 3: Sensitivities of average leakage power to *Z* at nominal process conditions (Z=0.5).

MC). The SP estimates agree well with the simulation results. In Table 3, the SP estimates for the first and second order sensitivities at the nominal process condition and relative estimation errors are also given. The results show that the SP method captures the sensitivities very accurately and can be calculated after the state occurence probability calculation. Similarly, one can perform similar analyses for sensitivities to threshold voltage, oxide thickness and VDD.

5.1 Modeling Parametric Dependencies

The leakage sensitivities are instrumental in optimizing and controlling the leakage, in yield calculations and in statistical analysis steps for leakage power. It may be also useful to approximate the parametric dependencies of leakage. For example, if we estimate the average leakage and its sensitivity to *Z* at nominal process conditions, we can construct an analytical model for the average leakage in terms of *Z*. This would obviate the need for pre-characterization of the gate library and estimating average leakage for these *Z* values. Hence, the leakage estimation process will be shortened. Next, we apply two emprical models to model dependency of leakage on *Z* and will compare it with simulation results from numerous Monte-Carlo runs.

The first model that uses the sensitivity information is a polynomial model. Using the estimates for the leak-

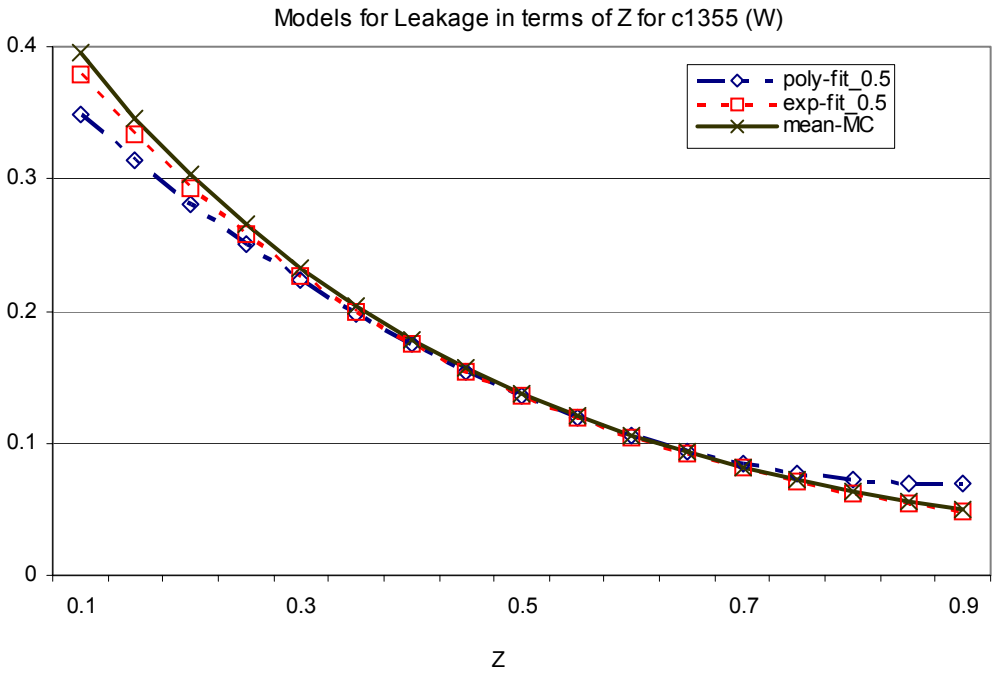


Figure 10. Modeling the leakage dependency of average leakage on Z using the sensitivities and linear and exponential models.

age and its sensitivities to Z at the nominal value ($Z_0 = 0.5$), we fit a second-order polynomial fit for the average leakage as:

$$\hat{\mu}_{L_{tot}}(Z_0) + \left.\frac{d\hat{\mu}_{L_{tot}}}{dZ}\right|_{Z_0}(Z - Z_0) + \left.\frac{d^2\hat{\mu}_{L_{tot}}}{dZ^2}\right|_{Z_0}\frac{(Z - Z_0)^2}{2} \tag{9}$$

The second model is an exponential fit mainly inspired by the nonlinear dependency on Z. The exponential model:

$$\alpha \exp(\beta Z) \tag{10}$$

where

$$\beta = \left.\frac{d\hat{\mu}_{SP,L_{tot}}}{dZ}\right|_{Z_0} / \hat{\mu}_{SP,L_{tot}}(Z_0) \text{ and } \alpha = \frac{\hat{\mu}_{SP,L_{tot}}(Z_0)}{\exp(\beta Z_0)}. \tag{11}$$

uses the leakage estimate and the first-order sensitivity information. One may generate other models using the

leakage estimates and its sensitivities at other evaluation points. Figure 10 shows the fits from these two models and the results obtained from extensive Monte-Carlo simulations for C1355. The plot shows that exponential fit is slightly more accurate than the linear fit for this example. These emprical models and the use of sensitivities reduce the characterization effort at many sample points, and give important intuition on the parametric dependencies of average leakage.

6. CONCLUSIONS

Static leakage estimation techniques are presented in this paper. It is demonstrated that the input dependency of the leakage is less than dependencies on process and environmental variations for many combinational circuits. The proposed SP method uses a probabilistic method to estimate of the average leakage of a combinational circuit, its components and sensitivities to process and environmental parameters. The efficient and accurate estimation of leakage and its sensitivities will be crucial in various stages of future power-aware design methodologies.

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