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Scaling MOSFETs to the Limit: A Physicist's Perspective

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Scaling MOSFETs to the limit: A physicists's perspective

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Abstract. **To circumvent its present practical limits – mainly gate leakage and poor performance – 'MOSFET scaling' has taken a different meaning: Not simply shrinking the device, but changing its nature. Here it is suggested that long-range Coulomb interactions constitute a possible fundamental cause of the poor performance of sub-50 nm devices. Alternative device-designs and materials are briefly discussed from a transport-physics perpsective: High-κ insulators, transport in thin Si body (SOI and double-gate), along different crystal directions and on different materials. The major role played by the interfaces (surface plasmons and phonons, roughness, confinement) emerges as one of the most important common elements.**
Keywords: Scaling, Coulomb interactions, high-κ insulators, strained Si, surface roughness

I. INTRODUCTION

Historically, scaling Metal-Oxide-Semiconductor field-effect transistors (MOSFETs) has simply meant considering a well-designed device (*i.e.*, electrostatically long-channel), reducing its linear dimensions, and understanding the modifications required to preserve its good electrostatic behavior (supply bias, junction depths, doping concentrations, gate insulator thickness, etc).[1]

Recently, because of concerns that this *evolutionary* approach may soon reach its practical and theoretical limits, the word 'scaling' has taken a different *revolutionary* meaning: As the linear dimensions of the MOSFET are reduced, novel device designs (*e.g.*, silicon-on-insulator, ground-plane, double-gate FETs) novel channel (most notably, strained Si or Ge) and gate-insulator (high-κ) materials, and novel contact designs (raised source and drain) are being considered. Thus, the problems a physicist has to confront when facing the 'limits of scaling' have moved from the clean and elegant realm of mesoscopic and quantum phenomena to a more mundane, varied, and confusing environment.

Thus, here scaling will be considered from a practical – but still deeply rooted in physics - perspective: First, 'mundane' effects seem to limit device scaling before 'elegant' phenomena become dominant: Tunneling across the gate insulator (gate leakage) is universally recognized as one of the major 'show-stoppers' in scaling, insulators with a higher dielectric constant (high-κ) being actively investigated to circumvent this problem. But disappointing performance of 'conventional' (*i.e.*, bulk) aggressively scaled MOSFETs is another concern whose possible fundamental cause I shall consider in Sec. II. Next I will consider some basic issues regarding the poor electron mobilities observed when using high-κ insulators (Sec. III), arguing that it is the high-κ itself which is the unavoidable cause of the problem. I shall next outline the 'mystery' of the high electron mobilities observed in strained-Si channels (Sec. IV), and, finally, conclude with a brief discussion of what limits the carrier mobility in thin-body devices – with a special emphasis on how to look at scattering with interface roughness – and at some opportunities we may have in improving device performance moving, if not to alternative semiconductors, at least to surface orientations different from the 'canonical' (100) surfaces.

II. LONG-RANGE COULOMB INTERACTIONS

'Conventional' scaling, as stated above, demands increasing doping concentrations in the substrate, drain, and source regions and a reduction of the insulator thickness. Thus, electrons in the conducting channel are in ever closer proximity to the high-density electron gases present in the source and drain regions – separated from each other by as little as tens of nanometers – and in the polycrystalline Si gate – separated from the channel by as little as 1.5 nm of SiO_2 (Ref. 2). As studied by us before[3], the role of these long-range Coulomb interactions is twofold: **1.** The interaction between electrons in the channel and the high-density electron gases in the source and drain regions can be pictured classically as a reshaping of the electron distribution in the channel caused by the potential-fluctuations, associated with plasma oscillations in the source and drain regions, 'leaking' into the low-density channel. Quantum-mechanically, this corresponds to emission and absorption of plasmons by the channel-electrons. While these processes do not subtract directly momentum from the electron gas, their net effect is a 'thermalization' of the hot-electrons energy-distribution in the channel, the resulting higher energy tail (whose presence has been recently inferred experimentally[4]) being affected by additional momentum-relaxation processes (phonons, ionized impurities). This causes, *indirectly*, a reduction of the effective electron velocity in the channel, and so, a depression of the transconductance as the channel length is reduced below about 4 nm, as illustrated in Fig. 1

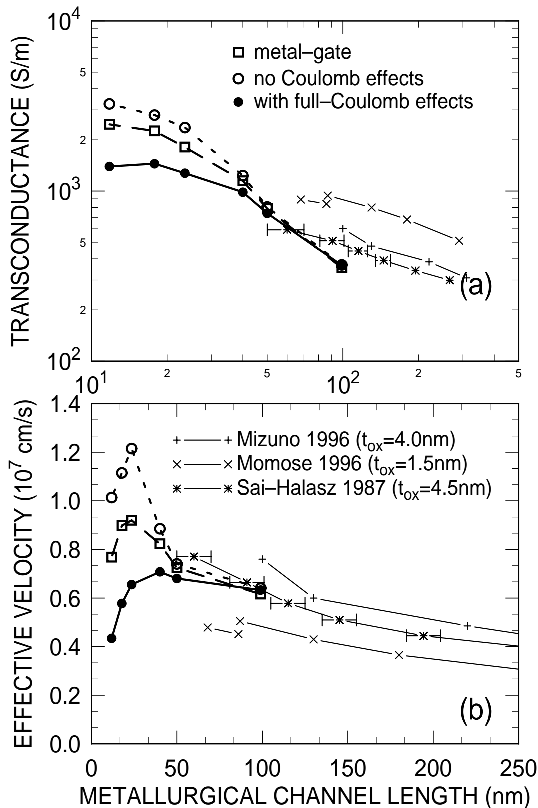

FIG. 1. (a) Room temperature transconductance g_m and (b) 'effective electron velocity' – transconductance divided by gate capacitance – g_m/C_g, obtained from two-dimensional Monte Carlo simulations of n-MOSFETs scaled from a 'nominal' 50 nm channel-length/2.8 nm-thick oxide to smaller (11.8/0.7 nm) and larger (100/5.6 nm) devices. Results obtained accounting for Coulomb interactions with the S/D and G regions (dots, 'full Coulomb') are compared to results obtained by ignoring the channel-gate interaction (open squares, labeled 'metal gate'), and all long- and short-range Coulomb interaction (circles, 'no Coulomb'). The transconductance has been evaluated from the difference in calculated drain current at gate-to-source biases of 1.0 V and 0.75 V. above threshold at 1.0 V of drain-to-source bias. Finally, comparison is made with some published experimental data.

together with some experimental data[2,5,6]. Such a disappointing behavior of aggressively scaled 'bulk' devices has been recently emphasized by the MIT group[7]. **2.** On the other hand, the interaction between channel-electrons and electrons in the gate ('Coulomb drag' across the very thin insulator) results in a *direct* loss of momentum of the electrons in the channel. Semiclassically, this interaction – also plasmon-mediated – has been estimated using our Monte Carlo program DAMOCLES[3] and, quantum mechanically, with calculations of the electron mobility in quantized Si channels performed by considering, in addition to the 'usual' momentum-relaxation processes (with Si phonons and interface roughness), also the momentum relaxation caused by the interaction of the two-dimensional electrons with the interface plasmons localized at the SiO_2/gate (poly-crystalline Si, assumed to be pure crystalline Si) interface. Both calculations predict a significant depression of the electron velocity for SiO_2 layers thinner than about 2-3 nm. This behavior has been observed experimentally[8–11], recent results[12] being in quantitative agreement with our early estimates[3].

The net conclusion we can draw from these results is that shrinking devices below the 4 nm-channel-length and the 2 nm-SiO_2-thickness regimes is not likely to result in any performance gain. In other words, the 'ballistic limit' may remain a pipe dream: Shorter channels are required for ballistic transport to occur. But as this is done, while also scaling the gate-insulator thickness, unavoidable Coulomb interactions gain strength, killing the concept of 'ballistic transport' at its onset.

III. ELECTRON MOBILITY IN HIGH-κ MOSFETS

Materials like metal oxides (such as Al_2O_3, HfO_2, ZrO_2), silicates (such as $HfSiO_4$ and $ZrSiO_4$), rare-earth oxides, and even perovskites have been considered as possible candidates to replace SiO_2. Clearly, issues related to material composition and processing have been the first obstacles met. So, early disappointing results regarding the low electron mobilities measured in high-κ Si MOSFETs were usually explained in terms of Coulomb scattering with defects, impurities, fixed charges and interface traps present in these high-κ stacks. Yet, as processing slowly begins to be controlled and better (*i.e.*, more ideal) materials become available, it is becoming apparent that the mobilities, while improved from early attempts, remain below expectations based on the Si-SiO_2 system. Once more, we have pointed out that something intrinsically related to the larger dielectric constant is at play.

The large static dielectric constant of an insulator can only originate from its ionic response – as its electronic response cannot increase without reducing the direct gap of the material. This implies the presence of soft optical phonons of large oscillator strength, because the bonds responsible for the large value of κ must be easily polarizable (hence the low energy of the phonons) and produce a large microscopic field (hence the large oscillator strength and so the large κ). (By contrast, the 'hard' Si-O bonds in SiO_2 yield a reduced ionic polarization. Associated with 'hard' bonds are high-energy optical phonons.) The large oscillator strength of these modes means that they couple very effectively with the electrons in the channel. Their low energy means that thermal electrons can easily emit and (at least at room temperature) absorb them. Both consideration show that, because of this additional scattering process – called 'remote phonon scattering'[13–15] –, one should expect a lower electron mobility in the channel of MOSFETs using high-κ insulators. In Ref. 16 we have indeed shown

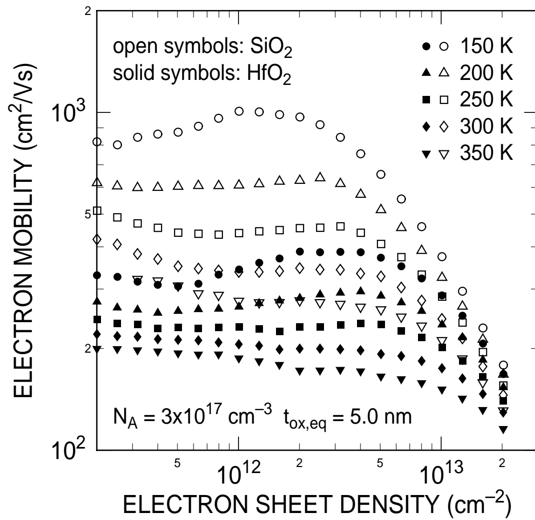

FIG. 2. Calculated electron mobility in Si inversion layers of Si-SiO_2 (open symbols) and Si-HfO_2 (solid symbols) as a function of carrier sheet density at various temperatures employing self-consistent Schrödinger-Poisson solutions at a concentration of 3 $\times 10^{17}$ acceptors/cm3 in the substrate. However, no Coulomb scattering with these impurities is accounted for in the calculations. Despite this, note the increasing role played by remote-phonon scattering at low densities, effects which vanishes at low substrate doping. Note also how at deceasing temperatures the mobility for the Si-HfO_2-system becomes increasingly worse than that for the Si-SiO_2-system.

that insulators with the larger dielectric constants exhibit the poorest mobilities. Thus, HfO_2 and ZrO_2 ($\kappa \approx$ 20-24) exhibited 'peak' mobilities a factor of 2 (or worse) lower than SiO_2, while their silicates ($\kappa \approx$ 10-12) appeared to be satisfactory. Figure 2 illustrates the results obtained for the Si/HfO_2/(poly)Si system, compared to the Si/SiO_2/(poly)Si system as a function of lattice temperature, having now employed a self-consistent Poisson-Schrödinger solution to calculate the subband energies and wavefunction in the channel. Note the significantly lower mobility for HfO_2, the fact that the additional scattering with remote phonons is still noticeable at reduced temperatures, and its weak dependence on the electron sheet density n_s. Of interest is also the fact that these calculations do not account for Coulomb scattering with ionized impurities in the Si depletion layer. Yet, as the electron density decreases, the mobility reaches a plateau, as usually expected for Coulomb scattering. This effect – not visible when using the triangular-well approximation – results from the fact that as n_s decreases below 2-to-5 $\times 10^{12}$ cm^{-2} the confinement in the inversion layer is mainly due to the charge of the substrate dopants (hence the famous 'effective field' concept). As n_s is reduced, so are both the strength of dielectric screening as well as the Fermi wavevector, K_F, of the electron gas. Since the scattering field of the surface-optical modes decays as $\exp(-Qz)$ as z moves deep into the Si substrate (the Si-SiO_2 interface being assumed to be located at $z = 0$), and electrons around the Fermi surface contribute to the mobility, the matrix element $\int \psi_i(z) \exp(-K_F z)\psi_i(z)dz$ (where ψ_i is the electron wavefunction in subband i) will grow with decreasing K_F (and so n_s), while dielectric screening weakens. Therefore, the electron mobility decreases. At even lower n_s confinement finally begins to weaken as well, and the mobility climbs towards its bulk value. Since screening gains strength at lower temperatures, this effect is even more significant below 250 K.

IV. ELECTRON TRANSPORT IN STRAINED SI

A second example of 'revolutionary' scaling is given by the search for 'faster' semiconductors. Strained Si is the most striking recent example. Here the problem we face is of a different nature: We do not understand the cause of the significant enhancements (with respect to relaxed Si) of the electron mobility observed in inversion layers of Si grown on relaxed $Si_{1-x}Ge_x$ substrates[17–24].

As explained in Ref. 25, the source of the difficulty lies in the simple observation that the electron confinement caused by the inversion-potential at the Si-SiO_2 interface lifts the degeneracy of the six conduction-band minima, exactly as tensile in-plane strain does. Thus, at a sufficiently large confinement potential (large gate bias, large n_s or 'effective field' F_{eff}), the energy $E_{0'}$ of the first four-fold degenerate 'primed' subband (in the usual terminology[36]) will be sufficiently larger than the energy E_0 of the ground-state doubly-degenerate 'unprimed' subband, to render ineffective the additional energy-shift caused by the tensile strain. In other words: The curves mobility-*vs.*-F_{eff} for relaxed and strained Si should merge at large F_{eff}. These expectations are far from what is observed. Figure 3 shows the vast disagreement between experimental results and theoretical expectations. Having expressed in print our puzzlement and having noticed that the experimental data could be explained only with the *ad hoc* assumption of a reduced scattering with interfacial roughness[25], an interesting study[26] was brought to our attention[27]: Molecular dynamics simulations and experiments performed on the reconstructed Si surface seem to indicated that indeed the surface of tensilely strained Si may be smoother. While this result does not directly address oxidized interfaces, it gives us a glimmer of hope.

V. CARRIER MOBILITY IN THIN SI LAYERS

Scattering with interface roughness clearly dominates the picture when considering electronic transport in thin Si layers, as for thin-body, fully-depleted SOI and double-gate FETs. The behavior of the electron mobility in this context has been extensively studied before theoretically[28–31] and experimentally[32,30].

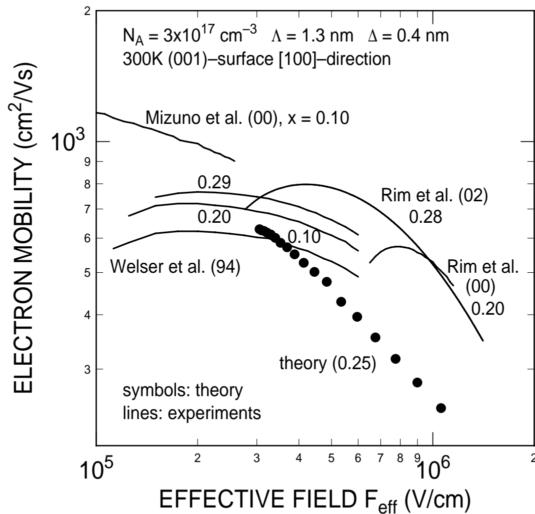

FIG. 3. Calculated electron mobility in strained-Si (grown on $Si_{0.75}Ge_{0.25}$, solid symbols) inversion layers wityh the indicated values for the surface-roughness Experimental data from Refs. 17, 21, 22, and 23 are also shown by the solid lines labeled by the corresponding substrate-Ge mole-fraction.

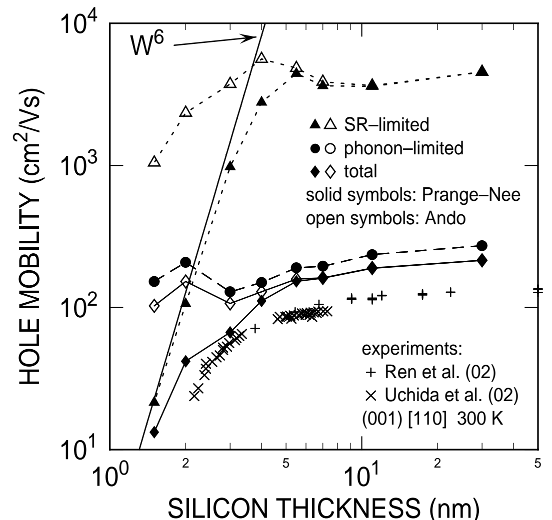

FIG. 4. Calculated total (diamonds), phonon-limited (circles), and surface-roughness-limited (triangles) hole mobility for the (001) surface along the [110] direction at 300 K and a surface field of 4×10^5 V/cm ($n_s \approx 2.6 \times 10^{12}$ cm^{-2}) as a function of the thickness of the Si layer. The symbols are calculated data, the lines are only a guide to the eye. Experimental data from Ren *et al.* (Ref. 33, open diamonds, for $n_s \approx 3 \times 10^{12}$ cm^{-2}) and Uchida *et al.* (Ref. 30, open squares, for $F_{eff} = 3 \times 10^5$ V/cm) are also shown. The dotted line shows the 'expected' W^6 dependence of the mobility in the regime in which scattering with surface-roughness dominates transport in thin layers. Open symbols indicate results obtained using Ando's model, solid symbols those obtained using Prange and Nee's model.

Focussing here on the less-studied subject of hole transport, we show in Fig. 4 recent experimental data[30,33] and calculations (using a 6-band $\mathbf{k}\cdot\mathbf{p}$ model[34]) of the 300 K hole mobility at a density of about 2.6 $\times 10^{12}$ cm^{-2} as a function of Si thickness. While the figure shows the expected trends mimicking the behavior of the electron mobility, the point to be noticed is that the results depend strongly on the particular model employed to treat scattering with interface roughness.

The well-known model proposed by Ando[36] considers scattering with two major roughness-related perturbations: **1.** The 'direct scattering at the step', with the associated matrix element $S(Q)\int \psi_i(z)(dV(z)/dz)\psi_j(z)dz$, where $V(z)$ is the confining potential and $S(Q)$ the Fourier transform of the autocovariance of the roughness. **2.** The Coulomb perturbation arising from the displacement of the carrier density at the steps and the dipole moments induced by the surface polarization and image charges. The first term is responsible for the expected F_{eff}^{-2} dependence of the mobility on the effective confining field F_{eff}. The remaining Coulomb terms, seldom accounted for, can be equally important and are periodically rediscovered (see Ref. 37 for a recent well formulated example). In the present context, term **1.** cannot account for variations of the thickness of the layer, as it accounts only for the confinement due to the field and not to the thin-film geometry. A reformulation is required, as explained in Refs. 34, 35. The original formulation by Prange and Nee[38], also used before in thin III-V layers[39,40], appropriately reformulated for a 6-band $\mathbf{k}\cdot\mathbf{p}$ model[34], is seen in Fig. 4 (solid symbols) to yield a satisfactory agreement with recent experimental data[30,33]. On the contrary, the naive use of the original Ando's model (admittedly conceived having bulk devices in mind...) badly overestimates the mobility (open symbols in Fig. 4. (An expression of the form $|S(Q)|^2 = \pi\Delta^2\Lambda^2/(1+Q^2\Lambda^2/2)^3$ has been used[41], with $\Delta = 0.4$ nm and $\Lambda = 2.6$ nm.) Interface roughness appears to dominate the mobility for Si layers thinner than

about 4 nm, similarly to what was found for electrons[35,39].

VI. CRYSTAL ORIENTATION

A final example of 'revolutionary' scaling is provided by the use interfaces aligned along crystallographic planes different from the 'usual' (001) surface, or even aligning the channel of the devices along directions different from the [110] commonly employed.

Figure 5 shows the expected performance gain in the case of Si *p*MOSFETs when moving to the (011) surface. Experimentally this effect is well-known (see the early references cited in Ref. 34). Of interest is the fact that calculations (performed with the 6-band $\mathbf{k}\cdot\mathbf{p}$ model mentioned above) reproduce qualitatively the correct trends: Experiments[43] exhibit consistently lower mobilities, presumably because of the current widespread use of nitrited oxides (effect ignored by the theory), but do show the expected good behavior of the (011) surface and the poor behavior of the (001) surface. Unfortunately, the electron mobility behaves in the diametrically opposite way.

Properties of structures farther away from the present mainstream technology are illustrated in Fig. 6. In the top frame of the figure the electron mobility in an inversion layer of the (111) surface of Ge (computed using the triangular-well approximation with the the inclusion of the L, X, and Γ-valleys and using the parameters of Ref. 42) is compared to the case of the (001) Si surface. The resulting optimistic picture – showing gains of up to a factor of two – must be taken with the usual 'grain of salt' which we should keep handy when using low-field mobilities to predict device performance. Indeed, despite claims to the contrary[44], low-field mobility and high-bias transconductance (or on-current) are only weakly related. The bottom frame of Fig. 6 shows the current-voltage characteristics of well-behaved small (effective channel length of about 25 nm) nMOSFETS fabricated on the two different surfaces (and materials). Assuming identical properties for the gate insulator and for the semiconductor/insulator interfaces, the 200% advantage of Ge(111) over Si(001) while still visible in the linear (low drain-to-source and gate biases) region, shrinks to 35% difference when looking at the transconductance at a gate overdrive of 0.7 V. It shrinks even more to insignificant differences at a gate overdrive of 1 V (not shown).

VII. CONCLUSIONS

'Revolutionary' scaling – the search for additional MOSFET performance by moving away from a conventional bulk, relaxed Si(001), SiO_2-based technology – is replacing 'evolutionary' scaling. This transition clearly

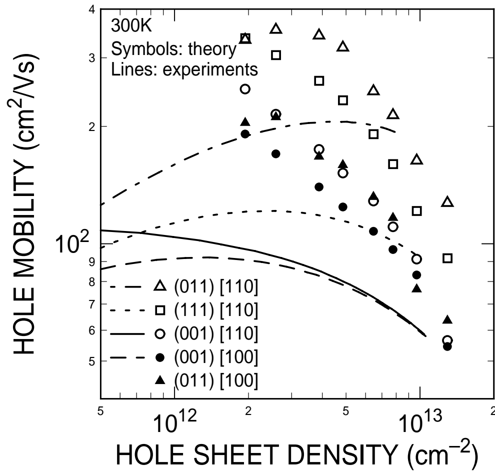

FIG. 5. Calculated total hole mobility at 300 K for the (001) surface along the [100] (dots) and [110] (circles) directions, for the (011) surface along the [100] (solid triangles) and [110] (open triangles) directions, and for the (111) surface along the [110] direction (open squares). Experimental data (Ref. 43) relative to the mobility along the [110] direction for the (001) (solid line), (011) (dot-dashed line), and (111) (dotted line) surfaces and along the [100] direction for the (001) (dashed line) are also shown.

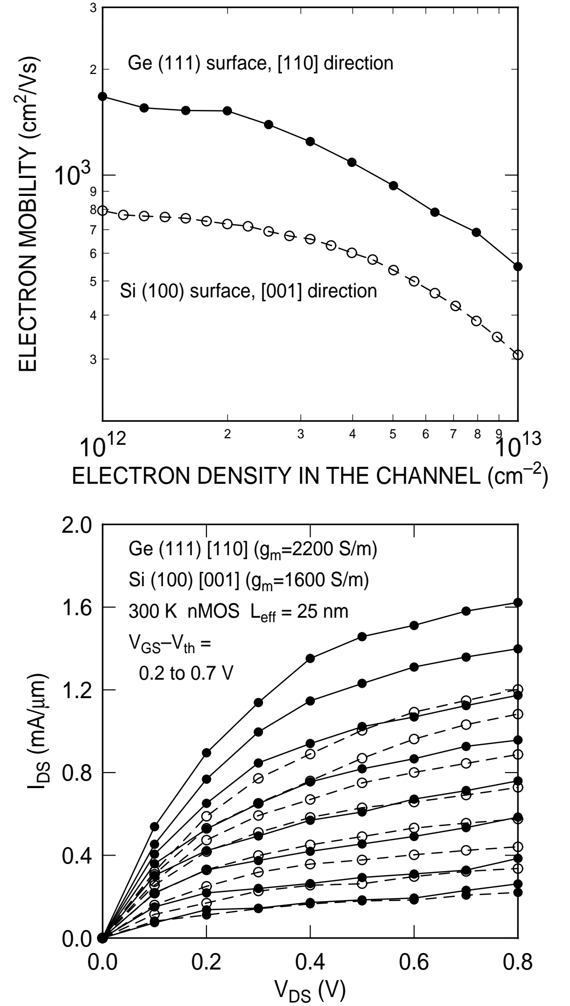

FIG. 6. (a) Calculated 300 K electron mobility in Ge and Si inversion layers on the (111) and (001) surfaces, respectively. (b) Calculated drain-current *vs.* drain-to-source voltage for nMOSFETs on the Ge(111) and Si(001) surfaces. The triangular well-approximation ans a simplified roiughness-roughness scattering model has been used to calculate the data shown in (a), while the self-consistent Monte Carlo/Poisson program DAMOCLES has been used to calculate the data shown in (b).

stems from the concern (fear? knowledge?) that the scaling of bulk Si devices will soon reach its limits. Rather than complex quantum-mechanical limits, these are proving to be instead mundane factors, gate-leakage and poor performance being the dominant ones. Having briefly discussed a possible fundamental cause of the poor behavior of sub-50 nm Si nMOSFTs, (namely, long-range Coulomb interactions), from a quick survey of new avenues open to the technology – high-κ insulators, strained Si, thin-body devices, alternative surface orientations and semiconductors – one common interesting fact has emerged: interfacial effects (plasma excitations, optical phonons, roughness, confinement) play the major role in determining the performance of the devices.

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[1] R. H. Dennard *et al.*, IEEE J. Solid State Circuits **SC-9**, 256 (1974).
[2] H. S. Momose *et al.*, Int. Electron Devices Meet., Tech. Dig. (IEEE, Piscataway, New Jersey, 1996), p. 105.
[3] M. V. Fischetti and S. E. Laux, J. Appl. Phys. **89**, 1205 (2001); M. V. Fischetti, J. Appl. Phys. **89**, 1232 (2001).
[4] K. G. Anil, S. Mahapatra, and I. Isele, Solid-State Electron. **47**, 995 (2003).
[5] T. Mizuno and R. Ohba, Int. Electron Devices Meet., Tech. Dig. (IEEE, Piscataway, New Jersey, 1996), p. 109.
[6] G. A. Sai-Halasz *et al.*, IEEE Electron Device Lett. **EDL-9**, 463 (1987).
[7] A. Lochtefeld and D. A. Antoniadis, IEEE Electron Device Lett. **22**, 95 (2001); D. A. Antoniadis, 2002 VLSI Symp. Tech. Dig. (IEEE, Piscataway, New Jersey, 2002) p. 2.
[8] A. Chin *et al.*, IEEE Electron Device Lett. **18**, 417 (1997).
[9] M. Krishnan *et al.*, Int. Electron Dev. Meet. Tech. Dig. (IEEE, Piscataway, New Jersey, 1998), p. 571; Int. Electron Dev. Meet. Tech. Dig. (IEEE, Piscataway, New Jersey, 1999), p. 241.
[10] N. Yang, W. Kirklen Henson, J. R. Hauser, and J. J. Wortman, IEEE Trans. Electron Devices, **47**, 440 (2000).
[11] G. Timp *et al.*, Int. Electron Devices Meet., Tech. Dig. (IEEE, Piscataway, New Jersey, 1997), p. 930.
[12] F. Lime, C. Guiducci, R. Clerc, G. Ghibaudo, C. Leroux, and T. Ernst, Solid-State Electron. **47**, 1147 (2003).
[13] S. Q. Wang and G. D. Mahan, Phys. Rev. B **6**, 4517 (1972).
[14] K. Hess and P. Vogl, Solid State Comm. **30**, 807 (1979)
[15] B. T. Moore and D. K. Ferry, J. Appl. Phys. **51**, 2603 (1980).
[16] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, J. Appl. Phys. **90**, 4587 (2001).
[17] J. Welser, J. L. Hoyt, S. Takagi, and J. F. Gibbons, Int. Electron Devices Meet., Tech. Dig. (IEEE, Piscataway, New Jersey, 1994), p. 373.
[18] S. Takagi, J. L. Hoyt, J. J. Welser, and J. F. Gibbons, J. Appl. Phys. **80**, 1567 (1996).
[19] K. Rim, J. L. Hoyt, and J. F. Gibbons, Int. Electron Devices Meet., Tech. Dig. (IEEE, Piscataway, New Jersey, 1998), p. 707.
[20] N. Sugii, K. Nakagawa, S. Yamaguchi, and M. Miyao, Appl. Phys. Lett. **75**, 2948 (1999).
[21] T. Mizuno, N. Sugiyama, H. Satake, and S. Takagi, 2000 Symposium on VLSI Tech. Dig. (IEEE, Piscataway, New Jersey, 2000), p. 210.
[22] K. Rim, J. L. Hoyt, and J. F. Gibbons, IEEE Trans. Electron Devices, **47**, 1406 (2000).
[23] K. Rim *et al.*, 2002 Symposium on VLSI Tech. Dig. (IEEE, Piscataway, New Jersey, 2002), p. 98.
[24] Hasan M. Nayfeh *et al.*, 60th Dev. Res. Conf. Dig. (IEEE, Piscataway, New Jersey, 2002), p. 43.
[25] M. V. Fischetti, F. Gámiz, and W. Hänsch, J. Appl. Phys. **92**, 7320 (2002)
[26] Y. H. Xie *et al.*, Phys. Rev. Lett. **73**, 3006 (1994).
[27] Thanks are due to Dr. Danny Chrastina, University of Warwick, for having brought Ref. 26 to my attention.
[28] F. Gámiz *et al.*, J. Appl. Phys. **86**, 6854 (1999).
[29] F. Gámiz and M. V. Fischetti, J. Appl. Phys. **89**, 5478 (2001).
[30] K. Uchida *et al.*, International Electron Device Meeting Tech. Digest (IEEE, Piscataway, New Jersey, 2002), p. 47.
[31] H. Iwata, J. Appl. Phys. **90**, 866 (2001).
[32] D. Esseni *et al.*, IEEE Trans. Electron Devices, **48**, 2842 (2001).
[33] Z. Ren *et al.*, International Electron Device Meeting Tech. Digest (IEEE, Piscataway, New Jersey, 2002), p. 51.
[34] M. V. Fischetti, Z. Ren, P. M. Solomon, M. Yang, and K. Rim, J. Appl. Phys. (to appear, Aug. 1, 2003).
[35] F. Gámiz *et al.*, J. Appl. Phys. **89**, 1764 (2001).
[36] T. Ando, J. Phys. Soc. Japan **43**, 1616 (1977); T. Ando, A. B. Fowler, and F. Stern, Rev. Mod. Phys. **54**, 437 (1982).
[37] C.-Y. Mou and T.-M. Hong, Phys. Rev. B **61**, 12612 (2000).
[38] R. E. Prange and T.-W. Nee, Phys. Rev. **168**, 779 (1968).
[39] A. Gold, Solid State Commun. **60**, 531 (1986); Phys. Rev. B **35**, 723 (1987).
[40] H. Sakaki *et al.*, Appl. Phys. Lett. **51**, 1934 (1987).
[41] D. R. Leadley *et al.*, Semicond. Sci. Technol. **17**, 708 (2002).
[42] M. V. Fischetti and S. E. Laux, J. Appl. Phys. **80**, 2234 (1996).
[43] M. Yang *et al.*, submitted to IEEE Electron. Device Lett. (2002).
[44] M. Lundstrom, IEEE Electron Device Lett. **18**, 361 (1997).