RC22853 (W0307-153) July 22, 2003
Electrical Engineering

IBM Research Report

The Assessment of On-chip Wire-length Distribution Models

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Abstract

This paper presents a comparison of wirelength distributions and interconnection count obtained with existing wirelength distribution models with on-chip wirelength distributions and actual number of interconnections in ASIC-like designs of a high-performance microprocessor. The actual distributions and number of interconnections are obtained from measurements of 100 control logic designs in the IBM POWER4 chip. In order to obtain wirelength distributions and estimates of number of interconnections with existing models, two empirical parameters are first extracted from the actual design data with the use of Rent's Rule. These two parameters are used as inputs in the existing models. Lack of agreement between the data and models is observed, and possible reasons for the lack of agreement are discussed and proposed as future work to improve existing models and to improve wirelength estimates.

Index Terms

ULSI, VLSI, circuit, design, wirelength distribution, wirelength models, Rent's Rule.

I. INTRODUCTION

An understanding of the amount of wire required to interconnect components in ultralarge-scale integrated (ULSI) systems is important to achieve buildable and functional chip designs within increasingly severe project constraints of real estate, number of metal layers, operating frequency, and power dissipation[1], [2], [3], [4], [5], [6], [7]. Although assessments of wirelength distributions and total wirelength requirements prior to actual chip implementation are important to achieve a successful design, such assessments are complex to implement and rely on incomplete design information particularly early in the design when designers typically rely on previous ad hoc design experience. Early assessments are tedious and typically occupy a large portion of the total time required to complete a chip for manufacturing. Wirelength assessments continue at regular intervals throughout a project; however, general methods do not exist to assess the accuracy of the assessments until after the design is complete and sent to manufacturing.

The goal of this work is to assess the extent to which existing wirelength distribution models agree with actual wirelength distributions for ASIC-like control logic designs in a high-performance microprocessor. Prior work has compared assessments obtained with the Donath (1979) and Donath (1981) models[9], [10] with chip data at that time; these models did not provide assessments with the accuracy we desire. A 1998 comparison of an assessment of wire

requirements with the Davis (1998) model[11], [12], [13] obtained Rent's parameters from fits to the wire distribution data[11]. In this paper, we provide wirelength distributions and wirelength requirements for 100 IBM POWER4 microprocessor designs. From the actual design data, we extract parameters that are referred to as Rent's parameters and then insert these parameters into existing wirelength models[8], [9], [10], [11], [12], [13]. We then compare the results of the models with actual wirelength distributions and wirelength requirements of 100 control logic designs in the IBM POWER4 core. This paper presents a comprehensive extraction of model parameters from all functional units of an actual microprocessor chip design and further use of these model parameters in existing wirelength models.

II. WIRELENGTH DISTRIBUTION MODELS

In this paper we will focus our attention on three existing wirelength distribution models that were published following the 1971 publication by Landman and Russo [16] of a summary of observations by E. F. Rent in two IBM memoranda. Since this time, Rent parameters have been obtained from linear fits to log-log plots of signal input and output terminals (IO) as a function of the number of gates [11]. These two parameters have been described with various notation; for example, the notation $\{K, r\}$ is used in Landman and Russo [16], $\{A, p\}$ is used in Donath (1979) [9], $\{A, p\}$ is used in Donath (1981) [10], and $\{k, p\}$ is used in Davis (1998) [11]. In the discussion in the rest of this paper, we will use the Davis notation $\{k, p\}$, where the notation k refers to the first parameter and p refers to the second parameter.

All three existing models assume that a design is a fully-packed tiled array of square gates, as illustrated in Fig. 1, where the width of each block is referred to as the *gatepitch*, which also equals the block height. The three models are summarized in Tables II- IV. Table II shows the model for the total number of interconnections derived by Donath (1979) [9] and models for the average wirelength derived by Donath (1979) [9] and by Davis (1998) [11]. Table III shows the models for the interconnection distribution function of Donath (1979) [9], Donath (1981) [10], and Davis [11], as well as models for the cumulative interconnection distribution function of Davis [11]. Table IV shows the normalized interconnection distribution function of Donath (1979) [9], Donath (1981) [10], and Davis [11] as well as models for the normalized cumulative interconnection distribution function of Davis [11]. In these expressions, the notation of each model is provided in Table I. Expressions for the total interconnection length follow from these

expressions by multiplying the appropriate expression for the average interconnection length by the total number of interconnections.

We now discuss a few specific details about each of the three existing models provided in Tables I- II.

A. 1979 Donath Model

In 1979 Donath [9] published expressions for the total number of connections and an upper bound on the average interconnection length for submodules arranged in tiled arrays of blocks. For an assembly of 4^L gates, where L is the number of levels of hierarchy placed according to a method described in this work, Donath obtained an expression for the total number of interconnections and interconnection distribution.

B. 1981 Donath Model

In 1981, Donath [10] derived an expression for the interconnection distribution of the number of nets between K-sized groups not connecting groups of size 4K, where K is given by the expression, $t_k = AK^p$ and where Donath states that "t_k is the number of terminals for a complex consisting of K elements" with length k, where Donath takes $k \sim \sqrt{K}$.

C. 1998 Davis Model

In 1998, Davis [11] et al. published expressions for a wirelength distribution for on-chip random logic networks. They state several assumptions, including: (1) "recursive application of Rent's Rule throughout an entire monolithic system;" (2) a square array of homogenerous logic gates; (3) each gate is a square with *width* equal to the *height* (*gatepitch*); (4) a minimum (maximum) wirelength in gatepitches of 1 ($2 \times \sqrt{N}$); (5) partitioning strategies [11] (see Fig. 13 in this reference); (6) total number of interconnections is given by Donath [9] as shown in Table II.

III. POWER4 ASIC-LIKE CONTROL DESIGNS

For our assessments of these three existing wirelength distribution models, we will choose 100 ASIC-like control logic designs in the IBM POWER4 core, which is currently incorporated

in the IBM Enterprise Server pSeries 680 and 690.[14], [15] In total, these 100 control designs occupy approximately 50% of the POWER4 core area; the two microprocessor cores occupy approximately one quarter of the area of each chip.[15] The reason we are interested in accurate assessments of wirelengths in these designs is that with them we can estimate wirelength requirements in significant portions of the microprocessor chip.

The physical design hierarchy of the POWER4 chip and examples of individual designs are shown in Fig. 2; the 18 control designs in the Instruction Fetch Unit (IFU) are the shaded regions on the left-hand side. Typical control designs are composed of logic books with uniform height, and the logic books have various widths that can be less than or greater than the gatepitch. The widths of typical logic books such as nand gates and inverters tend to be narrower than or on the order of the gatepitch, and the widths of more complex logic books such as local clock buffers tend to be wider than the gatepitch. In this paper, we will take the *gatepitch* to be equal to the height of the logic books, since all books have the same height. In addition, typical control designs can contain empty space between the books; a typical lower limit on empty space is approximately 20% in actual designs. An example of the physical design of a control design is shown in Fig. 3.

IV. Comparison of existing wirelength distribution models with chip design data

In this section, we present actual wirelength distributions and wirelength requirements of 100 actual control logic designs in the IBM POWER4 chip and compare these actual requirements with wirelength assessments obtained with three existing models. The method that we will use to perform the comparison is the following: First, we will extract the Rent parameter pair $\{k, p\}$ from the chip design data. Second, we will use the values of these parameters as inputs to the models. Third, we evaluate expressions for the average wirelength and total wirelength in each design based on the Davis model[11] and compare these values with values of average wirelength and total wirelength measured from the actual designs. Finally, we will evaluate expressions for the wirelength distribution functions of the Davis model[11] and compare with actual wirelength distribution functions.

The first step is to extract values of the Rent parameter pair $\{k, p\}$ from the chip design data. In this step, we identify all control designs in each of the six functional units of the POWER4 core

and count the number of input/output pins N_{IO} and number of gates N_{gates} used to implement design function. This data is shown in Fig. 4, where for designs in each of the six units, N_{IO} is plotted as a function of N_{gates}. By performing linear fits of the design data to the expression,

$$Log(N_{IO}) = Log(k) + p \times Log(N_{gates}), \tag{1}$$

we can extract values for $\{k, p\}$ for each unit; these values are shown in Table V. From the table, we see that $0.79 \leq k \leq 23.3$ and that $0.3 \leq p \leq 0.69$.

Next, we evaluate the expressions provided by the three models in Tables II- IV as functions of the values of the parameter pairs. With these expressions, estimates of the total number of interconnections $N(A, p)$, average wirelength $L_{avg}(p)$ and $\overline{R}(p)$, and total wirelength are obtained and are shown in Tables VI- VIII, respectively, where the range of each estimate is also shown. In these tables, the designs are listed in order of increasing N_{gates}. Table VI shows that the value of $N(A, p)$ underestimates N_{conn} for all designs by between 77% and 279%. The measured average wirelength L_a is obtained from the designs by averaging over all signal wirelengths according to the expression, $L_a = \frac{1}{N_{conn}} L_T$, where L_T is the measured total wirelength $L_T = \sum_{i=1}^{N_{conn}} L_i$ obtained by summing over the individual route lengths L_i of all interconnections i. Table VII shows a comparison of actual average wirelength values with estimates of the average wirelength obtained with the Davis model ($L_{avg}(p)$) and Donath model ($\overline{R}(p)$). The table shows that the value of $\overline{R}(p)$ agrees more closely with the measured value of L_a than is $L_{avg}(p)$. For the largest designs, the values for $\overline{R}(p)$ also tend to be closer to the values for L_a; the maximum Error for the Davis model is 105%. In these tables, the maximum Error for the Donath model is 48%; in these tables the Error is calculated by subtracting the actual average wirelength L_a from the estimate, and then dividing this quantity by the estimate. For example, for $L_{avg}(p)$, we take $Error = \frac{(L_a - L_{avg}(p)) * 100}{L_{avg}(p)}\%$; for $\overline{R}(p)$, we take $Error = \frac{(L_a - \overline{R}(p)) * 100}{\overline{R}(p)}$. We obtain estimates of the total wirelength requirement in each design by multiplying $L_{avg}(p) \times N(A, p)$; Table VIII shows a comparison of values for the total wirelength obtained in this manner with the measured total wirelengths. The minimum Error exceeds 85% and is as high as 544%. For the largest designs with $N_{gates} \geq 2323$, the Error is greater than 160%. Table IX summarizes the total measured wirelength and compares with estimates of the total wirelength $L_{tot}(p)$, where

we take $L_{tot}(p)$ to be given by the expression,

$$L_{tot}(p) = \sum_{i=1}^{N_{macros}} N(A,p) \times L_{avg}(p) \quad (2)$$

This table shows that $L_{tot}(p)$ approaches the total wirelength L_T only for the unit that contains only a few (4) macros. For three remaining units, $L_{tot}(p)$ overestimates L_T by $49\% - 80\%$ for three units and underestimates L_T by 79% and 200% for the remaining two units. For all designs, the estimate of the total wirelength requirements for all designs is within 60% of the actual value.

In the next step, the interconnection density function for each design and is compared with the actual interconnection density function. Expressions for the models in Table III are evaluated as functions of the parameter pair $\{k, p\}$ for four POWER4 Instruction Fetch Unit designs and are shown with the actual interconnection density function for the same four designs in Fig. 5. The interconnection density functions obtained from the design data are shown as solid circles, and the cumulative interconnection density functions are shown as hollow squares. The four designs shown in Fig. 5 are: (a) design7, (b) design1, (c) design2, and (d) design18. In this figure, distributions obtained with the three models for the interconnection density function are also shown, where values for $\{k, p\}$ are shown in Table V. The solid, dashed, and dotted lines indicate the distributions obtained with the Donath (1979) model, the Donath (1981) model, and the Davis (1998) model, respectively. The three solid lines that represent the Davis model are the estimate distribution, and the lower and upper bound on the estimate. This figure shows that the distributions obtained with the Donath model tend to underestimate the actual wirelength distributions; the distribution obtained with the Davis model also tends to underestimate the actual distribution, although the spread in the estimate as indicated by the upper and lower ranges appears to capture most of the actual distributions.

V. DISCUSSION

This paper presents an extensive comparison of actual wirelength distributions in a high-performance microprocessor chip designs with distributions obtained with three existing models. The goal of this work has been to assess the extent to which distributions obtained with existing models match the actual distributions. Of the three wirelength distributions obtained

with existing models shown in Fig. 5, the distribution obtained with the Donath (1979) model has curvature similar to that of the actual distribution, but it is offset and underestimates the number of interconnections with large wirelength. The distribution obtained with the Donath (1981) model is a straight line on the log-log plot rather than a curve similar to the observed distribution and tends to underestimate most the intermediate-length interconnections. The distribution obtained with the Davis (1998) model, where the ranges are shown as dotted lines around the central line, exhibits curvature similar to that in the actual distributions, and the dotted lines that indicate the ranges of this model tend to enclose the actual wirelength distribution. However, the ranges obtained with this model are large; the curve obtained with the Davis (1998) model underestimates the total number of interconnections, compared with the actual cumulative interconnection density function shown on the right-hand side of each figure. The total number of interconnections is underestimated because the Davis (1998) model is a function of the Donath expression for total number of interconnections[11]; this total number does not approximate well the actual number of interconnections in these designs.

We now speculate on possible reasons for the observed differences between the estimates of the total wirelength requirements and wirelength distributions obtained with existing models compared with wirelength distributions and wirelength requirements of actual chip designs:

(1) The assumptions of tiled arrays in the models are a simplification of the tiled gate structures in actual physical designs. The models also assume that physical designs are completely tiled with logic, are square, and are composed of square blocks. The actual physical designs considered in this work are typically (a) not completely filled with logic gates, in order to leave space for logical filler gates and decoupling capacitors, (b) rectangular, and (c) the logic blocks are typically rectangular, where the widths of the gates tend to be less than the height.

(2) The models typically assume unity fanout for signals in the designs. Actual physical designs considered here contain signals with unity fanout as well as signals with fanout much greater than unity.

(3) The square blocks are assumed to be interconnected within the physical design. Actual physical designs considered here are composed of interconnected logic gates upon which is superimposed a network of clocking circuitry that drives local clock buffers and latches in the design; this circuitry is typical of control designs in high-performance chips in which the logical signals need to be synchronized.

(4) Existing methods described in the literature, as for example in Ref. [11], indicate that values of the parameter pair $\{k, p\}$ are obtained from linear fits to log-log plots of the number of input/output pins N_{IO} as a function of gates N_{gates}. These methods are based on a 1971 interpretation of two IBM memoranda written by E. F. Rent in 1960.

We are interested in future work to investigate these four reasons in order to obtain improved wirelength distribution models.

VI. Conclusion

The goal of this work has been to assess how well existing wirelength distribution models agree with actual wirelength distributions for ASIC-like control logic designs in a high-performance microprocessor. In this paper, we have presented a comparison of on-chip wirelength distributions and actual number of interconnections in 100 IBM POWER4 designs with values obtained with existing wirelength distribution models. The comparison shows that the model estimates for the number of interconnections typically differs from the value of the actual interconnection count by approximately 100%. As a result, the model distributions tend to underestimate the actual wirelength distributions. Estimates of total wirelength obtained with existing models differ from actual wirelength requirements in each unit by between 5% and 209%. In this work we have learned that, in their current form, estimates obtained with existing models can differ by as much as 200% compared with actual values and that improved models are needed. Four assumptions of the models are reviewed, and we speculate that these assumptions may be possible reasons for the lack of agreement seen between the models and the actual distributions. We propose further investigation of these assumptions in order to help improve existing wirelength distribution models.

VII. Acknowledgments

We thank Thomas Bucelot, Cevdet Noyan, Leon Sigal, and James Warnock of IBM T. J. Watson Research Center, Yorktown Heights, NY, for discussions. We also thank Gerald Lopez and Jeff Davis, both of Georgia Institute of Technology, for discussions and for providing a copy of Dr. Davis' 1999 Ph.D. thesis with expressions in Tables II- IV. We also thank Kelvin Lewis and Izzy Bendrihem for supporting a seamless computing environment.

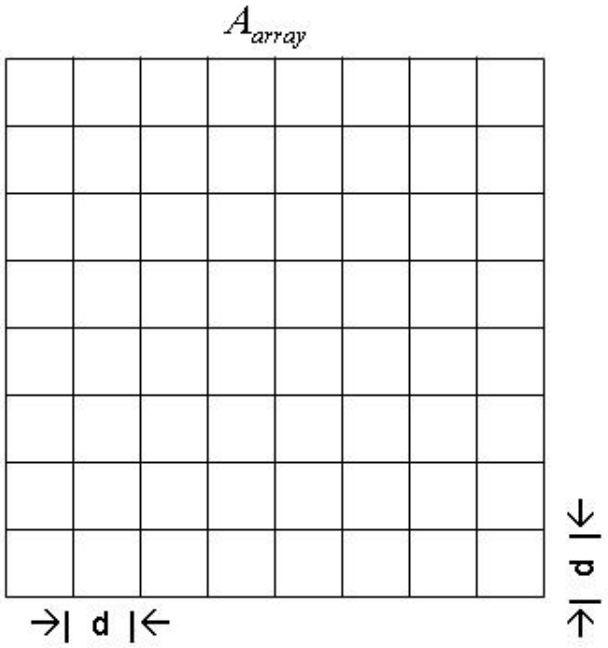

Fig. 1. Tiled 8×8 array composed of 64 square gates, where the gatepitch d is shown.

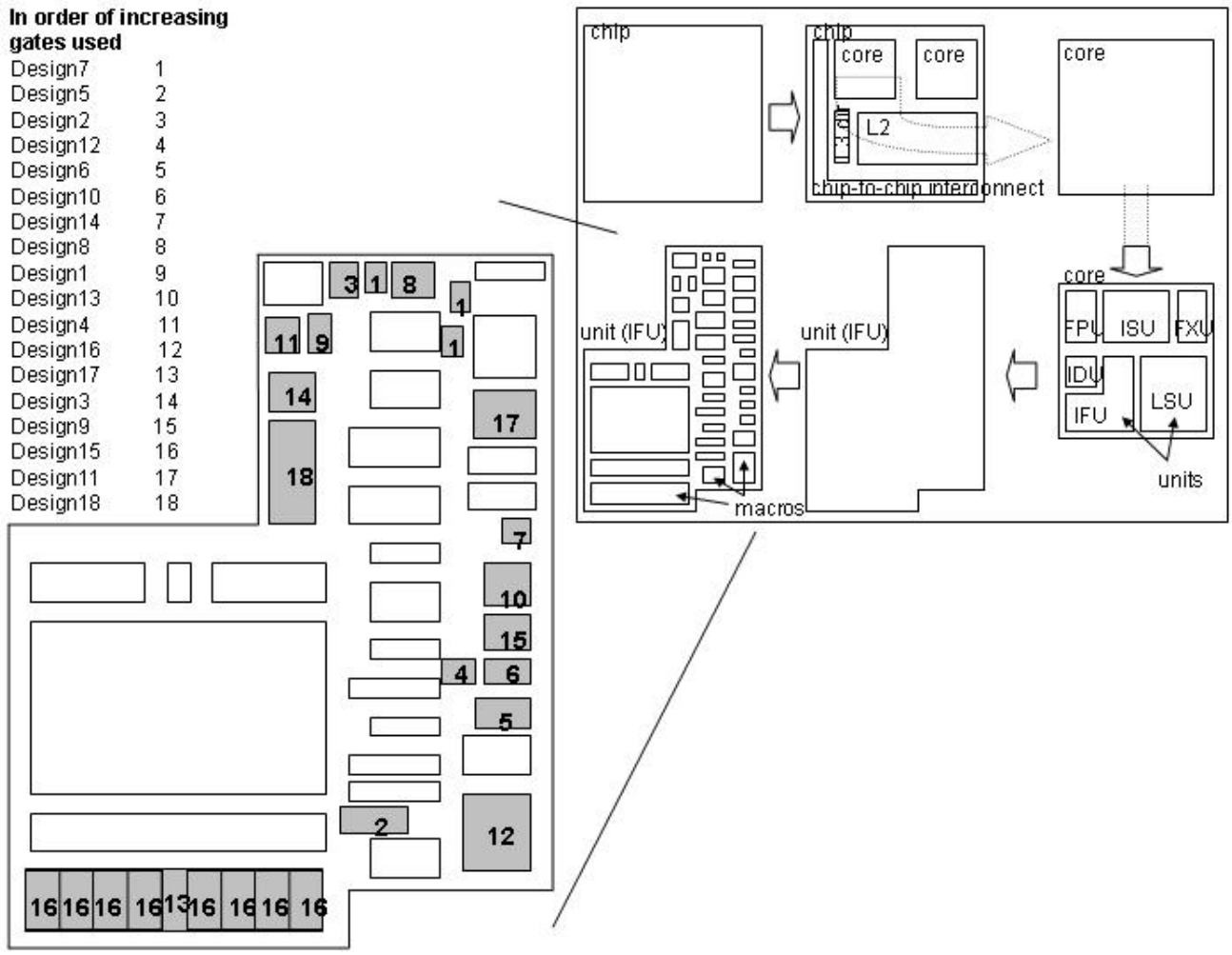

Fig. 2. Hierarchical physical design methodology for the POWER4 chip, with real estate for the Instruction Fetch Unit that contains actual transistor circuitry shown as rectangles on the lower left. The floorplan of POWER4 Instruction Fetch Unit is shown on the left with rlms shown as shaded rectangles in order of increasing number of used gates N_{gates}.

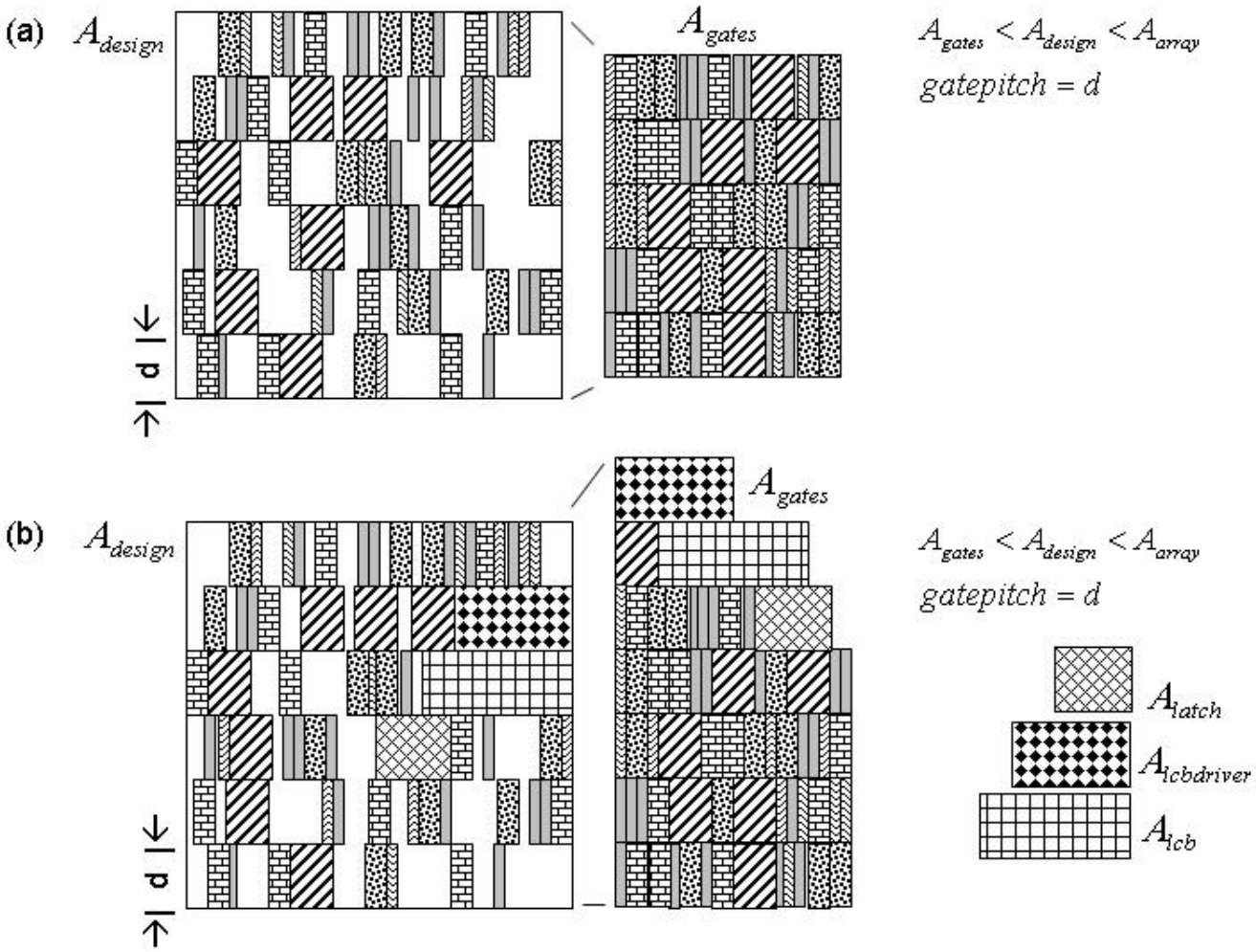

Fig. 3. Two examples of physical designs with 64 rectangular gates, where design shown contains (a) no clocking circuitry (zero latches) and (b) some clocking circuitry (1 latch and 1 local clock buffer). The gatepitch is d. A_{design} is the area of the design, A_{gates} is the area of the gates, and A_{array} is the area of the array shown in Fig. 1. In (b), A_{latch} is the area of the latch, $A_{lcbdriver}$ is the area of the lcbdriver (a buffer), and A_{lcb} is the area of the local clock buffer.

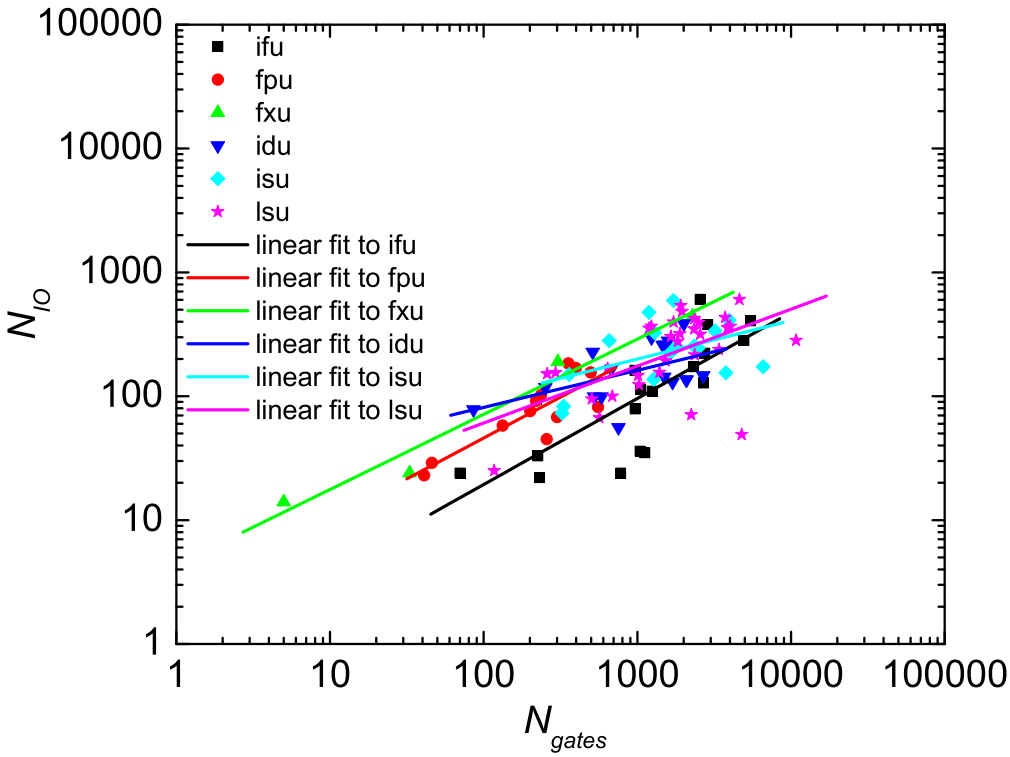

Fig. 4. Method to extract $\{k, p\}$ parameter pairs from designs with the method of Davis [11]: The number of input/output pins N_{IO} as a function of used gates N_{gates} for six units in POWER4 chip, to obtain parameters k and p values summarized in Table V.

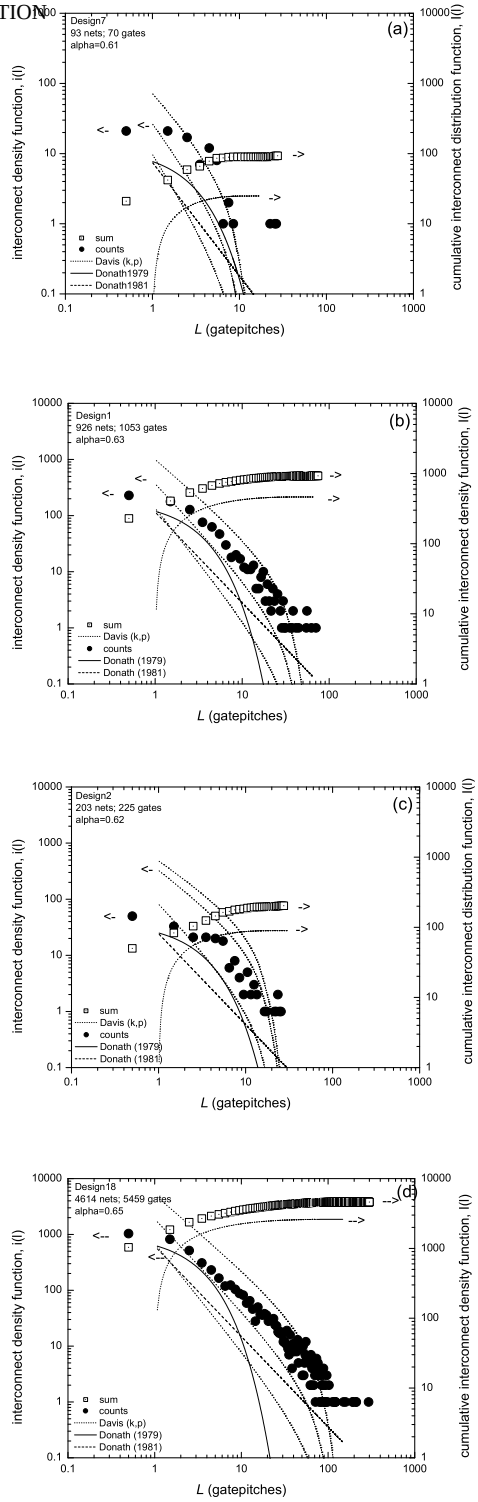

Fig. 5. Interconnection density function (solid circles) and cumulative interconnection density function (hollow squares) for four POWER4 Instruction Fetch Unit designs: (a) design7, (b) design1, (c) design2, and (d) design18. The three models for the interconnect density function are also shown, where the parameter pair $\{k, p\}$ from plots of IO versus gates shown in Table V is used in each model. For all macros, the gatepitch d is taken to be the book height of the standard cells. The solid line indicates the distribution obtained with the Donath (1979) model, the dashed line is obtained from the Donath (1981) model, and the dotted line is obtained from the Davis (1998) model.

TABLE I

EXPRESSIONS USED IN THE LITERATURE TO DESCRIBE RENT'S OBSERVATIONS, AND THE NOTATION ASSOCIATED WITH EACH EXPRESSION.

Reference	*Expression*
Landman and Russo (1971)[16]	$P = KB^r$ *P=''average number of pins per module''* *K=''average number of pins per block''* *B=''average number of blocks per module''* *r=exponent*
Donath (1979)[9]	$T = AC^p$ *A=''average terminals per gate''* *C=''average number of gates in a group of* 4^L*; L=int''* *P: a constant; ''0 < p < 1 is a constant* *T = ''average number of terminals required by a group containing an average of C gates''*
Donath (1981)[10]	$t_k = AK^p$ *K: number of elements in a group of C elements* *A:''number of terminals per individual complex''* *p:''the Rent exponent''* t_k*=number of terminals on k elements*
Davis (1998)[11]	$T = kN^p$ *N:number of gates in a random logic network* *k,p: ''empirical constants''* *T=''number of signal input and output (I/O) terminals''*

TABLE II

EXPRESSIONS PRESENTED IN THE LITERATURE FOR MODELS OF THE TOTAL NUMBER OF INTERCONNECTIONS AND THE AVERAGE WIRELENGTH IN DESIGNS, WHERE THE NOTATION IN EACH EXPRESSION IS GIVEN IN TABLE I.

Reference	*Number of Interconnections* $N(A,p)$	*Average Wirelength (*$\overline{R}(p)$ *and* $L_{avg}(p)$*)*
Donath (1979)[9]	$N(A,p) = \alpha AC(1 - C^{p-1})$	*for* $p \neq \frac{1}{2}$ *:* $\overline{R} = \frac{2}{9}\left(7\frac{\left(C^{p-1/2}-1\right)}{4^{p-1/2}-1} - \frac{1-C^{p-3/2}}{1-4^{p-3/2}}\right)\left(\frac{1-4^{p-1}}{1-C^{p-1}}\right)$ *for* $p = \frac{1}{2}$ *:* $\overline{R} = \frac{2}{9}\left(7log_4 C - \frac{1-C^{p-3/2}}{1-4^{p-3/2}}\right)\left(\frac{1-4^{p-1}}{1-C^{p-1}}\right)$
Donath (1981)[10]	*(assumed to be given by Donath 1979)*	-
Davis (1998)[11]	*(assumed to be given by Donath 1979)*	$L_{avg} = \frac{\left(\frac{p-0.5}{p} - \sqrt{N} - \frac{(p-0.5)}{6\sqrt{N}(p+0.5)} + N^p\left(\frac{-p-1+4^{p-0.5}}{2(p+0.5)(p)(p-1)}\right)\right)}{\left(N^{p-0.5}\frac{(-2p-1+2^{2p-1}}{2p(p-1)(2p-3)} - \frac{p-0.5}{6p\sqrt{N}} + 1 - \frac{(p-0.5)\sqrt{N}}{(p-1)}\right)}$

TABLE III

EXPRESSIONS PRESENTED IN THE LITERATURE FOR MODELS OF THE INTERCONNECTION DISTRIBUTION FUNCTION AND CUMULATIVE INTERCONNECT DISTRIBUTION FUNCTION.

Reference	*Interconnection Distribution (n_k, $i(l)$) and Cumulative Interconnection Distribution ($I(l)$)*
Donath (1979)[9]	$n_k = \alpha AC(1-4^{p-1})4^{k(p-1)}$ -
Donath (1981)[10]	$n_k \sim \alpha C k^{2p-2} \frac{1-4^{p-1}}{2k}$ -
Davis (1998)[11]	*for* $1 \leq l < \sqrt{N}$ *:* $i(l) = \frac{\alpha k}{2}\Gamma\left(\frac{l^3}{3} - 2\sqrt{N}l^2 + 2Nl\right) l^{2p-4}$ $I(l) = \frac{\alpha k}{2}\Gamma\left(\frac{l^{2p}-1}{6p} + 2\sqrt{N}\frac{-l^{2p-1}+1}{2p-1} - N\frac{\left(-l^{2p-2}+1\right)}{p-1}\right)$ *for* $\sqrt{N} \leq l < 2\sqrt{N}$ *:* $i(l) = \frac{\alpha k}{6}\Gamma\left(2\sqrt{N} - l\right)^3 l^{2p-4}$ $I(l) = \frac{\alpha k}{2}\Gamma\left(\frac{\sqrt{N}^{2p}-1}{6p} + 2\sqrt{N}\frac{-\sqrt{N}^{2p-1}+1}{2p-1} - N\frac{-\sqrt{N}^{2p-2}+1}{p-1}\right)$ $+\frac{\alpha k}{6}\Gamma\left(-8N^{3/2}\frac{-l^{2p-3}+N^{p-3/2}}{2p-3} + 6N\frac{-l^{2p-2}+N^{p-1}}{p-1} - 6\sqrt{N}\frac{-l^{2p-1}+N^{p-1/2}}{2p-1} + \frac{-l^{2p}+N^p}{2p}\right)$ *where* $\Gamma = \frac{2N\left(1-N^{p-1}\right)}{\left(-N^p\frac{(1+2p-2^{2p-1})}{p(2p-1)(p-1)(2p-3)} - \frac{1}{6p} + \frac{2\sqrt{N}}{2p-1} - \frac{N}{p-1}\right)}$

TABLE IV

EXPRESSIONS PRESENTED IN THE LITERATURE FOR MODELS OF THE NORMALIZED INTERCONNECTION DISTRIBUTION FUNCTION AND NORMALIZED CUMULATIVE INTERCONNECTION DISTRIBUTION FUNCTION, WHERE THE TOTAL NUMBER OF INTERCONNECTIONS ASSUMED IN EACH MODEL IS GIVEN BY THE EXPRESSION $N(A,p)$ SHOWN IN TABLE II.

Reference	*Normalized Interconnection Distribution (f_k, $p_{int}(l)$)* *Normalized Cumulative Interconnection Distribution ($P(l)$)*
Donath (1979)[9]	$f_k = \frac{1-4^{p-1}4^{k(p-1)}}{(1-C^{p-1})}$ -
Donath (1981)[10]	$f_k \sim \frac{k^{2p-2}\left(1-4^{p-1}\right)}{2kA(1-C^{p-1})}$ -
Davis (1998)[11]	*for* $1 \leq l < \sqrt{N}$ *:* $p_{int}(l) = \frac{1}{2N(1-N^{p-1})}\Gamma\left(\frac{l^3}{3} - 2\sqrt{N}l^2 + 2Nl\right) l^{2p-4}$ $P(l) = \frac{1}{2N(1-N^{p-1})}\Gamma\left(\frac{l^{2p}-1}{6p} + 2\sqrt{N}\frac{-l^{2p-1}+1}{(2p-1)} - N\frac{-l^{2p-2}+1}{(p-1)}\right)$ *for* $\sqrt{N} \leq l < 2\sqrt{N}$ *:* $p_{int}(l) = \frac{1}{6N(1-N^{p-1})}\Gamma\left(2\sqrt{N} - l\right)^3 l^{2p-4}$ $P(l) = \frac{1}{2N(1-N^{p-1})}\Gamma\left(\frac{\sqrt{N}^{2p}-1}{6p} + 2\sqrt{N}\frac{-\sqrt{N}^{2p-1}+1}{2p-1} - N\frac{-\sqrt{N}^{2p-2}+1}{p-1}\right)$ $+\frac{1}{6N(1-N^{p-1})}\Gamma\left(-8N^{3/2}\frac{-l^{2p-3}+N^{p-3/2}}{2p-3} + 6N\frac{-l^{2p-2}+N^{p-1}}{p-1} - 6\sqrt{N}\frac{-l^{2p-1}+N^{p-1/2}}{2p-1} + \frac{-l^{2p}+N^p}{2p}\right)$ *where* $\Gamma = \frac{2N\left(1-N^{p-1}\right)}{\left(-N^p\frac{\left(1+2p-2^{2p-1}\right)}{p(2p-1)(p-1)(2p-3)} - \frac{1}{6p} + \frac{2\sqrt{N}}{2p-1} - \frac{N}{p-1}\right)}$

TABLE V

VALUES FOR THE PARAMETER PAIR $\{k, p\}$ FOR EACH POWER4 UNIT, WHERE THE VALUES ARE EXTRACTED BY FITTING THE DATA FOR EACH UNIT IN FIG. 4 TO THE EXPRESSION $log(N_{IO}) = log(k) + p \times log(N_{gates})$.

unit	*macros*	k *[range]*	p *[range]*
ifu	18	$0.79[0.29, 2.14]$	$0.69[0.55, 0.84]$
fpu	12	$2.21[1.06, 4.58]$	$0.66[0.52, 0.79]$
fxu	4	$4.36[2.81, 6.78]$	$0.61[0.52, 0.69]$
idu	18	$20.5[8.44, 49.8]$	$0.30[0.17, 0.43]$
isu	16	$23.3[7.79, 69.9]$	$0.31[0.16, 0.46]$
lsu	32	$7.33[3.02, 17.8]$	$0.46[0.34, 0.58]$

TABLE VI

TOTAL NUMBER OF GATES N_{gates}, ACTUAL NUMBER OF INTERCONNECTIONS N_{conn}, PREDICTED NUMBER OF INTERCONNECTIONS $N(A,p)$ IN THE IFU, AND ERROR, WHERE $N(A,p)$ IS OBTAINED WITH TABLE II. HERE WE TAKE $Error = \frac{(N_{conn} - N(A,p)) * 100}{N(A,p)}\%$. THE ERROR IS SHOWN IN %.

design	N_{gates}	N_{conn}	$N(A,p)$ [range]	Error
i1	70	93	$24.5[10.6, 45.9]$	279
i2	220	318	$91.3[38.1, 179.7]$	248
i3	225	203	$89.2[37.2, 175.8]$	128
i4	231	255	$99.1[41.3, 195.6]$	157
i5	779	800	$353.3[142.7, 731.2]$	126
i6	964	996	$441.3[177.5, 920.5]$	126
i7	967	837	$442.7[178.0, 923.6]$	89
i8	1042	1051	$478.6[192.2, 1001.0]$	120
i9	1053	926	$461.9[185.4, 966.4]$	100
i10	1118	1147	$507.2[203.3, 1063.5]$	126
i11	1250	1030	$552.1[220.8, 1162.1]$	87
i12	2323	2131	$1115.1[441.0, 2396.5]$	91
i13	2561	2287	$1269.9[501.4, 2737.6]$	80
i14	2691	2358	$1278.3[504.3, 2760.0]$	84
i15	2746	2500	$1305.2[514.8, 2819.9]$	92
i16	2871	3046	$1407.8[554.8, 3045.9]$	116
i17	4934	4365	$2382.8[931.4, 5240.6]$	83
i18	5459	4614	$2602.8[1015.9, 5741.3]$	77

TABLE VII

MEASURED AVERAGE WIRELENGTH FOR IFU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p)$) AND DONATH ($\overline{R}(p)$) WITH TABLE II ARE ALSO SHOWN. NOTE THAT L_a, $L_{avg}(p)$, AND $\overline{R}(p)$ ARE EXPRESSED IN UNITS OF GATEPITCHES. FOR $L_{avg}(p)$, WE TAKE $Error = \frac{(L_a - L_{avg}(p)) * 100}{L_{avg}(p)}\%$; FOR $\overline{R}(p)$, WE TAKE $Error = \frac{(L_a - \overline{R}(p)) * 100}{\overline{R}(p)}$. THE ERROR FOR $\overline{R}(p)$ IS SHOWN IN THE RIGHT-HAND COLUMN. THE ERRORS ARE SHOWN IN %.

design	N_{gates}	L_a	$L_{avg}(p)$ *[range]*	*Error*	$\overline{R}(p)$ *[range]*	*Error*
i1	70	3.3	$2.4[2.2, 2.6]$	39	$2.9[2.6, 3.2]$	13
i2	220	5.5	$3.0[2.6, 3.5]$	85	$3.8[3.3, 4.5]$	43
i3	225	3.4	$3.0[2.6, 3.5]$	15	$3.9[3.3, 4.6]$	-12
i4	231	4.0	$3.0[2.6, 3.5]$	32	$3.9[3.3, 4.6]$	1.9
i5	779	3.7	$3.8[3.1, 4.8]$	-2	$5.2[4.1, 6.6]$	-27
i6	964	6.0	$4.0[3.2, 5.1]$	50	$5.4[4.2, 7.0]$	11
i7	967	5.4	$4.0[3.2, 5.1]$	35	$5.4[4.2, 7.0]$	-1
i8	1042	4.1	$4.1[3.3, 5.2]$	0	$5.5[4.3, 7.2]$	-27
i9	1053	4.6	$4.1[3.3, 5.2]$	1.4	$5.5[4.3, 7.2]$	-16
i10	1118	3.6	$4.1[3.3, 5.3]$	-1.2	$5.6[4.3, 7.4]$	-36
i11	1250	4.0	$4.2[3.3, 5.4]$	-4.4	$5.8[4.4, 7.6]$	-30
i12	2323	8.9	$4.8[3.7, 6.4]$	86	$6.6[4.8, 9.2]$	35
i13	2561	9.5	$4.9[3.7, 6.6]$	95	$6.8[4.9, 9.4]$	41
i14	2691	6.8	$4.9[3.7, 6.7]$	38	$6.8[4.9, 9.6]$	0
i15	2746	7.9	$4.9[3.7, 6.7]$	59	$6.9[4.9, 9.6]$	15
i16	2871	10.2	$5.0[3.8, 6.8]$	105	$6.9[5.0, 9.8]$	48
i17	4934	8.4	$5.6[4.1, 7.9]$	51	$7.8[5.4, 11.5]$	8
i18	5459	9.3	$5.7[4.1, 8.2]$	63	$8.0[5.4, 11.9]$	17

TABLE VIII

MEASURED TOTAL WIRELENGTH L_T FOR IFU DESIGNS $L_T = \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF TOTAL WIRELENGTH OBTAINED BY MULTIPLYING $L_{avg}(k,p)$ FROM THE DAVIS MODEL WITH THE ESTIMATED WITH THE NUMBER OF INTERCONNECTIONS $N(A,p)$ FROM THE DONATH MODEL. HERE WE TAKE $Error = \frac{(L_T - L_{avg}(p) \times N(A,p)) * 100}{L_{avg}(p) \times (N(A,p))}\%$. THE ERROR IS SHOWN IN %. NOTE THAT L_T AND $L_{avg}(p) \times N(A,p)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_T	$L_{avg}(p) \times N(A,p)$ *[range]*	*Error*
i1	70	305.5	58.2[53.1, 64.2]	425
i2	220	1745.8	271.1[236.0, 315.2]	544
i3	225	847.6	266.1[231.4, 309.7]	219
i4	231	1011.2	297.3[258.2, 346.5]	240
i5	779	2999.5	1352.7[1104.0, 1689.5]	122
i6	964	6218.3	1764.5[1422.9, 2233.6]	252
i7	967	4731.2	1771.4[1428.1, 2242.7]	167
i8	1042	4261.1	1944.0[1560.7, 2473.2]	119
i9	1053	4472.9	1880.1[1508.4, 2393.4]	138
i10	1118	4140.6	2089.9[1670.9, 2670.9]	98
i11	1250	4312.9	2327.0[1848.4, 2995.8]	85
i12	2323	19794.9	5334.1[4079.3, 7164.5]	271
i13	2561	21765.9	6196.9[4709.9, 8381.5]	251
i14	2691	16555.1	6301.2[4774.0, 8552.9]	163
i15	2746	20318.6	6460.6[4888.4, 8782.1]	214
i16	2871	31544.6	7032.4[5305.7, 9590.1]	349
i17	4934	38034.0	13299.2[9678.8, 18884.4]	186
i18	5459	43767.3	14831.2[10719.2, 21224.8]	195

TABLE IX

MEASURED TOTAL WIRELENGTH L_T OF THE SIX UNITS OF THE POWER4 CORE, AS WELL AS THE CORE, AND PREDICTED TOTAL WIRELENGTH L_{tot} (IN GATEPITCHES) FOR $\{k, p\}$, WHERE $L_{tot}(k,p) = \sum_{i=1}^{N_{macros}} N(A,p) \times L_{avg}(p)$ AND ERROR FOR ALL SIGNALS i IN EACH UNIT OF THE POWER4 CHIP, WHERE $N(A,p)$ IS THE PREDICTED NUMBER OF UNIT INTERCONNECTIONS. HERE WE TAKE $Error = \frac{(L_T - L_{tot}(k,p)) * 100}{L_{tot}(k,p)}\%$. THE ERROR IS SHOWN IN %. NOTE THAT L_T AND $L_{tot}(p)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

unit	N_{macros}	L_T	$L_{tot}(k,p)$ *[range]*	*Error*
ifu	18	226826.9	$73477.9[55477.2, 100315.0]$	209
fpu	12	21915.9	$12218.0[10508.0, 14423.0]$	79
fxu	4	26030.9	$27469.5[23706.5, 32248.9]$	-5
idu	18	148700.6	$740047.5[649463.2, 868919.1]$	-80
isu	16	309901.8	$1.3E6[1.1E6, 1.6E6]$	-76
lsu	32	553852.8	$1.1E6[906577.6, 1.4E6]$	-49
core	$6units$	1287230.0	$3.25E6[2.75E6, 4.01E6]$	-60

APPENDIX

This appendix contains tables with model estimates and actual data for the remaining five units in the POWER4 core: FPU, FXU, IDU, ISU, LSU. The first five tables show N_{gates}, N_{conn}, and $N(A, p)$ for these units. The second five tables show L_a, $L_{avg}(p)$, and $\overline{R}(p)$ (in units of gatepitches).

TABLE X

TOTAL NUMBER OF GATES N_{gates}, ACTUAL NUMBER OF INTERCONNECTIONS N_{conn}, PREDICTED NUMBER OF INTERCONNECTIONS $N(A,p)$ IN THE FPU, AND ERROR. HERE WE TAKE $Error = \frac{(N_{conn} - N(A,p)) * 100}{N(A,p)}\%$. THE ERROR IS SHOWN IN %.

design	N_{gates}	N_{conn}	$N(A,p)$ [range]	Error
f1	41	57	$37.6[20.9, 58.1]$	51
f2	46	68	$41.4[22.9, 64.3]$	64
f3	133	168	$147.5[79.0, 239.4]$	14
f4	201	246	$240.8[127.6, 397.2]$	2
f5	219	287	$251.7[133.0, 416.4]$	14
f6	236	302	$272.5[143.8, 452.1]$	11
f7	257	279	$322.4[169.8, 536.5]$	-13
f8	300	338	$368.4[193.3, 616.6]$	-8
f9	356	476	$414.2[216.5, 697.3]$	15
f10	398	486	$481.1[250.8, 812.9]$	1
f11	497	561	$616.9[320.1, 1050.2]$	-9
f12	555	593	$735.7[380.9, 1256.9]$	-19

TABLE XI

TOTAL NUMBER OF GATES N_{gates}, ACTUAL NUMBER OF INTERCONNECTIONS N_{conn}, PREDICTED NUMBER OF INTERCONNECTIONS $N(A,p)$ IN THE FXU, AND ERROR. HERE WE TAKE $Error = \frac{(N_{conn} - N(A,p)) * 100}{N(A,p)}\%$. THE ERROR IS SHOWN IN %.

design	N_{gates}	N_{conn}	$N(A,p)$ [range]	Error
x1	5	14	$5.1[3.8, 6.6]$	174
x2	33	49	$65.6[45.9, 89.9]$	-25
x3	304	398	$628.3[422.7, 904.0]$	-37
x4	2283	2269	$6350.7[4185.4, 9407.3]$	-64

TABLE XII

TOTAL NUMBER OF GATES N_{gates}, ACTUAL NUMBER OF INTERCONNECTIONS N_{conn}, PREDICTED NUMBER OF INTERCONNECTIONS $N(A,p)$ IN THE IDU, AND ERROR. HERE WE TAKE $Error = \frac{(N_{conn} - N(A,p)) * 100}{N(A,p)}\%$. THE ERROR IS SHOWN IN %.

design	N_{gates}	N_{conn}	$N(A,p)$[range]	Error
d1	86	120	$842.6[354.0, 1973.1]$	-86
d2	252	295	$3035.2[1263.7, 7207.7]$	-90
d3	513	665	$6437.9[2670.6, 15384.9]$	-90
d4	524	587	$7107.6[2948.1, 169878.0]$	-92
d5	585	658	$7468.2[3096.3, 17864.4]$	-91
d6	677	609	$8515.2[3528.4, 20389.2]$	-93
d7	755	788	$10116.7[4190.5, 24241.3]$	-92
d8	1238	1441	$16635.9[6880.8, 39974.6]$	-91
d9	1464	1610	$19986.1[8263.2, 48063.9]$	-92
d10	1497	1574	$20743.6[8575.9, 49890.7]$	-92
d11	1498	1703	$19841.7[8203.1, 47721.8]$	-91
d12	1500	1708	$19868.3[8214.1, 47786.1]$	-91
d13	1587	1807	$21025.6[8691.4, 50582.4]$	-91
d14	1697	1681	$23180.8[9580.9, 55784.0]$	-93
d15	2008	2330	$26626.5[11001.4, 64121.1]$	-91
d16	2082	2075	$28460.7[11758.5, 68548.1]$	-93
d17	2091	2086	$28584.2[11809.4, 68846.6]$	-93
d18	2685	2695	$36183.9[14942.7, 87232.1]$	-93

TABLE XIII

TOTAL NUMBER OF GATES N_{gates}, ACTUAL NUMBER OF INTERCONNECTIONS N_{conn}, PREDICTED NUMBER OF INTERCONNECTIONS $N(A,p)$ IN THE ISU, AND ERROR. HERE WE TAKE $Error = \frac{(N_{conn}-N(A,p))*100}{N(A,p)}\%$. THE ERROR IS SHOWN IN %.

design	N_{gates}	N_{conn}	$N(A,p)$ [range]	Error
s1	323	440	$4660.7[1572.5, 13602.3]$	-91
s2	331	353	$5005.1[1688.4, 14611.8]$	-93
s3	360	386	$5036.5[1698.1, 14717.7]$	-92
s4	656	912	$9383.7[3154.0, 27586.4]$	-90
s5	1188	1940	$17885.1[5998.5, 52821.9]$	-89
s6	1277	1306	$19528.0[6548.1, 57701.9]$	-93
s7	1299	1335	$19565.1[6560.2, 57818.0]$	-93
s8	1649	1732	$24863.7[8331.5, 73585.1]$	-93
s9	1719	1943	$24727.2[8284.9, 73198.6]$	-92
s10	1798	2104	$28371.6[9504.9, 84008.6]$	-93
s11	2347	2381	$36525.1[12229.3, 108304.6]$	-93
s12	2485	2837	$38679.8[12949.2, 114726.3]$	-93
s13	3207	3366	$50700.5[16965.6, 150556.9]$	-93
s14	3766	4083	$55182.3[18460.6, 163976.2]$	-93
s15	3962	4207	$63590.8[21271.9, 189000.4]$	-93
s16	6578	6831	$108744.6[36352.9, 323779.7]$	-94

TABLE XIV

TOTAL NUMBER OF GATES N_{gates}, ACTUAL NUMBER OF INTERCONNECTIONS N_{conn}, PREDICTED NUMBER OF INTERCONNECTIONS $N(A,p)$ IN THE LSU, AND ERROR. HERE WE TAKE $Error = \frac{(N_{conn}-N(A,p))*100}{N(A,p)}\%$. THE ERROR IS SHOWN IN %.

design	N_{gates}	N_{conn}	$N(A,p)$ *[range]*	*Error*
l1	117	118	$443.9[189.4, 1009.1]$	-73
l2	259	334	$1083.1[457.4, 2499.5]$	-69
l3	294	366	$1233.7[520.4, 2853.0]$	-70
l4	506	513	$2364.5[992.3, 5512.5]$	-78
l5	567	613	$2735.6[1147.0, 6387.6]$	-78
l6	641	728	$2917.0[1221.8, 6822.0]$	-75
l7	687	646	$3227.7[1351.3, 7555.3]$	-80
l8	1011	1021	$4632.3[1934.2, 10892.3]$	-78
l9	1024	954	$4692.6[1959.3, 11035.8]$	-80
l10	1191	1231	$5468.3[2281.1, 12880.8]$	-77
l11	1235	1279	$5672.7[2365.8, 13367.5]$	-77
l12	1392	1464	$6602.7[2751.9, 15578.0]$	-78
l13	1527	1635	$7360.1[3066.0, 17380.8]$	-78
l14	1655	1787	$7864.5[3274.8, 18586.2]$	-77
l15	1722	1715	$7938.0[3304.7, 18767.0]$	-78
l16	1835	1920	$8728.6[3632.8, 20648.2]$	-78
l17	1892	1869	$9002.3[3746.1, 21301.6]$	-79
l18	1920	2345	$8859.9[3686.6, 20967.5]$	-74
l19	1954	2111	$9018.3[3752.2, 21345.6]$	-77
l20	2241	2294	$10840.8[4507.7, 25690.1]$	-79
l21	2348	2017	$10684.4[4441.8, 25329.7]$	-81
l22	2353	2444	$11047.3[4592.6, 26190.4]$	-78
l23	2368	1995	$11118.3[4622.0, 26360.2]$	-82
l24	2516	2314	$11637.2[4836.4, 27604.3]$	-80
l25	2569	2475	$12255.7[5093.0, 29076.3]$	-80
l26	3398	3413	$16489.7[6845.0, 39207.3]$	-79
l27	3728	3900	$17832.0[7399.8, 42427.7]$	-78
l28	3866	3967	$19056.9[7907.1, 45353.9]$	-79
l29	4025	4338	$20721.2[8596.4, 49328.9]$	-79
l30	4622	4420	$21130.8[8762.4, 50352.2]$	-79
l31	4705	3799	$22260.6[9648.2, 55461.8]$	-84

TABLE XV

MEASURED AVERAGE WIRELENGTH FOR FPU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p)$) AND DONATH ($\overline{R}(p)$) ARE ALSO SHOWN. HERE WE TAKE $Error = \frac{(L_a - L_{avg}(p)) \times 100}{L_{avg}(p)}\%$ FOR $L_{avg}(p)$, AND $Error = \frac{(L_a - \overline{R}(p)) \times 100}{\overline{R}(p)}\%$ FOR $\overline{R}(p)$. THE ERROR IS SHOWN IN %. NOTE THAT L_a, $L_{avg}(p)$, AND $\overline{R}(p)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p)$ *[range]*	*Error*	$\overline{R}(p)$ *[range]*	*Error*
f1	41	3.0	2.1 [2.0, 2.3]	0.44	2.5 [2.3, 2.7]	21
f2	46	2.6	2.1 [2.0, 2.3]	0.19	2.6 [2.4, 2.8]	-1
f3	133	4.4	2.6 [2.3, 2.9]	0.69	3.3 [2.9, 3.8]	33
f4	201	5.1	2.8 [2.5, 3.2]	0.80	3.6 [3.1, 4.2]	40
f5	219	4.1	2.9 [2.5, 3.3]	0.45	3.7 [3.2, 4.3]	12
f6	236	4.6	2.9 [2.5, 3.4]	0.59	3.8 [3.2, 4.4]	23
f7	257	5.6	2.9 [2.6, 3.4]	0.91	3.8 [3.3, 4.5]	48
f8	300	5.0	3.0 [2.6, 3.6]	0.66	4.0 [3.3, 4.7]	27
f9	356	5.8	3.1 [2.7, 3.7]	0.84	4.1 [3.4, 4.9]	41
f10	398	6.9	3.2 [2.7, 3.8]	1.16	4.2 [3.5, 5.1]	64
f11	497	4.9	3.3 [2.8, 4.0]	0.47	4.4 [3.6, 5.4]	11
f12	555	7.1	3.4 [2.9, 4.1]	1.09	4.5 [3.7, 5.6]	58

TABLE XVI

MEASURED AVERAGE WIRELENGTH FOR FXU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p)$) AND DONATH ($\overline{R}(p)$) ARE ALSO SHOWN. HERE WE TAKE $Error = \frac{(L_a - L_{avg}(p)) \times 100}{L_{avg}(p)}\%$ FOR $L_{avg}(p)$, AND $Error = \frac{(L_a - \overline{R}(p)) \times 100}{\overline{R}(p)}\%$ FOR $\overline{R}(p)$. THE ERROR IS SHOWN IN %. NOTE THAT L_a, $L_{avg}(p)$, AND $\overline{R}(p)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p)$ *[range]*	*Error*	$\overline{R}(p)$ *[range]*	*Error*
x1	5	1.4	$1.4[1.4, 1.5]$	-0.05	$1.42[1.42, 1.43]$	-4.1
x2	33	4.3	$2.0[1.9, 2.1]$	1.17	$2.31[2.22, 2.41]$	85
x3	304	7.1	$2.9[2.6, 3.2]$	1.48	$3.71[3.33, 4.14]$	92
x4	2283	9.8	$4.0[3.5, 4.7]$	1.44	$5.39[4.48, 6.55]$	82

TABLE XVII

MEASURED AVERAGE WIRELENGTH FOR IDU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R)$) AND DONATH ($\overline{R}(p)$) ARE ALSO SHOWN. HERE WE TAKE $Error = \frac{(L_a - L_{avg}(p)) \times 100}{L_{avg}(p)}\%$ FOR $L_{avg}(p)$, AND $Error = \frac{(L_a - \overline{R}(p)) \times 100}{\overline{R}(p)}\%$ FOR $\overline{R}(p)$. THE ERROR IS SHOWN IN %. NOTE THAT L_a, $L_{avg}(p)$, AND $\overline{R}(p)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p)$ *[range]*	*Error*	$\overline{R}(p)$ *[range]*	*Error*
d1	86	2.2	$1.9[1.8, 2.1]$	0.17	$2.3[2.1, 2.5]$	-2
d2	252	4.1	$2.1[1.9, 2.3]$	0.93	$2.6[2.3, 2.9]$	60
d3	513	6.4	$2.2[2.0, 2.5]$	1.84	$2.7[2.4, 3.2]$	135
d4	524	5.5	$2.2[2.0, 2.6]$	1.44	$2.7[2.4, 3.2]$	103
d5	585	3.3	$2.3[2.0, 2.6]$	0.45	$2.7[2.4, 3.2]$	21
d6	677	4.5	$2.3[2.1, 2.6]$	0.94	$2.8[2.4, 3.3]$	61
d7	755	4.9	$2.3[2.1, 2.7]$	1.12	$2.8[2.4, 3.3]$	76
d8	1238	7.7	$2.4[2.1, 2.8]$	2.21	$2.9[2.5, 3.5]$	167
d9	1464	7.5	$2.4[2.1, 2.8]$	2.09	$2.9[2.5, 3.6]$	158
d10	1497	5.4	$2.4[2.1, 2.8]$	1.22	$2.9[2.5, 3.6]$	85
d11	1498	7.3	$2.4[2.1, 2.8]$	2.02	$2.9[2.5, 3.6]$	152
d12	1500	6.0	$2.4[2.1, 2.8]$	1.47	$2.9[2.5, 3.6]$	106
d13	1587	6.3	$2.4[2.1, 2.9]$	1.58	$2.9[2.5, 3.6]$	115
d14	1697	4.9	$2.4[2.1, 2.9]$	1.01	$2.9[2.5, 3.6]$	68
d15	2008	6.9	$2.5[2.2, 2.9]$	1.77	$3.0[2.5, 3.7]$	132
d16	2082	5.6	$2.5[2.2, 2.9]$	1.25	$3.0[2.5, 3.7]$	88
d17	2091	5.3	$2.5[2.2, 2.9]$	1.14	$3.0[2.5, 3.7]$	79
d18	2685	5.4	$2.5[2.2, 3.0]$	1.13	$3.0[2.5, 3.8]$	78

TABLE XVIII

MEASURED AVERAGE WIRELENGTH FOR ISU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R)$) AND DONATH ($\overline{R}(p)$) ARE ALSO SHOWN. HERE WE TAKE $Error = \frac{(L_a - L_{avg}(p)) \times 100}{L_{avg}(p)}\%$ FOR $L_{avg}(p)$, AND $Error = \frac{(L_a - \overline{R}(p)) \times 100}{\overline{R}(p)}\%$ FOR $\overline{R}(p)$. THE ERROR IS SHOWN IN %. NOTE THAT L_a, $L_{avg}(p)$, AND $\overline{R}(p)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p)$ *[range]*	*Error*	$\overline{R}(p)$ *[range]*	*Error*
s1	323	3.9	$2.2[2.0, 2.5]$	0.80	$2.6[2.3, 3.1]$	49
s2	331	5.8	$2.2[2.0, 2.5]$	1.65	$2.6[2.3, 3.1]$	119
s3	360	3.5	$2.2[2.0, 2.5]$	0.60	$2.7[2.3, 3.2]$	33
s4	656	4.9	$2.3[2.0, 2.7]$	1.10	$2.8[2.4, 3.4]$	74
s5	1188	7.9	$2.4[2.1, 2.9]$	2.27	$2.9[2.4, 3.7]$	171
s6	1277	5.8	$2.4[2.1, 2.9]$	1.37	$2.9[2.4, 3.7]$	97
s7	1299	7.1	$2.4[2.1, 2.9]$	1.91	$2.9[2.4, 3.7]$	142
s8	1649	5.7	$2.5[2.1, 3.0]$	1.30	$3.0[2.4, 3.8]$	91
s9	1719	8.0	$2.5[2.1, 3.0]$	2.23	$3.0[2.4, 3.8]$	169
s10	1798	7.3	$2.5[2.1, 3.0]$	1.92	$3.0[2.5, 3.8]$	143
s11	2347	6.8	$2.5[2.2, 3.1]$	1.68	$3.0[2.5, 4.0]$	124
s12	2485	8.0	$2.5[2.2, 3.1]$	2.16	$3.0[2.5, 4.0]$	164
s13	3207	9.1	$2.6[2.2, 3.2]$	2.51	$3.1[2.5, 4.1]$	194
s14	3766	4.2	$2.6[2.2, 3.3]$	0.62	$3.1[2.5, 4.2]$	35
s15	3962	11.1	$2.6[2.2, 3.3]$	3.26	$3.1[2.5, 4.2]$	257
s16	6578	12.9	$2.7[2.2, 3.5]$	3.80	$3.2[2.5, 4.4]$	305

TABLE XIX

MEASURED AVERAGE WIRELENGTH FOR IDU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R)$) AND DONATH ($\overline{R}(p)$) ARE ALSO SHOWN. HERE WE TAKE $Error = \frac{(L_a - L_{avg}(p)) \times 100}{L_{avg}(p)}\%$ FOR $L_{avg}(p)$, AND $Error = \frac{(L_a - \overline{R}(p)) \times 100}{\overline{R}(p)}\%$ FOR $\overline{R}(p)$. THE ERROR IS SHOWN IN %. NOTE THAT L_a, $L_{avg}(p)$, AND $\overline{R}(p)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p)$ *[range]*	*Error*	$\overline{R}(p)$ *[range]*	*Error*
l1	117	2.5	$2.2[2.0, 2.4]$	0.12	$2.7[2.4, 3.0]$	-9
l2	259	7.1	$2.4[2.2, 2.7]$	1.95	$3.0[2.7, 3.5]$	136
l3	294	7.0	$2.5[2.2, 2.8]$	1.85	$3.1[2.7, 3.6]$	128
l4	506	5.9	$2.6[2.3, 3.0]$	1.26	$3.3[2.8, 3.9]$	79
l5	567	6.0	$2.7[2.4, 3.1]$	1.25	$3.4[2.9, 4.0]$	79
l6	641	5.9	$2.7[2.4, 3.1]$	1.19	$3.4[2.9, 4.1]$	73
l7	687	5.9	$2.7[2.4, 3.2]$	1.17	$3.4[2.9, 4.1]$	72
l8	1011	5.2	$2.9[2.5, 3.4]$	0.81	$3.6[3.0, 4.4]$	43
l9	1024	5.4	$2.9[2.5, 3.4]$	0.89	$3.6[3.0, 4.4]$	50
l10	1191	5.4	$2.9[2.5, 3.5]$	0.86	$3.7[3.0, 4.6]$	47
l11	1235	5.5	$2.9[2.5, 3.5]$	0.90	$3.7[3.0, 4.6]$	50
l12	1392	5.9	$3.0[2.5, 3.5]$	1.01	$3.7[3.1, 4.7]$	59
l13	1527	6.0	$3.0[2.5, 3.6]$	0.99	$3.8[3.1, 4.7]$	58
l14	1655	6.8	$3.0[2.6, 3.6]$	1.26	$3.8[3.1, 4.8]$	78
l15	1722	10.0	$3.0[2.6, 3.7]$	2.30	$3.8[3.1, 4.8]$	160
l16	1835	7.1	$3.0[2.6, 3.7]$	1.34	$3.9[3.1, 4.9]$	85
l17	1892	9.4	$3.1[2.6, 3.7]$	2.08	$3.9[3.1, 4.9]$	143
l18	1920	10.1	$3.1[2.6, 3.7]$	2.30	$3.9[3.1, 4.9]$	161
l19	1954	9.0	$3.1[2.6, 3.7]$	1.92	$3.9[3.1, 4.9]$	131
l20	2241	4.6	$3.1[2.6, 3.8]$	0.49	$3.9[3.2, 5.1]$	18
l21	2348	8.3	$3.1[2.6, 3.8]$	1.65	$4.0[3.2, 5.1]$	109
l22	2353	10.9	$3.1[2.6, 3.8]$	2.49	$4.0[3.2, 5.1]$	176
l23	2368	5.5	$3.1[2.6, 3.8]$	0.76	$4.0[3.2, 5.1]$	39
l24	2516	8.0	$3.1[2.6, 3.9]$	1.55	$4.0[3.2, 5.1]$	102
l25	2569	6.9	$3.2[2.6, 3.9]$	1.19	$4.0[3.2, 5.2]$	73
l26	3398	7.3	$3.2[2.7, 4.1]$	1.25	$4.1[3.3, 5.4]$	78
l27	3728	8.8	$3.3[2.7, 4.1]$	1.68	$4.2[3.3, 5.5]$	112
l28	3866	9.3	$3.3[2.7, 4.1]$	1.82	$4.2[3.3, 5.5]$	123
l29	4035	11.0	$3.3[2.7, 4.2]$	2.58	$4.2[3.3, 5.5]$	162

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