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Interpretation of Rent's Rule for Ultralarge-scale Integrated Circuit Designs, with Application to Wire-length Distribution Models

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Abstract

Computer hardware components have changed significantly since the 1960's, 1970's, 1980's, and even since the early 1990's. All work concerning Rent's Rule prior to the present paper has been based on a 1971 interpretation of two unpublished memoranda written in 1960 by E. F. Rent at IBM, even though today's computer components are significantly different from those in 1960 and 1971. However, because of the significant changes in design and implementation of computer hardware components since 1960-1971, a new interpretation of Rent's Rule is needed for today's components. We have obtained copies of Rent's two memos; in these 1960 memos, E. F. Rent describes the method that he used to deduce an empirical relationship between properties of IBM 1401 and 1410 computer hardware components. We have studied these memos carefully in order to understand Rent's original intent. Based on our careful reading of these two memos, the personal knowledge of one of us (R. Rand) with the 1401 and 1410 computers, and our experience with ULSI circuit design for high-performance microprocessors, we have derived an historically-equivalent interpretation of Rent's Rule suitable for today's computer components. The purpose of this paper is to present this new interpretation of Rent's Rule and its application to wirelength distributions of ultralarge-scale integrated (ULSI) circuits. In this paper, we will: (1) describe the contents of the memos and Rent's method, (2) provide an historically-equivalent interpretation of Rent's Rule for today's computer components, and (3) apply this new interpretation to actual ULSI circuit designs. In this paper, we will show that this new interpretation provides improved wirelength distribution models with better qualitative agreement and more accurate estimates of wirelength distributions and wirelength requirements in ULSI designs compared with prior methods.

Index Terms

ULSI, VLSI, circuit, design, Rent's Rule, wirelength distribution, average wirelength.

I. INTRODUCTION

Because of significant changes in the design and implementation of computer hardware components since the 1960's, 1970's, 1980's and even since the 1990's[1], [2], a new interpretation of empirical rules such as Rent's Rule - described by E.F. Rent in 1960[3] and first interpreted in 1971[4] - is needed for today's computer components. All of the prior extensive work concerning Rent's Rule, including for example Refs.[5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], has been based on the 1971 interpretation of two unpublished memoranda written in 1960 by E. F. Rent at IBM, even though today's computer components differ significantly from those in 1960-1971. Since significant differences exist between the

components discussed in Rent's original work and today's computer components, a new interpretation of Rent's Rule that is suitable for ultralarge-scale integrated (ULSI) designs is therefore required.

We have obtained copies of both of E. F. Rent's IBM memoranda[3] dated November 28, 1960 and December 12, 1960, and we have studied these memos in order to understand the method that E. F. Rent employed to analyze characteristics of the IBM 1401 and 1410 computers. In these memos, Rent describes the method that he used to deduce an empirical relationship between properties of computer hardware components of these computers. Based on our careful reading of these two memos, the personal knowledge of one of us (R. Rand) with the 1401 and 1410 computers, and our experience designing and wiring ULSI circuits for high-performance microprocessors, we have derived an historically-equivalent interpretation of Rent's Rule suitable for today's computer components.

In this paper, we present an historically-equivalent interpretation of Rent's Rule suitable for today's ULSI circuit designs. The contributions of this paper are: (1) a description of the contents of the two memoranda and Rent's method; (2) an historically-equivalent interpretation of Rent's Rule suitable for today's computer components; and (3) application of this interpretation to actual ULSI microprocessor chip designs. The first application will be to extract historically-equivalent empirical values of Rent's parameters for these designs. The second application will be to evaluate existing wirelength distribution models and existing expressions for average wirelength as functions of these new empirical parameters. We will then compare these distributions and average wirelength values with actual distributions and average wirelengths observed on actual chip designs. The designs selected for this study are all (100) of the functional control designs in the IBM POWER4 core, which is currently incorporated in the IBM Enterprise Server pSeries 680 and pSeries 690.[21], [22] The control designs occupy approximately 50% of the core area.[22]

We will show that this comparison shows improved qualitative agreement between the measured and estimated wirelength distributions and average wirelengths, compared with prior work, such as Refs.[6], [7], [20], where differences are seen when the previous (1971) interpretation of Rent's Rule is used. We observe that the distributions and average wirelength estimates obtained with existing models[11], [12], [14] are in fact improved when they are evaluated as

functions of the new empirical parameters derived based on the new historically-equivalent interpretation of Rent's memos. This new method provides designers with a technique to evaluate the amount and distribution of wire required to interconnect components in ULSI systems in order to achieve buildable and functional chip designs within increasingly severe project constraints of real estate, number of metal layers, operating frequency, and power dissipation[9], [10], [16], [18], [23], [24], [25].

II. Computer Hardware Components

To illustrate the significant changes in the design and implementation of computer hardware components since the 1950's, we have compiled a list of technical hardware innovations in IBM computers in the past several decades. This information is provided in Table I. For each decade since the 1950's, technical innovations in the physical design and implementation of computer hardware components have provided new generations of IBM computers listed in the third column of the table.

In this section, we summarize briefly the types of computer hardware components. A thorough description of IBM computers is available in Ref. [1] and elsewhere [2]. Throughout much of the 1950's, a key component of IBM computers was the banana-sized cathode-ray vacuum tube, and as a result, a single central processing unit (CPU) composed of many of these tubes occupied 5ft x 3ft x 6ft of floor space. By 1959-1960, vacuum tube technology was superseded by the introduction of discrete transistors in the 1401 and 1410 computers, which are the computers Rent discusses in his two memos. In 1964, discrete transistor technology was replaced by hybrid solid logic technology consisting of semiconductor chips, printed wires, and printed resistors in the System/360 computer. In 1985, IBM introduced its first mainframe with memory chips containing 1 million bits each. In 1990, each memory chip in the RISC System/6000 contained 4 million bits. In 2001, the POWER4 chip in the IBM Enterprise Server pSeries 680 and 690 contained two CPUs, 174 million transistors, and more than one mile of copper wiring on a penny-sized $4cm^2$ silicon chip[21], [22], for a significant volume reduction compared with the early 1950's CPU.

III. E. F. RENT'S TWO MEMORANDA

In this section, we describe our approach toward understanding the two memoranda written by E. F. Rent and dated November 28, 1960 and December 12, 1960. We will describe Rent's memoranda and the method that Rent used to analyze components of the 1410 and 1401, two computers introduced by IBM in 1959-1960. The 1410 computer was an IBM IO processor that read in punch cards and output computing results

Components of 1410 and 1401 computer hardware discussed by Rent in his memos are: the computer *chassis*, *card*, *circuit count*, and *edge connector count*. The computer chassis contains several cards that are connected together in the chassis. Each card is composed of one or more circuits; the circuits on the card can either be used or unused; used circuits are connected to used circuits on other cards within the chassis with the use of edge connectors. A circuit is also referred to as a *logic block*. Figure 1 shows a schematic depiction prepared by the present authors of the computer components described in E. F. Rent's two memos. This figure shows (a) a schematic of a design, including a computer chassis and cards (e.g., card A), and (b) a card, circuit, edge connectors, used circuit, and unused circuit.

In the first memo, Rent describes his method to obtain the *circuit count* and *edge connector count* of the cards on each chassis:

(1) circuit count: *"the circuit count was made by card type and then a count of one given for each of the following: 2 way logic block, 3 way logic block, emitter follower, indicator follower, indicator driver, power inverter, line driver, etc. No count was made for diode clamp or resistor load cards. All unused circuits on cards were removed from the count to give an actual logic circuit count for each chassis,"* [3] and

(2) edge connector count: *"the net edge connector count required a total for all edge connectors on a chassis less, (1) those connectors that were used to feed signals across a chassis and not go to any logic on the chassis and (2) those connectors that were used to distribute to the adjacent chassis signals that were developed on the chassis."* [3]

Rent plotted the circuit count per card as a function of the number of edge connectors per card on log-log graph paper in each memo. Rent also calculated the average block to edge connector ratio and wrote in the memorandum that *"the average of the three control chassis will be considered as more typical of all chassis and will be used as the reference point in further*

discussions." [3] In the first memo, the ordinate is labelled *"logic blocks/card"*, and the abscissa is labelled *"signal pins/card."* Each plot contains several data points drawn by hand, where the data points are the number of logic blocks and number of edge connectors obtained with the descriptions provided in italics above. A line is drawn by hand through several data points in these plots; our inspection of this line indicates that it may be described by the expression,

$$y = m \times x + b, \tag{1}$$

where we obtain $m = 1.49$, $b = -0.94$ for the line on the plot. This expression may be inverted (that is, ordinate and abscissa interchanged) to display the signal pins per card as a function of the logic blocks per card, to take the form,

$$x = m' \times y + b', \tag{2}$$

where $m' = 0.67$ and $b' = 0.63$. Figure 1(c) shows a schematic illustration of the method for plotting log-log plots to obtain Rent's parameters.

IV. Historically-equivalent interpretation of Rent's memoranda for today's ULSI computer components

In this section, we derive an interpretation of Rent's Rule suitable for use with today's ULSI computer components based on the information described in Rent's memoranda, as presented in the previous section.

We first prepare a schematic of ULSI circuits used in today's computer components in a manner that is historically-equivalent to that described by Rent. In today's designs, the historically-equivalent term for *circuit count* is *gate count*, or the number of gates in a design; the historically-equivalent term for *edge connector count* is *used connections*, or the number of used connections in a design. Figure 2 shows a schematic that can be used to obtain an historically-accurate interpretation of the circuit count and edge connector count. The figure shows: (a) a schematic of current designs with designs containing logic gates, (b) circuitry with used gates and unused gates and connections on the gates, and (c) a method for calculating historically-equivalent Rent's parameters to which we will refer with terms k_R and p_R, where the subscript R refers to *Rent*.

Historically-equivalent expressions for the *gate count* and *used connections* are obtained by following the method described by Rent and applying them to today's computer components. In this paper, we will use the terms N_{gates} to refer to the *number of gates*, and N_{conn} to refer to the number of *used connections*.

First, as an historically-equivalent expression for the *circuit count* in today's computer components, we introduce the expression for *gate count*, or N_{gates}, given by,

$$N_{gates} = N_{all} - N_{unconnected} - N_{spare} - N_{filler} - N_{decap}, \tag{3}$$

where the term N_{all} refers to the total number of gates in a design, $N_{unconnected}$ refers to the number of unconnected gates, N_{spare} refers to the number of gates associated with spare logic, N_{filler} refers the number of filler cells, and N_{decap} refers to the number of decoupling capacitors. To obtain an accurate count of N_{gates}, we note that it is important to itemize carefully all contributions to the four terms: $N_{unconnected}$, N_{spare}, N_{filler}, and N_{decap}, since these terms do not contribute to the number of functional gates in a design, although they may for various reasons exist in different design specifications; for example, $N_{unconnected}$ can result from logic bug fixes, and N_{spare} can be included in anticipation of future logic bugs.

Second, as an historically-equivalent expression for the *edge connector count* in today's computer components, we introduce the expression for *used connections*, or N_{conn}, given by,

$$N_{conn} = \sum_{i=1}^{N_{nets}} (F_i + 1) - N_{IO}, \tag{4}$$

where the sum is taken over all signal nets N_{nets}, F_i is the fanout of each signal net, and N_{IO} is the number of input pins and output pins in the design. In Eqn. 4, the term $(F_i + 1)$ represents the total number of connections made by a single signal net in a design; each signal net has a single driver and can have fanout $F_i \geq 1$. The total number of connections of all signal nets is obtained by taking the sum of this term $(F_i + 1)$ over all signal nets in the design. The number of input/output pins N_{IO} is subtracted from the right-hand-side of Eqn. 4 in order to follow Rent's method in an historically-equivalent manner since Rent also subtracted this contribution. Since the total fanout F_{total} can be written as $F_{total} = \sum_{i=1}^{N_{nets}} F_i$, Eqn. 4 can be rewritten according to the expression,

$$N_{conn} = F_{total} + N_{nets} - N_{IO}. \tag{5}$$

Figure 2(c) shows an example of a log-log plot of the total number of connections as a function of the number of used gates.

Figure 3 shows an example of a schematic and associated calculations to obtain the quantities N_{gates} and N_{conn} from a design such as Design A shown in Fig. 2. In this figure, the used signals are labelled $\{s1, ..., s9\}$, and the used gates are labelled $\{g1, ..., g4\}$. The quantities N_{gates} and N_{conn} are obtained from Eqns. 3- 5. An example of an explicit calculation for Design A is shown in Fig. 3(c), where $N_{gates} = 4$, $F_{total} = 10$, $N_{nets} = 9$, and $N_{IO} = 7$. From these values, we obtain $N_{conn} = 12$ which can be verified by inspection in Fig. 3(a).

We now introduce the terms k_R and p_R to refer to Rent's parameters that can be obtained with our interpretation of Rent's memos and a log-log plot of N_{conn} as a function of N_{gates}. The parameters k_R and p_R represent the inverse log of the intercept and slope, respectively, of a linear fit to the quantities in the log-log plot shown in Fig. 1(c), according to the expression,

$$Log(N_{conn}) = Log(k_R) + p_R \times Log(N_{gates}). \tag{6}$$

We will use the expressions in Eqns. 3- 6 to extract values of the parameters $\{k_R, p_R\}$ from chip design data. For comparison, in the rest of this paper, the terms k and p are used to refer to Rent's parameters obtained based on the 1971 interpretation of Rent's memos, in which k and p are obtained from log-log plots of N_{IO} as a function of N_{gates}. [4], [11], [12].

V. Application to wirelength distribution models

In this section, we will apply the historically-equivalent interpretation of Rent's memos of the previous section to wirelength distribution models [6], [7], [11]. We wish to determine if estimates of wirelength requirements obtained by evaluating the existing models as functions of the historically-equivalent Rent's parameters $\{k_R, p_R\}$ will more closely approximate actual wirelength requirements of control designs in the POWER4 core. For this comparison, we choose the Donath (1979) and Davis (1998) models [6], [11], [12], [14]. The interconnection density function provided by the Davis model exhibited curvature that most closely approximated the curvature of the actual wirelength distribution described in Ref. [20] compared with two other models [6], [7]. In this section, we will evaluate models for the normalized probability density function $p_{int}(L)$, probability density function $P(L)$, and average wirelength $L_{avg}(p_R)$.

The first step is to extract the model parameter pair $\{k_R, p_R\}$ from the POWER4 chip design data. In this case, the number of used connections N_{conn} and number of used gates N_{gates} are counted in each of the 100 designs; Figure 4(b) shows a log-log plot of N_{conn} as a function of N_{gates} for the six units in the POWER4 core. Linear fits to the design data to Eqn. 6 allows us to extract the parameter pair $\{k_R, p_R\}$ as well as the range of k_R and p_R for each unit, as summarized in Table II. This table shows that $k_R \sim 1 - 4$, with range $1.24 \leq k_R \leq 3.82$, and that $p_R \sim 1$, with range $0.95 \leq p_R \leq 1.12$. By comparison, Fig. 4(a) shows a prior method to extract $\{k, p\}$ parameter pairs from designs with the method of Davis [11]; in this figure, the number of input/output pins N_{IO} as a function of used gates N_{gates} for six units in POWER4 chip, to obtain parameters k and p values summarized in Ref. [20].

The next step is to evaluate these models as functions of k_R and p_R to obtain estimates and ranges for $N(A_R, p_R)$, average wirelength $L_{avg}(p_R)$ and $\overline{R}(p_R)$, and total wirelength shown in Tables III- V, respectively. Table III shows that $N(A_R, p_R)$ underestimates N_{conn} for all designs except for the largest by up to 204%; however the values of $N(A_R, p_R)$ tend to underestimate less than the estimates obtained with $N(A, p)$, and for several of the largest designs (i.e., designs with $N_{gates} \geq 1250$, the estimates with $N(A_R, p_R)$ are improved, to within 27% of the values of N_{conn}. The average fanout f is $1.6 \leq f \leq 2.3$ for this group of signals as shown in Table III.

Table IV shows a comparison of the actual wirelength of each control design in the POWER4 Instruction Fetch Unit (IFU) with average wirelength estimates obtained with the Davis model ($L_{avg}(p_R)$) and Donath model ($\overline{R}(p_R)$). These tend to overestimate the average wirelength; This table shows that the value of $L_{avg}(p_R)$ tends more closely approximate the measured value of L_a compared with the value of $\overline{R}(p_R)$, particularly for large designs with $N_{gates} \geq 2323$ where the estimates are within approximately 20% of the actual values. Table V shows a comparison of estimates of the total wirelength requirement with the actual total wirelength L_T in each design; the values tend to more closely estimate the actual values, with Error less than 84% for all designs except for the two smallest designs with least gates $N_{gates} \leq 220$. In this case, we take the Error to be given by the expression, $Error = \frac{(L_T - L_{avg}(p_R) \times N(A_R, p_R)) \times 100}{L_{avg}(p_R) \times N(A_R, p_R)}$; the Errors are shown in $\%$. Table VI compares the total measured wirelength L_T in each unit with the estimated total wirelength $L_{tot}(p_R)$ given by the expression,

$$L_{tot}(p_R) = \sum_{i=1}^{N_{macros}} N(A_R, p_R) \times L_{avg}(p_R). \quad (7)$$

This table shows that the estimates $L_{tot}(p_R)$ are within 40% of the actual values for all units and are within 9% of L_T of one of the units (the IFU). Moreover, the estimate of total wirelength requirements for all control designs in the POWER4 core is within 23% of the actual wire requirements, which is improved compared with the previous method. [20]

Next, we evaluate the interconnection density function of the Davis (1998) model as functions of parameter pairs $\{k, p\}$ and $\{k_R, p_R\}$ and compare the distributions obtained with these models with measured interconnection density functions of POWER4 control designs. Figure 5 shows the normalized probability density function $p_{int}(L)$ (solid circles) and probability density function $P(L)$ (hollow squares) for four designs in the POWER4 IFU. We chose the normalized probability density functions rather than the probability density functions for this comparison because the expression for the total number of interconnections predicted by Donath (1979) [6] takes on nonphysical values for $p \geq 1$, since $N(A, p)$ becomes negative for $p > 1$, and $N(A, p) = 0$ when $p = 0$. Since $N(A, p) > 1$ for several of the units in the POWER4 core, we have evaluated the normalized distribution functions provided by Davis [11], [12], [14]; these functions are independent of $N(A, p)$. Figure 5 shows examples of these normalized distribution functions for four designs: (a) design7, (b) design1, (c) design2, and (d) design18. For all macros, the gatepitch is taken to be the book height of the logic books in each design. The dotted line indicates the curve obtained for $p_{int}(L)$ and $P(L)$ from the Davis model with the parameter pair $\{k, p\}$ [20], and the solid line indicates the curve obtained with the Davis model with parameter pair $\{k_R, p_R\}$. Of these two distributions, the curve obtained with the use of the historically-equivalent Rent parameter pair $\{k_R, p_R\}$ is a qualitatively better fit to the actual distribution compared with the the curve obtained with parameter pair $\{k, p\}$. Moreover, the former curve more closely approximates the form of the normalized probability density function in actual designs, particularly at smaller values of wirelength L.

VI. Discussion

In the previous section, we have seen that the application of the two historically-equivalent Rent's parameters $\{k_R, p_R\}$ to existing wirelength distribution models shows that the estimates and distributions obtained with these models are greatly improved compared with existing methods in which the 1971 interpretation of Rent's rule is used. For example, evaluation of expressions provided by the Davis model as a function of $\{k_R, p_R\}$ shows that the total wirelength

estimates are within 4% to 48% of the actual total wirelength values for designs containing more than 779 logic gates; these estimates are more accurate than those obtained with the 1971 interpretation of Rent's rule, with which total wirelength estimates differ from the actual values for most designs by more than 100% and as much as 400%, as described in Ref. [20]. As another example, wirelength distribution functions provided by the Davis model as functions of $\{k_R, p_R\}$ have greatly improved qualitative agreement in their distribution curve and ranges (upper and lower bound curves) compared with actual wirelength distributions, particularly compared with three existing wirelength distributions (Donath 1979, Donath 1981 and Davis 1998) that exhibit larger spread and poorer qualitative agreement with the 1971 interpretation of Rent's rule. [20]

We now speculate on possible factors that one might explore to further improve the agreement of wirelength distribution estimates with measurements obtained from actual chip design data. Now that we have introduced a new historically-accurate interpretation of Rent's Rule, and have applied this interpretation to existing models as described in the previous section, we note that existing models have been derived for circuit designs with simplifications such as tiled arrays of square logic gates with unity-fanout nets. By comparison, actual chips such as the one described in the comparison provided in this paper, have physical designs that demonstrate additional characteristics, such as:

(1) actual chips contain non-square gates;

(2) actual chips tend to contain many signals with greater-than-unity fanout nets;

(3) actual chips contain logic gates and signals that are not associated with the logical function of the design; these gates include, for example, gates associated with clocking circuitry.

In particular, regarding (1), the gates in the ULSI designs considered in the POWER4 core do have uniform height (albeit varying widths). Regarding (2), most nets in the POWER4 do have fanout less than three. Regarding (3), some examples of signals associated with clocking circuitry include the clock control signals and scan signals; signals associated with clocking circuitry tend to have fanout much greater than unity. Modifying existing models to account for these three factors in future work may help further improve the agreement of estimates obtained with existing models compared with actual wirelength distributions.

VII. Conclusion

In this paper, we have presented a new historically-equivalent interpretation of Rent's Rule suitable for today's computer hardware components. This work has been motivated by the need for a new interpretation of Rent's Rule, since computer components have changed significantly compared with the components described in Rent's original work. For the work described in this paper, we have obtained copies of Rent's two memos in which Rent describes a method to deduce empirical relationships between properties of 1960 computer hardware components. Based on our careful study of these memos, the personal knowledge of one of us (R. Rand) with the 1401 and 1410 computers described in these memos, and our experience with $ULSI$ designs for high-performance microprocessors, we have derived an historically-equivalent interpretation of Rent's Rule suitable for use with today's computer components. In addition, we have applied this new interpretation to actual ultralarge-scale integrated (ULSI) circuit designs in the POWER4 core, and we have shown that evaluating existing wirelength distribution models and average wirelength models with this new interpretation provides improved qualitative agreement and more accurate estimates of actual chip wirelength requirements compared with prior methods. Additional potential applications include use of the historically-equivalent Rent parameters in computer system design. [10]

VIII. Acknowledgments

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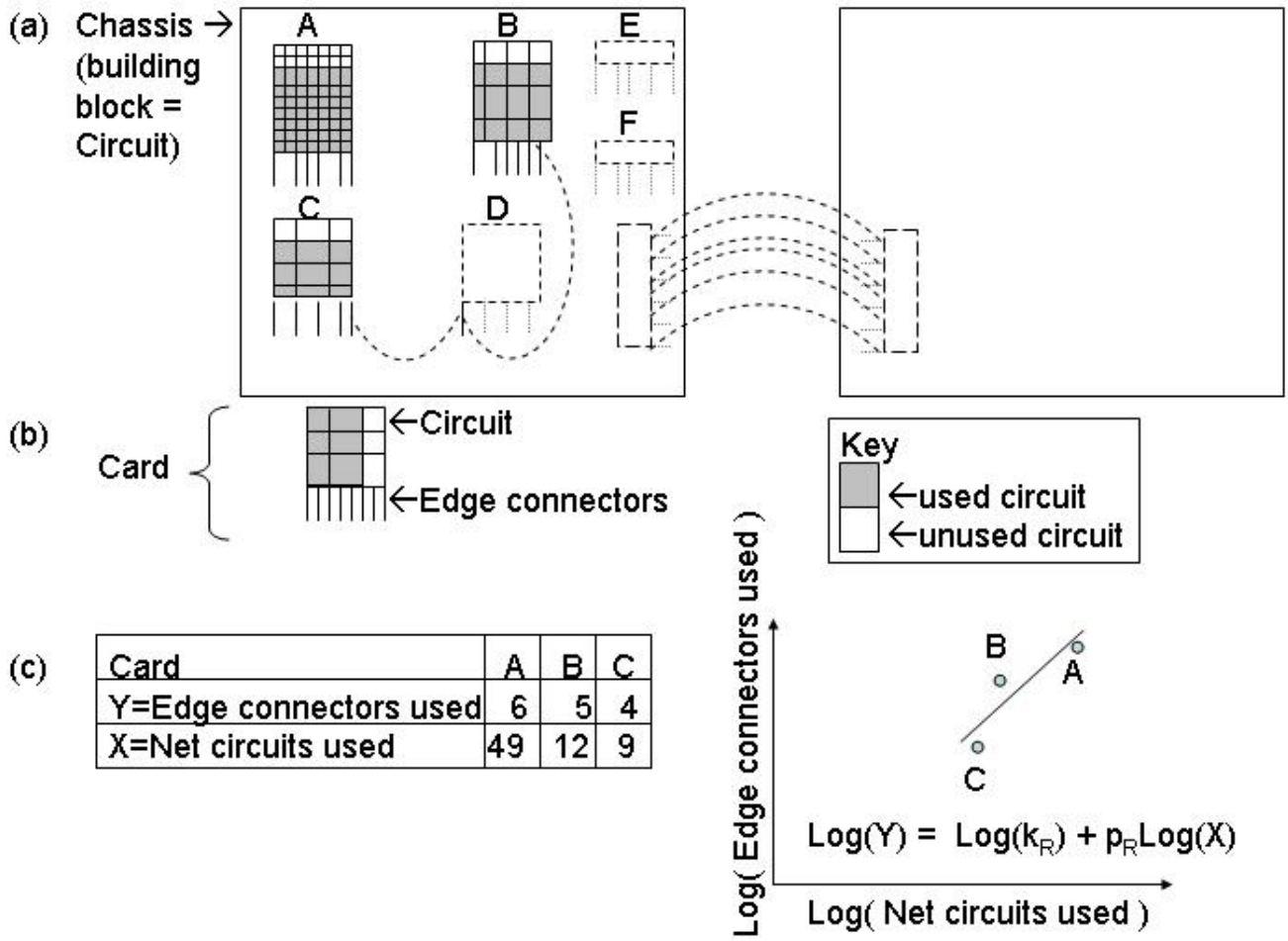
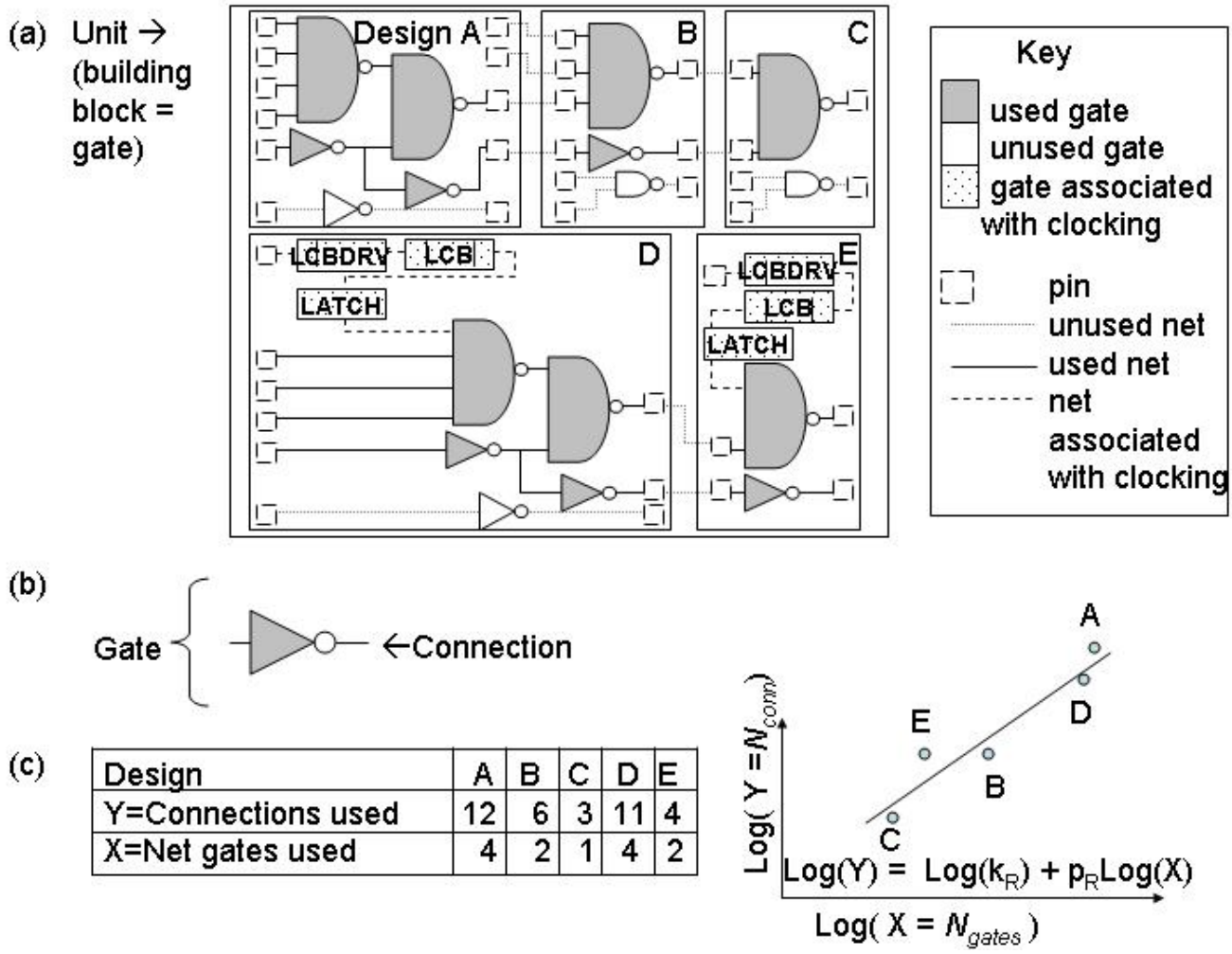


Card	A	B	C
Y=Edge connectors used	6	5	4
X=Net circuits used	49	12	9

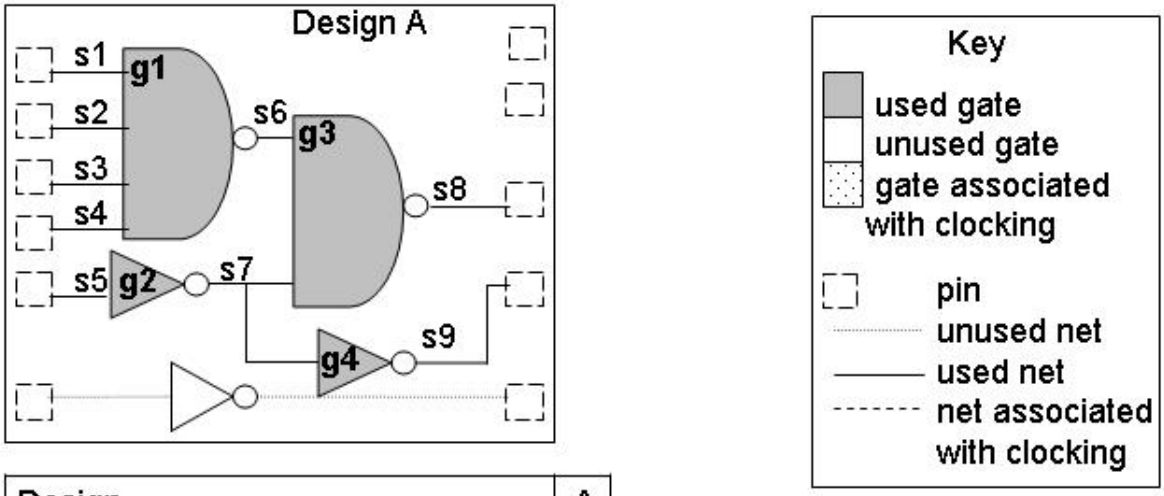
Fig. 1. (a) Visual depiction of Rent's rule based on interpretation of Rent's two 1960 memos. (b) Schematic of design, including gates and (c) a method for calculating k_R and p_R. In (a), the shaded small squares in cards A-C represent used circuits, the white squares represent unused circuits, the solid lines pointing downward below cards A-C represent used edge connectors, the dashed squares in D-F represent unused cards, the dashed solid lines represent unused edge connectors, and the dashed curved lines between the two chassis represent that these connections are not included in Rent's calculation.



Design	A	B	C	D	E
Y=Connections used	12	6	3	11	4
X=Net gates used	4	2	1	4	2

Fig. 2. Visual depiction of the historically-equivalent interpretation of Rent's rule for ULSI circuit designs. (a) shows a schematic of several current designs, including (b) clocking circuitry with gates and (c) calculation of k_R and p_R are shown. In (a), the shaded gates represent used gates, or gates used in the functional logic of the design; the white gates represent unused gates, or gates that are not used to implement the functional logic of the design; and speckled gates represent gates that are associated with clocking circuitry. The dashed white squares represent IO pins, the dotted lines represent unused nets, the solid lines represent used nets, and the dashed lines represent nets that are associated with clocking circuitry.

(a)



(b)

Design	A
Y=Connections used (N_{conn})	12
X=Net gates used (N_{gates})	4

(c)

$$N_{gates} = \sum_{i=1}^{4} 1 = 4$$

$$N_{conn} = F_{total} + N_{nets} - N_{IO} = 10 + 9 - 7 = 12$$

$$F_{total} = \sum_{i=1}^{N=9} F_{si} = F_{s1} + F_{s2} + F_{s3} + F_{s4} + F_{s5} + F_{s6} + F_{s7} + F_{s8} + F_{s9} = 1+1+1+1+1+1+2+1+1 = 10$$

$$N_{nets} = \sum_{i=1}^{N=9} 1 = 9$$

$$N_{IO} = \sum_{i=1}^{5} 1 + \sum_{i=8}^{9} 1 = 7$$

Fig. 3. An example of calculations to obtain N_{conn} and N_{gates} from a design such as Design A shown in (a), where the used signals are labelled $\{s1, ..., s9\}$ and the used gates are labelled $\{g1, ..., g4\}$. N_{gates} is obtained by taking a sum over all used gates. N_{conn} is obtained from the expression $N_{conn} = F_{total} + N_{nets} - N_{IO}$, where F_{total} is the total fanout of all used nets, N_{nets} is the number of used nets, and N_{IO} is the number of used IO pins in the design. An example of an explicit calculation for Design A is shown in (c), where $F_{total} = 10$, $N_{nets} = 9$, and $N_{IO} = 7$.

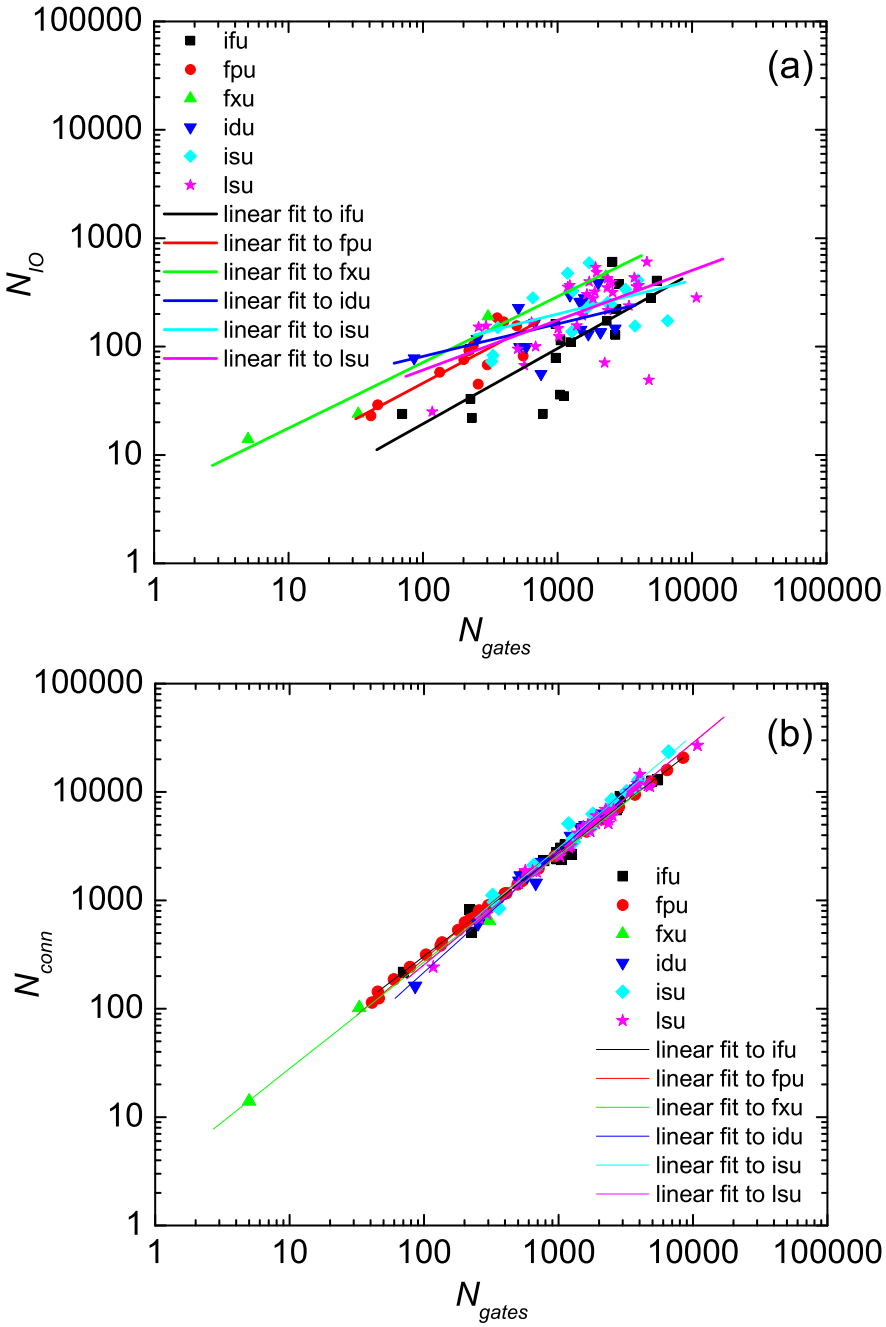


Fig. 4. (a) The number of input/output pins N_{IO} as a function of used gates N_{gates} for six units in POWER4 chip, to obtain parameters k and p values summarized in Ref. [20] with prior method to extract $\{k, p\}$ parameter pairs from designs (see for example, Davis [11]). (b) New method to extract Rent's parameter pair presented in this paper. The number of used connections N_{conn} is shown in (b) as a function of used gates N_{gates} for six units in POWER4 chip, according to the historically-equivalent interpretation of Rent's memos for ULSI circuit designs presented in this paper. This method is used to extract the Rent's parameters k_R and p_R listed in Table II.

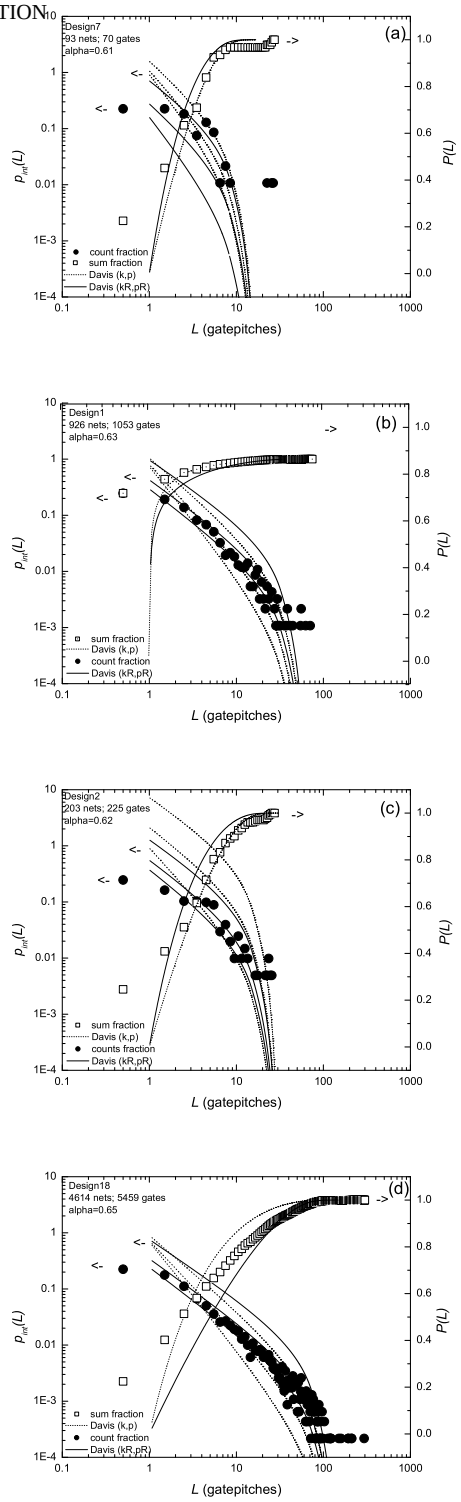


Fig. 5. Normalized probability density function $p_{int}(L)$ (solid circles) and probability density function $P(L)$ (hollow squares) for (a) design7, (b) design1, (c) design2, and (d) design18 in POWER4 Instruction Fetch Unit. For all macros, the gatepitch is taken to be the book height d of the standard cells. The dotted line represents the distribution obtained for $p_{int}(L)$ and $P(L)$ by evaluating expressions provided by the Davis model as functions of previous Rent's parameter pair $\{k, p\}$ from Ref. 1. The solid lines represent the distributions obtained with the Davis model and new parameter pair $\{k_R, p_R\}$ obtained with the method described in this paper and listed in Table II.

TABLE I

TYPICAL HARDWARE COMPONENTS IN IBM COMPUTERS SINCE 1952. THE SMS CARD REFERS TO IBM'S PROPRIETARY STANDARD MODULAR SYSTEM OF CIRCUIT PACKAGING. THE TERM SLT REFERS TO IBM'S SOLID LOGIC TECHNOLOGY.

Date[1]	*Technology[1]*	*IBM System*[1]
1952	*cathode-ray vacuum tubes, magnetic drum and tape storage, card reader/punch*	*701*
1954	*5ft x 3ft x 6ft CPU, rotating magnetic drum, card reader/punch, magnetic core memory*	*650*
1959	*SMS circuit packaging technology: discrete transistors, resistors, jumper wires on* $2.5in \times 2.5in$ *circuit cards punched cards; magnetic tape.*	*1401*
1959	*SMS circuit packaging technology*	*7090*
1960	*SMS circuit packaging technology*	*1410*
1964	*SLT hybrid solid logic technology, with 1.6 sq. in. printed circuit boards; cards with semiconductor chips, printed lines and resistors; ferrite-core memories*	*System/360*
1968	*monolithic integrated circuits with 1-4 circuits/silicon chip; 4 chips/ceramic module*	*System/360 Model 85*
1970	*monolithic systems technology; all-semiconductor main memory*	*System/370 Model 145*
1980	*thermal conduction module with > 100 chips*	*3081*
1985	*1st mainframe with 1-million-bit memory chips*	*3090*
1990	*VLSI: 4-million-bit memory chip 800,000 transistors per chip*	*RISC System/6000*
1994	*first CMOS mainframe*	*System/390 G1*
1997	*ULSI: up to 10 microprocessors*	*System/390 G4*
2001	*ULSI CMOS technology 170 million transistors per 4 sq. cm.*	*pSeries (680, 690)*

TABLE II

VALUES FOR THE RENT'S PARAMETER PAIR $\{k_R, p_R\}$ FOR EACH POWER4 UNIT, WHERE THE VALUES ARE OBTAINED BY FITTING THE UNIT DATA IN FIG. 4 TO THE EXPRESSION $log(N_{conn}) = log(k_R) + p_R \times log(N_{gates})$ DISCUSSED IN THE TEXT.

unit	*macros*	k_R *[range]*	p_R *[range]*
ifu	18	$3.82[3.15, 4.65]$	$0.95[0.92, 0.98]$
fpu	12	$2.46[2.27, 2.66]$	$1.03[1.02, 1.05]$
fxu	4	$2.91[2.36, 3.59]$	$0.98[0.94, 1.02]$
idu	18	$1.24[1.02, 1.52]$	$1.12[1.09, 1.25]$
isu	16	$2.31[1.71, 3.12]$	$1.04[1.00, 1.08]$
lsu	32	$2.28[1.92, 2.71]$	$1.02[1.00, 1.05]$

TABLE III

TOTAL NUMBER OF USED GATES N_{gates}, AVERAGE FANOUT f OF THE INTERCONNECTIONS, ACTUAL NUMBER OF INTERCONNECTIONS N_{conn}, PREDICTED NUMBER OF INTERCONNECTIONS $N(A_R, p_R)$ IN THE IFU, AND ERROR. THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(N_{conn} - N(A_R, p_R)) \times 100}{N(A_R, p_R)}\%$; THE ERRORS ARE SHOWN IN %.

design	N_{gates}	f	N_{conn}	$N(A_R, p_R)$ *[range]*	*Error*
i1	70	1.6	93	$30.6[37.2, 17.1]$	204
i2	220	1.9	318	$126.5[151.9, 71.7]$	151
i3	225	1.7	203	$123.9[148.7, 70.2]$	64
i4	231	2.0	255	$138.0[165.7, 78.3]$	85
i5	779	1.9	800	$545.2[645.0, 314.0]$	47
i6	964	1.9	996	$692.9[817.6, 400.2]$	44
i7	967	2.0	837	$695.3[820.4, 401.6]$	20
i8	1042	1.9	1051	$756.1[891.3, 437.1]$	39
i9	1053	1.7	926	$730.3[860.8, 422.2]$	27
i10	1118	1.9	1147	$805.7[949.0, 466.2]$	42
i11	1250	1.7	1030	$884.8[1040.7, 512.7]$	16
i12	2323	2.0	2131	$1873.8[2188.3, 1094.3]$	14
i13	2561	2.3	2287	$2149.4[2507.3, 1256.8]$	6
i14	2691	2.0	2358	$2171.5[2531.6, 1270.5]$	9
i15	2746	2.0	2500	$2220.6[2588.2, 1299.5]$	13
i16	2871	2.1	3046	$2403.0[2799.4, 1407.0]$	27
i17	4934	2.0	4365	$4228.4[4895.4, 2492.7]$	3
i18	5459	1.9	4614	$4651.5[5379.1, 2745.6]$	-1

TABLE IV

MEASURED AVERAGE WIRELENGTH FOR IFU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. THE ESTIMATES OF AVERAGE WIRELENGTH ARE OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R)$) AND DONATH ($\overline{R}(p_R)$). THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_a - L_{avg}(p_R)) \times 100}{L_{avg}(p_R)}\%$, FOR $L_{avg}(p)$ AND BY $Error = \frac{(L_a - \overline{R}(p_R)) \times 100}{\overline{R}(p_R)}\%$ FOR $\overline{R}(p_R)$; THE ERRORS ARE SHOWN IN %. NOTE THAT L_a, $L_{avg}(p_R)$, AND $\overline{R}(p_R)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p_R)$ [range]	Error	$\overline{R}(p_R)$ [range]	Error
i1	70	3.3	$2.8[2.8, 2.9]$	15	$3.5[3.4, 3.6]$	-6
i2	220	5.5	$3.9[3.8, 4.1]$	40	$5.1[5.0, 5.3]$	7
i3	225	3.4	$4.0[3.8, 4.1]$	-14	$5.2[5.0, 5.3]$	-34
i4	231	4.0	$4.0[3.9, 4.1]$	-1	$5.2[5.1, 5.4]$	-24
i5	779	3.7	$5.8[5.5, 6.0]$	-35	$8.0[7.6, 8.3]$	-53
i6	964	6.0	$6.2[5.9, 6.5]$	-3	$8.6[8.2, 9.0]$	-30
i7	967	5.4	$6.2[5.9, 6.5]$	-13	$8.6[8.2, 9.0]$	-37
i8	1042	4.1	$6.3[6.0, 6.7]$	-36	$8.9[8.4, 9.3]$	-54
i9	1053	4.6	$6.4[6.1, 6.7]$	-27	$8.9[8.5, 9.3]$	-48
i10	1118	3.6	$6.5[6.2, 6.8]$	-44	$9.1[8.7, 9.5]$	-60
i11	1250	4.0	$6.7[6.4, 7.1]$	-40	$9.5[9.0, 9.9]$	-57
i12	2323	8.9	$8.2[7.8, 8.7]$	8	$11.8[11.1, 12.5]$	-25
i13	2561	9.5	$8.5[8.0, 9.0]$	12	$12.2[11.5, 13.0]$	-22
i14	2691	6.8	$8.7[8.1, 9.2]$	-21	$12.5[11.7, 13.2]$	-45
i15	2746	7.9	$8.7[8.2, 9.3]$	-10	$12.6[11.8, 13.3]$	-37
i16	2871	10.2	$8.8[8.3, 9.4]$	16	$12.8[12.0, 13.5]$	-20
i17	4934	8.4	$10.6[9.9, 11.4]$	-21	$15.6[14.5, 16.6]$	-46
i18	5459	9.3	$11.0[10.3, 11.8]$	-15	$16.2[15.1, 17.3]$	-42

TABLE V

MEASURED TOTAL WIRELENGTH L_T FOR IFU DESIGNS $L_T = \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF TOTAL WIRELENGTH OBTAINED BY MULTIPLYING $L_{avg}(p_R)$ FROM THE DAVIS MODEL WITH THE ESTIMATED NUMBER OF INTERCONNECTIONS $N(A_R, p_R)$ FROM THE DONATH MODEL. THE ERROR IS GIVEN BY THE EXPRESSION $Error = \frac{(L_T - L_{avg}(p_R) \times N(A_R, p_R)) \times 100}{L_{avg}(p_R) \times N(A_R, p_R)}\%$. NOTE THAT L_T, $L_{avg}(p_R) \times N(A_R, p_R)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_T	$L_{avg}(p_R) \times N(A_R, p_R)$ *[range]*	*Error*
i1	70	305.5	$87.0[85.2, 88.8]$	251
i2	220	1745.8	$497.2[482.0, 513.0]$	251
i3	225	847.6	$490.0[474.9, 505.7]$	73
i4	231	1011.2	$550.2[533.1, 567.9]$	84
i5	779	2999.5	$3151.1[3011.7, 3296.5]$	-5
i6	964	6218.3	$4284.9[4084.8, 4494.0]$	45
i7	967	4731.2	$4304.2[4103.0, 4514.4]$	10
i8	1042	4261.1	$4793.6[4565.3, 5032.2]$	-11
i9	1053	4472.9	$4645.5[4423.7, 4877.4]$	-4
i10	1118	4140.6	$5225.1[4972.0, 5490.0]$	-21
i11	1250	4312.9	$5947.9[5651.8, 6257.9]$	-27
i12	2323	19794.9	$15437.4[14552.0, 16369.2]$	28
i13	2561	21765.9	$18293.4[17221.8, 19422.0]$	19
i14	2691	16555.1	$18789.9[17677.5, 19962.0]$	-12
i15	2746	20318.6	$19344.8[18194.6, 20557.0]$	5
i16	2871	31544.6	$21249.0[19973.6, 22593.6]$	48
i17	4934	38034.0	$44931.9[41922.0, 48120.0]$	-15
i18	5459	43767.3	$51175.3[47679.4, 54881.4]$	-14

TABLE VI

MEASURED TOTAL WIRELENGTH L_T OF THE SIX UNITS OF THE POWER4 CORE, AS WELL AS THE CORE, AND PREDICTED TOTAL WIRELENGTH L_{tot} (IN GATEPITCHES) FOR $\{k_R, p_R\}$, WHERE $L_{tot}(p_R) = \sum_{i=1}^{N_{conn,i}} L_{avg}(p_R) \times N_{conn,i}$ AND ERROR FOR UNIT SIGNALS i, WHERE $N_{conn,i}$ IS THE TOTAL NUMBER OF INTERCONNECTIONS IN EACH MACRO i. NOTE THAT N_{conn} IS USED SINCE THE NUMBER OF INTERCONNECTIONS PREDICTED BY DONATH'S MODEL BECOMES ZERO FOR $p = 1$ AND BECOMES NEGATIVE FOR VALUES OF $p > 1$. THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_T - L_{tot}(p_R)) \times 100}{L_{tot}(p_R)}\%$. L_T AND $L_{tot}(p_R)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

unit	N_{macros}	L_T	$L_{tot}(p_R)$ *[range]*	*Error*
ifu	18	226826.9	$249497.0[234517.7, 265301.2]$	-9
fpu	12	21915.9	$19046.1[18685.9, 19412.3]$	15
fxu	4	26030.9	$21818.4[20098.3, 23659.3]$	19
idu	18	148700.6	$243123.7[230804.0, 255815.9]$	-39
isu	16	309901.8	$390247.9[356529.6, 426134.9]$	-21
lsu	32	553852.8	$747767.6[709590.4, 787415.6]$	-26
core	$6units$	$1.29E6$	$1.67E6[1.57E6, 1.78E6]$	-23

APPENDIX

This appendix contains tables with model estimates and actual data for all other units in the POWER4 core (FPU, FXU, IDU, ISU, LSU). The five tables show L_a, $L_{avg}(p_R)$, and $\overline{R}(p_R)$ (in units of gatepitches).

TABLE VII

MEASURED AVERAGE WIRELENGTH FOR FPU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R)$) AND DONATH ($\overline{R}(p_R)$) ARE ALSO SHOWN. THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_a - L_{avg}(p_R)) \times 100}{L_{avg}(p_R)}\%$, FOR $L_{avg}(p)$ AND BY $Error = \frac{(L_a - \overline{R}(p_R)) \times 100}{\overline{R}(p_R)}\%$ FOR $\overline{R}(p_R)$; THE ERRORS ARE SHOWN IN %. NOTE THAT L_a, $L_{avg}(p_R)$, AND $\overline{R}(p_R)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p_R)$ *[range]*	*Error*	$\overline{R}(p_R)$ *[range]*	*Error*
f1	41	3.0	$2.6[2.6, 2.6]$	17	$3.0[3.0, 3.1]$	-1
f2	46	2.6	$2.7[2.7, 2.7]$	-5	$3.2[3.2, 3.2]$	-20
f3	133	4.4	$3.7[3.6, 3.7]$	20	$4.7[4.6, 4.7]$	-6
f4	201	5.1	$4.2[4.1, 4.3]$	21	$5.4[5.4, 5.5]$	-7
f5	219	4.1	$4.3[4.2, 4.4]$	-4	$5.6[5.5, 5.7]$	-26
f6	236	4.6	$4.4[4.3, 4.5]$	5	$5.8[5.7, 5.9]$	-20
f7	257	5.6	$4.5[4.5, 4.6]$	24	$6.0[5.9, 6.0]$	-5
f8	300	5.0	$4.8[4.7, 4.9]$	6	$6.3[6.2, 6.4]$	-20
f9	356	5.8	$5.1[5.0, 5.2]$	14	$6.7[6.6, 6.8]$	-14
f10	398	6.9	$5.2[5.1, 5.4]$	32	$7.0[6.9, 7.1]$	-1
f11	497	4.9	$5.7[5.5, 5.8]$	-13	$7.6[7.5, 7.8]$	-36
f12	555	7.1	$5.8[5.7, 6.0]$	21	$8.0[7.8, 8.1]$	-10

TABLE VIII

MEASURED AVERAGE WIRELENGTH FOR FXU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R)$) AND DONATH ($\overline{R}(p_R)$) ARE ALSO SHOWN. THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_a - L_{avg}(p_R)) \times 100}{L_{avg}(p_R)}\%$, FOR $L_{avg}(p)$ AND BY $Error = \frac{(L_a - \overline{R}(p_R)) \times 100}{\overline{R}(p_R)}\%$ FOR $\overline{R}(p_R)$; THE ERRORS ARE SHOWN IN %. NOTE THAT L_a, $L_{avg}(p_R)$, AND $\overline{R}(p_R)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p_R)$ *[range]*	*Error*	$\overline{R}(p_R)$ *[range]*	*Error*
x1	5	1.4	$1.5[1.5, 1.5]$	-10	$1.4[1.4, 1.4]$	-5
x2	33	4.3	$2.4[2.3, 2.4]$	80	$2.8[2.7, 2.8]$	55
x3	304	7.1	$4.5[4.3, 4.7]$	58	$6.0[5.7, 6.3]$	19
x4	2283	9.8	$8.8[8.0, 9.5]$	12	$12.5[11.5, 13.6]$	-22

TABLE IX

MEASURED AVERAGE WIRELENGTH FOR IDU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R)$) AND DONATH ($\overline{R}(p_R)$) ARE ALSO SHOWN. THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_a - L_{avg}(p_R)) \times 100}{L_{avg}(p_R)}\%$, FOR $L_{avg}(p)$ AND BY $Error = \frac{(L_a - \overline{R}(p_R)) \times 100}{\overline{R}(p_R)}\%$ FOR $\overline{R}(p_R)$; THE ERRORS ARE SHOWN IN %. NOTE THAT L_a, $L_{avg}(p_R)$, AND $\overline{R}(p_R)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p_R)$ *[range]*	*Error*	$\overline{R}(p_R)$ *[range]*	*Error*
d1	86	2.2	$3.5[3.4, 3.5]$	-35	$4.2[4.1, 4.3]$	-47
d2	252	4.1	$5.0[4.8, 5.2]$	-18	$6.5[6.3, 6.6]$	-37
d3	513	6.4	$6.5[6.2, 6.7]$	-2	$8.6[8.3, 8.9]$	-26
d4	524	5.5	$6.5[6.3, 6.8]$	-16	$8.7[8.4, 9.0]$	-37
d5	585	3.3	$6.8[6.5, 7.1]$	-52	$9.1[8.8, 9.4]$	-64
d6	677	4.5	$7.2[6.9, 7.5]$	-38	$9.7[9.3, 10.0]$	-54
d7	755	4.9	$7.5[7.2, 7.8]$	-35	$10.1[9.7, 10.5]$	-52
d8	1238	7.7	$9.1[8.6, 9.5]$	-15	$12.5[11.9, 13.0]$	-38
d9	1464	7.5	$9.7[9.2, 10.2]$	-23	$13.4[12.8, 14.0]$	-44
d10	1497	5.4	$9.8[9.3, 10.3]$	-45	$13.5[12.9, 14.1]$	-60
d11	1498	7.3	$9.8[9.3, 10.3]$	-25	$13.5[12.9, 14.1]$	-46
d12	1500	6.0	$9.8[9.3, 10.3]$	-39	$13.5[12.9, 14.1]$	-56
d13	1587	6.3	$10.0[9.5, 10.5]$	-37	$13.8[13.2, 14.5]$	-55
d14	1697	4.9	$10.3[9.8, 10.8]$	-52	$14.2[13.6, 14.9]$	-65
d15	2008	6.9	$11.0[10.4, 11.6]$	-38	$15.3[14.6, 16.0]$	-55
d16	2082	5.6	$11.2[10.6, 11.8]$	-50	$15.5[14.8, 16.3]$	-64
d17	2091	5.3	$11.2[10.6, 11.8]$	-53	$15.6[14.8, 16.3]$	-66
d18	2685	5.4	$12.4[11.7, 13.1]$	-57	$17.3[16.5, 18.2]$	-69

TABLE X

MEASURED AVERAGE WIRELENGTH FOR ISU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R)$) AND DONATH ($\overline{R}(p_R)$) ARE ALSO SHOWN. THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_a - L_{avg}(p_R)) \times 100}{L_{avg}(p_R)}\%$, FOR $L_{avg}(p)$ AND BY $Error = \frac{(L_a - \overline{R}(p_R)) \times 100}{\overline{R}(p_R)}\%$ FOR $\overline{R}(p_R)$; THE ERRORS ARE SHOWN IN %. NOTE THAT L_a, $L_{avg}(p_R)$, AND $\overline{R}(A_R, p_R)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p_R)$ *[range]*	*Error*	$\overline{R}(p_R)$ *[range]*	*Error*
s1	323	3.9	$4.9[4.7, 5.2]$	-20	$6.5[6.2, 6.8]$	-40
s2	331	5.8	$5.0[4.7, 5.2]$	17	$6.6[6.3, 6.9]$	-12
s3	360	3.5	$5.1[4.9, 5.4]$	-31	$6.8[6.5, 7.1]$	-48
s4	656	4.9	$6.3[5.9, 6.7]$	-23	$8.6[8.1, 9.1]$	-43
s5	1188	7.9	$7.8[7.2, 8.3]$	1.8	$10.8[10.1, 11.5]$	-27
s6	1277	5.8	$8.0[7.4, 8.6]$	-28	$11.1[10.4, 11.9]$	-48
s7	1299	7.1	$8.0[7.4, 8.6]$	-12	$11.2[10.4, 12.0]$	-37
s8	1649	5.7	$8.8[8.9, 9.5]$	-35	$12.3[11.4, 13.2]$	-54
s9	1719	8.0	$8.9[8.2, 9.6]$	-10	$12.5[11.6, 13.4]$	-36
s10	1798	7.3	$9.0[8.3, 9.8]$	-19	$12.7[11.8, 13.7]$	-43
s11	2347	6.8	$10.0[9.2, 10.8]$	-32	$14.2[13.1, 15.3]$	-52
s12	2485	8.0	$10.2[9.3, 11.1]$	-21	$14.5[13.4, 15.7]$	-45
s13	3207	9.1	$11.2[10.2, 12.2]$	-19	$16.1[14.8, 17.4]$	-44
s14	3766	4.2	$11.9[10.8, 13.1]$	-65	$17.2[15.7, 18.6]$	-75
s15	3962	11.1	$12.1[11.1, 13.3]$	-8	$17.5[16.0, 19.0]$	-36
s16	6578	12.9	$14.8[13.3, 16.3]$	-12	$21.6[19.6, 23.6]$	-40

TABLE XI

MEASURED AVERAGE WIRELENGTH FOR LSU DESIGNS $L_a = \frac{1}{N_{conn}} \sum_{i=1}^{N_{conn}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R)$) AND DONATH ($\overline{R}(p_R)$) ARE ALSO SHOWN. THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_a - L_{avg}(p_R)) \times 100}{L_{avg}(p_R)}\%$, FOR $L_{avg}(p)$ AND BY $Error = \frac{(L_a - \overline{R}(p_R)) \times 100}{\overline{R}(p_R)}\%$ FOR $\overline{R}(p_R)$; THE ERRORS ARE SHOWN IN %. NOTE THAT L_a, $L_{avg}(p_R)$, AND $\overline{R}(p_R)$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}	L_a	$L_{avg}(p_R)$ *[range]*	*Error*	$\overline{R}(p_R)$ *[range]*	*Error*
l1	117	2.5	3.5[3.4, 3.6]	−30	4.4[4.3, 4.5]	−44
l2	259	7.1	4.5[4.4, 4.6]	59	5.9[5.8, 6.1]	21
l3	294	7.0	4.7[4.6, 4.8]	49	6.2[6.0, 6.4]	13
l4	506	5.9	5.6[5.4, 5.8]	6	7.6[7.4, 7.8]	−22
l5	567	6.0	5.8[5.6, 6.0]	3	7.9[7.7, 8.2]	−24
l6	641	5.9	6.1[5.9, 6.3]	−3	8.3[8.0, 8.6]	−29
l7	687	5.9	6.2[6.0, 6.5]	−5	8.5[8.2, 8.8]	−31
l8	1011	5.2	7.1[6.8, 7.4]	−27	9.9[9.5, 10.3]	−48
l9	1024	5.4	7.2[6.9, 7.4]	−24	9.9[9.6, 10.3]	−46
l10	1191	5.4	7.6[7.2, 7.9]	−29	10.5[10.1, 10.9]	−49
l11	1235	5.5	7.6[7.3, 8.0]	−28	10.7[10.3, 11.1]	−48
l12	1392	5.9	8.0[7.6, 8.3]	−26	11.2[10.8, 11.6]	−47
l13	1527	6.0	8.3[7.9, 8.6]	−28	11.6[11.1, 12.1]	−49
l14	1655	6.8	8.5[8.1, 8.9]	−20	12.0[11.5, 12.5]	−43
l15	1722	10.0	8.6[8.2, 9.0]	16	12.2[11.7, 12.7]	−18
l16	1835	7.1	8.8[8.4, 9.2]	−19	12.5[11.9, 13.0]	−43
l17	1892	9.4	8.9[8.5, 9.3]	6	12.6[12.1, 13.2]	−25
l18	1920	10.1	9.0[8.6, 9.4]	13	12.7[12.2, 13.2]	−20
l19	1954	9.0	9.0[8.6, 9.4]	−1	12.8[12.2, 13.3]	−30
l20	2241	4.6	9.5[9.0, 9.9]	−51	13.5[12.9, 14.1]	−66
l21	2348	8.3	9.6[9.2, 10.1]	−14	13.7[13.1, 14.4]	−40
l22	2353	10.9	9.6[9.2, 10.1]	13	13.8[13.1, 14.4]	−21
l23	2368	5.5	9.7[9.2, 10.1]	−43	13.8[13.2, 14.4]	−60
l24	2516	8.0	9.9[9.4, 10.4]	−19	14.1[13.5, 14.8]	−43
l25	2569	6.9	10.0[9.5, 10.5]	−31	14.2[13.6, 14.9]	−51
l26	3398	7.3	11.0[10.5, 11.6]	−34	15.9[15.2, 16.7]	−54
l27	3728	8.8	11.4[10.8, 12.0]	−23	16.5[15.7, 17.3]	−47
l28	3866	9.3	11.6[11.0, 12.2]	−20	16.8[15.9, 17.6]	−45
l29	4035	11.8	11.8[11.2, 12.4]	−2	17.0[16.2, 17.8]	−31

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