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Wirelength Distributions for Signals Associated with Functional Logic Circuitry and Synchronization Circuitry in Ultralarge-scale Integrated Circuit Designs

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Wire-length distribution models for functional logic circuitry and synchronization circuitry in ultralarge-scale integrated circuit designs

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Abstract

The synchronization of functional logic signals in computer hardware components is required for successful design and implementation of high-performance hardware. The goal of this paper is to obtain methods to quantify the requirements of the two groups of signals. Most of the work concerning Rent's Rule prior to the present paper has been based on a 1971 interpretation of two unpublished memoranda written in 1960 by E. F. Rent at IBM, even though today's computer components require, in addition to their logic function, a complex synchronization network that synchronizes the operation of functional logic at today's multi-GHz frequencies. In this paper, we will refer to the type of signals and circuitry that are associated with logic function with the term *function type* and will use the term *synchronization type* to refer to the remaining circuits and signals; most of the remaining signals are associated with a clocking network superimposed on the functional logic, and the rest perform other non-functional tasks such as clock control and scan. Prior work does not distinguish among signals and circuitry according to these two types: *function type* and *synchronization type*. However, because of the increasingly complex design and implementation of synchronization circuitry since 1960-1971 for high-performance chips, an understanding of the separate requirements of both types is needed. To address this point, we have obtained copies of Rent's two original memos in which Rent describes functional logic of two 1960 computers and describes a method to assess connections and circuits associated with functional logic. In this paper, we will: (1) discuss the two types; (2) apply an historically-equivalent interpretation of Rent's Rule to circuitry with *function type* in actual ultralarge scale integrated (ULSI) circuit designs; (3) present a new empirical model for wire-length distributions for circuitry with *synchronization type*; and (4) compare these models with wire-length distributions for signals of both types for 100 POWER4 control logic designs. We will show that these methods provide greatly improved qualitative agreement with actual wire-length distributions compared with prior methods.

Index Terms

ULSI, VLSI, circuit design, functional circuitry, synchronization circuitry, clock distribution, clock signal, local clock buffer, latch.

I. INTRODUCTION

With the increasing complexity of synchronization circuitry associated with high-performance functional logic circuitry in computer hardware components since early work by E. F. Rent in 1960, a reevaluation of requirements for today's computer components is needed. All of the prior extensive work including for example[1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17] concerning Rent's Rule has been based on the 1971 interpretation [18] of two unpublished memoranda [19] written in 1960 by E. F. Rent at IBM, even though

today's computer components differ significantly from those at that time[20], [21]. For example, today's computer components require, in addition to correct logic function, the successful implementation of complex synchronization circuitry to achieve hardware that operates at multi-GHz frequencies. All work prior to this paper does not distinguish between the impact of two different types of circuitry - namely, circuitry associated with functional logic and circuitry associated with synchronization - on the design and implementation of computer hardware components. In this paper, we will use the term *function type* to refer to signals and circuitry that are associated with logic function and will use the term *synchronization type* to refer to the remaining circuits and signals; most of the remaining signals are associated with a clock network superimposed on the functional logic, and the rest perform other non-functional tasks such as clock control and scan. However, because of the increasingly complex design and implementation of synchronization circuitry since 1960-1971, an understanding of the requirements of both types is needed.

We have obtained copies of Rent's two IBM memoranda [19] and have continued our study of them in order to further understand Rent's original intent. In these memos, Rent is concerned with functional logic in 1960 computer hardware components and describes the connectivity of signals and circuits associated with functional logic. Based on our careful reading of these two memos, we will evaluate components of actual ULSI circuit designs according to the functional type described by Rent. For an evaluation of ULSI designs in a manner similar to the one described by Rent, we will need to separate functional logic components from the entire group of components, thereby separating the entire group into the two types: *functional type* and *synchronization type*. In this paper, we will (1) introduce the two circuitry types; (2) apply an historically-equivalent interpretation of Rent's Rule[21] to circuitry with *function type* in actual ULSI designs; (3) present a empirical model for wire-length distributions for circuitry with *synchronization type*; (4) present measured wire-length distributions for signals of both types in actual ULSI designs. The designs selected for this study are all functional control designs in the IBM POWER4 core, which is currently incorporated in the IBM Enterprise Server pSeries 680 and pSeries 690[22], [23]. These control designs occupy approximately 50% of the core area.

The first application will be to extract historically-equivalent empirical values of Rent's parameters for signals with *function type*. We will then evaluate existing wire-length distribution

models[7], [8], [10] and existing expressions for average wire-length as functions of these parameters. We then compare the distributions and values of average wire-lengths with measurements from actual chip designs. We will show that these methods provide improved qualitative agreement for wire-length estimates compared with prior work[2], [3], [17] in which no distinction is made between the functional logic circuitry and synchronization circuitry. The second application will be to compare actual total wirelength requirements for signals with *synchronization type* with values obtained with a new empirical model.

The methods presented in this paper provide designers with techniques to evaluate the amount and distribution of wire required to interconnect components according to type in order to achieve buildable and functional chip designs within increasingly severe project constraints of real estate, number of metal layers, operating frequency, and power dissipation[5], [6], [13], [15], [24], [25], [26].

II. Types of circuitry and signals

In this section, we present a brief discussion of two types of signals and circuitry in ASIC-like designs. The two types are *functional type* and *synchronization type*, as described in the previous section. The designs are composed of an interconnected assortment of logic gates that implement an assigned function as well as other logic gates that synchronize the operation of the functional gates.

A. Circuitry and signals with functional type

A signal or a logic gate is assigned with *functional type* when this circuitry element is required to implement the design function correctly. The number of connections $N_{conn}^{function}$ associated with functional logic can be obtained by analogy with the treatment in Ref. [21] according to the expression,

$$N_{conn}^{function} = \sum_{i=1}^{N_{nets}^{function}} (F_i + 1) - N_{IO}^{function}, \tag{1}$$

where the sum is taken over only those signal nets $N_{nets}^{function}$ associated with functional logic, F_i is the fanout of each net, and $N_{IO}^{function}$ is the number of input pins and output pins associated with functional logic. As described in Ref.[21], the term $(F_i + 1)$ represents the total number of connections made by a single net in a design; for the designs considered in this work, each net

has a single driver and has fanout $F_i \geq 1$. Therefore, the total number of connections of signals associated with functional logic is obtained by taking the sum of this term $(F_i + 1)$ over this subset of signals, as given by the expression,

$$N_{conn}^{function} = F_{total}^{function} + N_{nets}^{function} - N_{IO}^{function}, \tag{2}$$

where Eqn. 2 follows from Eqn. 1, and $F_{total}^{function}$ and $N_{nets}^{function}$ are the total fanout and total number of signal nets associated with functional logic, respectively.

The total number of gates $N_{gates}^{function}$ associated with *function type* is obtained by subtracting the number of gates N_{gates}^{synch} associated with *synchronization type* from the total number of gates N_{gates} according to the expression,

$$N_{gates}^{function} = N_{gates} - N_{gates}^{synch}, \tag{3}$$

where

$$N_{gates}^{synch} = N_{lat} + N_{LCB} + N_{LCBgates}, \tag{4}$$

and N_{lat} is the number of latches, N_{LCB} is the number of local clock buffers (LCBs), and $N_{LCBgates}$ is the number of logic gates associated with the LCBs.

B. Circuitry and signal nets with synchronization type

A signal net or a logic gate is assigned with *synchronization type* when the signal net or gate does not implement the design function. In this case, the circuitry element is associated with synchronization or other non-function tasks. To understand the wire requirements for signals associated with synchronization circuitry, we first discuss properties of a clock network that is superimposed on the interconnected network of functional gates. Examples of signals associated with synchronization circuitry are shown in Fig. 3. This figure illustrates that the global clock signal clk is input into 32 LCBs; in turn the LCBs distribute the clk signal to latches. The distribution of other signals associated with the clock network is also shown.

An expression for the number of gates N_{gates}^{synch} associated with synchronization circuitry is given in the previous section. An expression for the number of signals N_{synch} associated with synchronization circuitry can be approximated as the sum of three contributions: (1) unity, to represent the contribution of the single global clock signal clk; (2) the number N_{dc} of dc signals

associated with synchronization circuitry, such as clock control and scan; and (3) twice the number N_{LCB} of LCBs, where the factor of 2 arises since typically each LCB generates two clock signals as inputs for the $L1$ and $L2$ master-slave latches, from which we obtain the expression,

$$N_{synch} \sim 1 + N_{dc} + 2 \times N_{LCB}, \tag{5}$$

where the approximation is used because not all dc signals are input into each LCB and most (but not all) LCBs generate two signals. With Eqn. 5, $N_{dc} = 5$, and the values for N_{LCB} shown in Table I for POWER4 IFU designs, we estimate values for N_{synch} shown in the table. From the table we see that N_{synch} is approximately equal to the actual number of signals $N_{synchsig}$ associated with synchronization circuitry for all designs except for *i17* which contains a large number of short scan signals.

III. Wire-lengths for signals associated with functional logic

In this section, we apply an historically-equivalent interpretation of Rent's Rule[21] to obtain empirical Rent's parameters for circuitry with *function type*. Figure 1 shows a log-log plot of $N_{conn}^{function}$ as a function of $N_{gates}^{function}$. From this plot, the parameter pair for signals associated with functional circuitry can be extracted according to a method described in Ref. [21]; we will refer to this parameter pair with the notation $\{k_R^{function}, p_R^{function}\}$, where the terms $k_R^{function}$ and $p_R^{function}$ are given as the inverse log of the intercept and slope, respectively, of a linear fit to the quantities in Fig. 1, according to the expression,

$$Log(N_{conn}^{function}) = Log(k_R^{function}) + p_R^{function} \times Log(N_{gates}^{function}) \tag{6}$$

The values and ranges for $\{k_R^{function}, p_R^{function}\}$ for POWER4 IFU control designs are shown in Table II. The table shows that values for $k_R^{function}$ lie between $1.7 \leq k_R^{function} \leq 6.2$, and that $p_R^{function}$ is approximately 1, with range $0.89 \leq p_R^{function} \leq 1.08$.

We estimate wire requirements for functional logic signals by evaluating existing models[2], [7], [8], [10] for the number of signals $N(A_R^{function}, p_R^{function})$, normalized probability density function $p_{int}(L)$, probability density function $P(L)$, and average wire-length ($L_{avg}(p_R^{function})$ from the Davis model and $\overline{R}(p_R^{function})$ from the Donath model) as functions of the parameter pair $\{k_R^{function}, p_R^{function}\}$ as shown in Tables III- VI. Table III shows that $N(A_R^{function}, p_R^{function})$

overestimates $N_{conn}^{function}$ for all designs except for the two smallest designs by up to 61%; however, the estimates are improved compared with those obtained in Ref.[21] with parameter pair $\{k_R, p_R\}$ in which no distinction is made between functional circuitry and synchronization circuitry. In this case, we take the Error (in $\%$) to be given by the expression,

$$Error = \frac{(N_{conn}^{function} - N(A_R^{function}, p_R^{function})) \times 100}{N(A_R^{function}, p_R^{function})}\%. \quad (7)$$

The average fanout f of these signals is $1.5 \leq f \leq 2.0$. Table IV shows a comparison of $L_{avg}(p_R^{function})$ and $\overline{R}(p_R^{function})$ with the actual average wire-length $L_a^{function}$; values of $\overline{R}(p_R^{function})$ do not approximate the actual average wirelength as well as do the values of $L_{avg}(p_R^{function})$. Table V shows a comparison of estimates of the total wirelength requirement $L_{tot}^{function}$ with the actual total wirelength $L_T^{function}$. For these estimates we choose $L_{avg}(p_R^{function}) \times N(A_R^{function}, p_R^{function})$; the estimated values tend to overestimate the actual values by $50\% - 60\%$. Table VI shows a second comparison of estimates of the total wirelength requirement with $L_T^{function}$ where we use $L_{avg}(p_R^{function}) \times N_{conn}^{function}$; estimates are within 36% of the values of $L_T^{function}$ for each design.

We find it necessary to compare total wirelength requirements for all POWER4 units with $N_{conn}^{function}$ rather than with $N(A_R^{function}, p_R^{function})$ since the expression for $N(A_R^{function}, p_R^{function})$ takes on nonphysical values (i.e., becomes zero or negative) for those units with values of $p_R^{function} \geq 1$. Table VII compares $L_T^{function}$ with $L_{tot}(p_R^{function})$ where,

$$L_{tot}(p_R^{function}) = \sum_{i=1}^{N_{macros}} N_{conn}^{function} \times L_{avg}(p_R^{function}); \quad (8)$$

estimates are within 34% of the actual totals for all units and is within 1% of the actual total wirelength for the IFU. Total wirelength estimates for all control designs in the POWER4 core are within 24% of the actual values.

We next evaluate the interconnect density functions provided by the Davis (1998) model with the parameter pair $\{k_R^{function}, p_R^{function}\}$ for four POWER4 IFU designs and compare with actual wire-length distributions. Figures 2(a)-(d) show the normalized probability density function $p_{int}(L)$ (solid circles) and probability density function $P(L)$ (hollow squares) for four designs with different number of $N_{gates}^{function}$ in the POWER4 IFU, where the gatepitch is taken to be the book height of the standard cells. For these comparisons, we choose the normalized probability

density functions because the Donath expression [2] for $N(A_R^{function}, p_R^{function})$ (assumed by the Davis model) takes nonphysical values when p is greater than 1. The solid lines show $p_{int}(L)$ and $P(L)$; upper and lower limit curves are also shown for $p_{int}(L)$. This figure shows that the qualitative fit to the data is much improved compared with the curves in Ref.[21] in which the parameter pair $\{k_R, p_R\}$ is used, particularly since the spread in the range shown by the upper and lower bounds is greatly reduced, closer to the actual wirelength distribution.

IV. WIRE-LENGTHS FOR SIGNALS ASSOCIATED WITH SYNCHRONIZATION CIRCUITRY

In this section, we discuss wirelength requirements for signals associated with synchronization circuitry. The total wirelength requirement for these signals can be represented with the term L_{tot}^{synch} and can be obtained by summing the contributions to total wirelength that result from each of the three terms in Eqn. 5. These contributions are: (1) the wirelength L_{clk} associated with the input global clock signal clk; (2) the wirelength L_{dc} associated with the number N_{dc} of dc signals; and (3) the wirelength L_{LCB} associated with the signals generated by each LCB, such that L_{tot}^{synch} can be approximated according with the expression,

$$L_{tot}^{synch} \sim L_{clk} + L_{dc} + L_{LCB}. \tag{9}$$

We now provide approximate expressions for the three terms on the right-hand side of Eqn. 9. The total length L_{clk} of the clk signal is obtained by summing over all local clock wires i, according to the expression,

$$L_{clk} = \sum_{i=1}^{N_{clk}} l_{clk}^i, \tag{10}$$

where N_{clk} is the number of connected clk pins, and l_{clk}^i is the length of each local clock wire i. Three examples of straight clk wires from the clk input pins to three LCBs are shown in Fig. 4. For the case in which vertical rows of pins are separated by N_d gatepitches (gatepitch = d), each local clock wire i has length $0 \leq l_{clk}^i \leq N_d/2$, where l_{clk}^i is expressed in gatepitches. Since the minimum (maximum) horizontal distance between each LCB and each clk pin is 0 ($N_d/2$) (in gatepitches), an estimate of L_{clk} is then,

$$L_{clk} \sim \frac{N_d}{4} \cdot N_{clk} \sim \frac{N_d}{4} \cdot \frac{N_{LCB}}{4}, \tag{11}$$

since on the order of 3 to 4 LCBs are connected to each clk pin in POWER4 designs.

An expression for L_{dc} can be obtained by summing over the lengths of all dc signals,

$$L_{dc} = \sum_{i=1}^{N_{dc}} l_{dc}^{i}, \tag{12}$$

where N_{dc} is the number of dc signals, and l_{dc}^{i} is the length of each dc signal. The maximum signal length can be taken to be twice the (square) design width, namely, $2 \times \sqrt{N_{gates}}$[7]. With this assumption, Eqn. 12 becomes,

$$L_{dc} \sim 2 \cdot N_{dc} \cdot \sqrt{N_{gates}}. \tag{13}$$

Next, an expression for L_{LCB} follows from some knowledge of the placement of and relative proportions of latches and LCBs in ASIC-like designs. We can write L_{LCB} according to the expression,

$$L_{LCB} \sim 2 \cdot l_{LCB} \cdot N_{LCB}, \tag{14}$$

where the factor of 2 accounts for contributions from both signals generated by each LCB, l_{LCB} is the wirelength that connects latches to each LCB, and N_{LCB} is the number of LCBs in the design. The term l_{LCB} is a function of the relative placement of the latches and LCBs as quantified by an observed clustering parameter, $\tilde{l}_c$, and the ratio of the total number of latches to the total number of LCBs, N_{lat}/N_{LCB}. As an example, Fig. 5 shows a wire with length l_{LCB} that connects N_{lat} clustered latches in a typical ASIC-like design; the wirelength l_{LCB} is shown for three different cluster distances $l_c = 0, 1, 2$ (in gatepitches) in (a)-(c). By comparison, in a typical dataflow design, a signal with length l_{LCB} connects latches stacked in single rows (a) and double rows (b) adjacent to the LCB, as shown in Fig. 6. Such row placements are not observed in ASIC-like designs for which CAD tools tend to implement latch clusters rather than latch rows that require manual intervention. Table VIII lists the route length l_{LCB} (in gatepitches) for three values of the clustering parameter l_c (also in gatepitches). A value for the clustering parameter $\tilde{l}_c$ for each design can be extracted from Table VIII and the mean of a Gaussian fit to wire distributions for signals associated with synchronization circuitry. Figures 2(a')-(d') show examples of wire distributions for signals associated with synchronization circuitry in four designs in the POWER4 IFU with the results of Gaussian fits shown as solid lines. From the means, we see that $\tilde{l}_c$ is approximately 1 except for those few designs with largest values of $N_{gates}^{function}$, for which $\tilde{l}_c$ is approximately 2.

An expression for L_{tot}^{synch} is obtained by substituting Eqn. 11 and Eqns. 13- 14 into Eqn. 9,

$$L_{tot}^{synch} \sim \frac{N_d}{4} \cdot \frac{N_{LCB}}{4} + 2 \cdot N_{dc} \cdot \sqrt{N_{gates}} + 2 \cdot l_{LCB} \cdot N_{LCB}, \quad (15)$$

where l_{LCB} is given in Table VIII. Table X compares values obtained with Eqn. 15 with actual measured values, where $N_d = 18$ and $N_{dc} = 5$. Estimates of the total wirelength obtained with Eqn. 15 are reasonable and are within $30\% - 40\%$ of the actual wirelength for all designs except the two designs with least N_{gates}^{synch}. Moreover, for the three designs that contain the most synchronization circuitry, L_{tot}^{synch} is within approximately $20\% - 30\%$ of the actual values.

V. DISCUSSION

The methodology described in this paper has two primary benefits for obtaining wirelength requirements and wirelength distributions for ASIC-like chip designs. First, this methodology provides a new way to think about the subcomponents of designs. The first group, which we denote with the term *function type*, consists of logic gates that implement the intended function (e.g., AND gates, OR gates, inverters), and the second group, which we denote with the term *synchronization type*, consists of gates that synchronize the logic (e.g., latches, local clock buffers). Second, this methodology provides a new understanding of the signal connectivity of the two groups. This methodology shows that itemizing the design components according to *function type* and *synchronization type* and separating the signal circuitry into two corresponding groups does indeed provide effective techniques (1) for obtaining relatively accurate wirelength estimates and (2) for thinking about the logic for which we wish to obtain wire distributions.

It should be noted that in this paper we have assumed that all signals in a design can be categorized according to one of two types of signals. This assumption is reasonable, as each signal can be categorized as one of these two types. We have seen that the accuracy with which we can now assess wirelength requirements in designs is now quite acceptable and can be used to assess wirelength requirements in high-performance microprocessors such as the POWER4 chip. However in principle, to obtain more detailed information about design wirelength requirements, one may further subdivide the two groups of signals. For example, two possible additional subcategories for *function type* include *control signals* and *datapath signals*; possible additional subcategories for *synchronization type* include *clocking signals*, *clock control signals*, and *scan signals*.

This paper has been concerned with wirelength requirements of ASIC-like designs. Additional work that remains includes methodologies for wirelength requirements of dataflow designs and cache arrays. With this new information, it will be possible to assess overall wirelength in chips by summing the contributions from all designs, namely ASIC-like designs, dataflow designs, and cache arrays.

VI. Conclusion

This paper presents assessments of wirelength requirements for signals associated with functional logic and signals associated with synchronization in today's computer hardware components. Work prior to this paper does not distinguish among signals and circuitry according to the two types of signals. However, because of the increasingly complex design and implementation of synchronization circuitry since 1960-1971, an understanding of the requirements of both types was needed. To address this need, we obtained copies of Rent's two original memos in which he describes functional logic of two 1960 computers and describes a method to assess connections and circuits associated with functional logic.

In this paper, we have discussed the two types of signals and circuitry - the functional type and the synchronization type; we have applied an historically-equivalent interpretation of Rent's Rule to circuitry with *function type* in actual ultralarge scale integrated (ULSI) circuit designs; we presented an empirical model for wire-length distributions for circuitry with *synchronization type*; and compare wire-length distributions for signals of both types in actual ULSI designs in the POWER4 chip.

The methods we describe in this paper provide improved qualitative agreement and accuracy in wire-length estimates compared with prior methods. In total, 100 ASIC-like designs in the POWER4 core are investigated in this study. For POWER4 IFU *functional logic*, estimates of average wireltength are typically within 32% of the actual average wirelength for designs with more than 1900 logic gates and are within 44% of the average wirelength for designs with fewer than 1900 logic gates. Very good qualitative agreement with actual wirelength distributions is obtained with the use of an historically-equivalent interpretation of Rent's memos for circuits with *function type*. For POWER4 IFU circuitry with *synchronization type*, our estimate of the total wirelength is within 33% for designs with more than 174 gates associated with synchronization circuitry. Moreover, we obtain estimates of total wirelength that are within 34% of

the actual total wirelength for all ASIC-like designs in each POWER4 unit. As a result, we feel confident that the methods presented in this paper now provide designers with techniques to evaluate the amount and distribution of wire required to interconnect ULSI components in high-performance microprocessors such as the POWER4 chip.

VII. Acknowledgements

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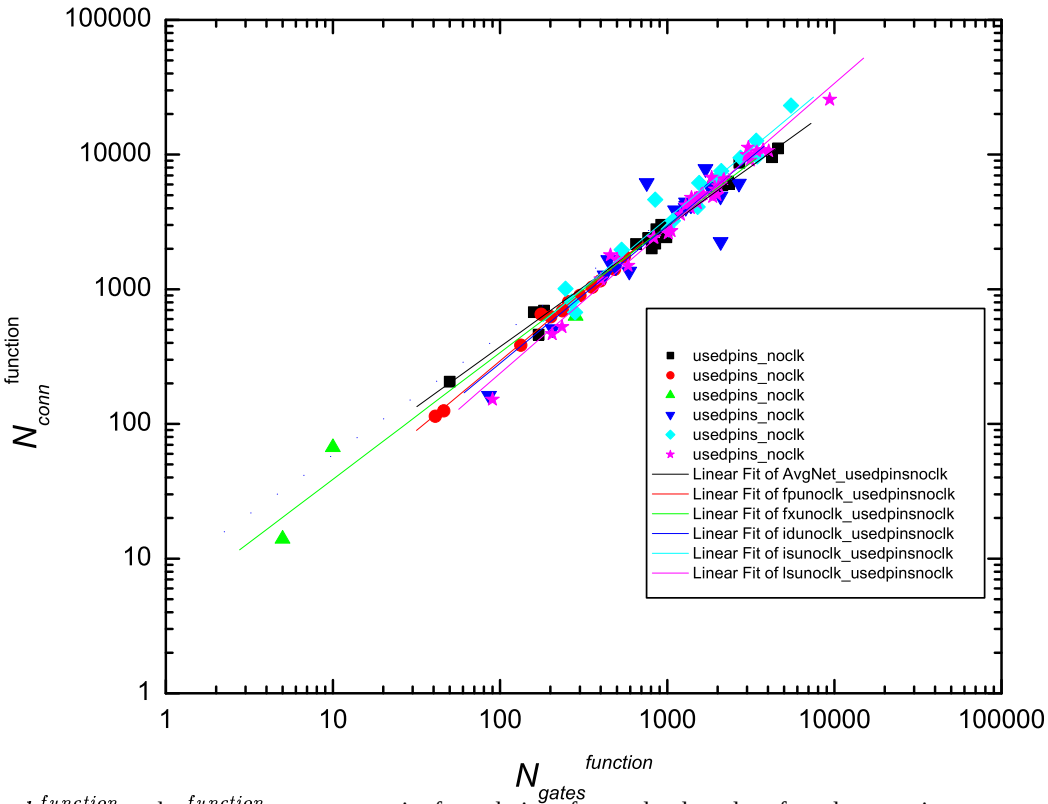

Fig. 1. Method to extract $k_R^{function}$ and $p_R^{function}$ parameter pairs from designs from a log-log plot of used connections $N_{conn}^{function}$ as a function of used gates $N_{gates}^{function}$ for six units in POWER4 chip. The values are summarized in Table II.

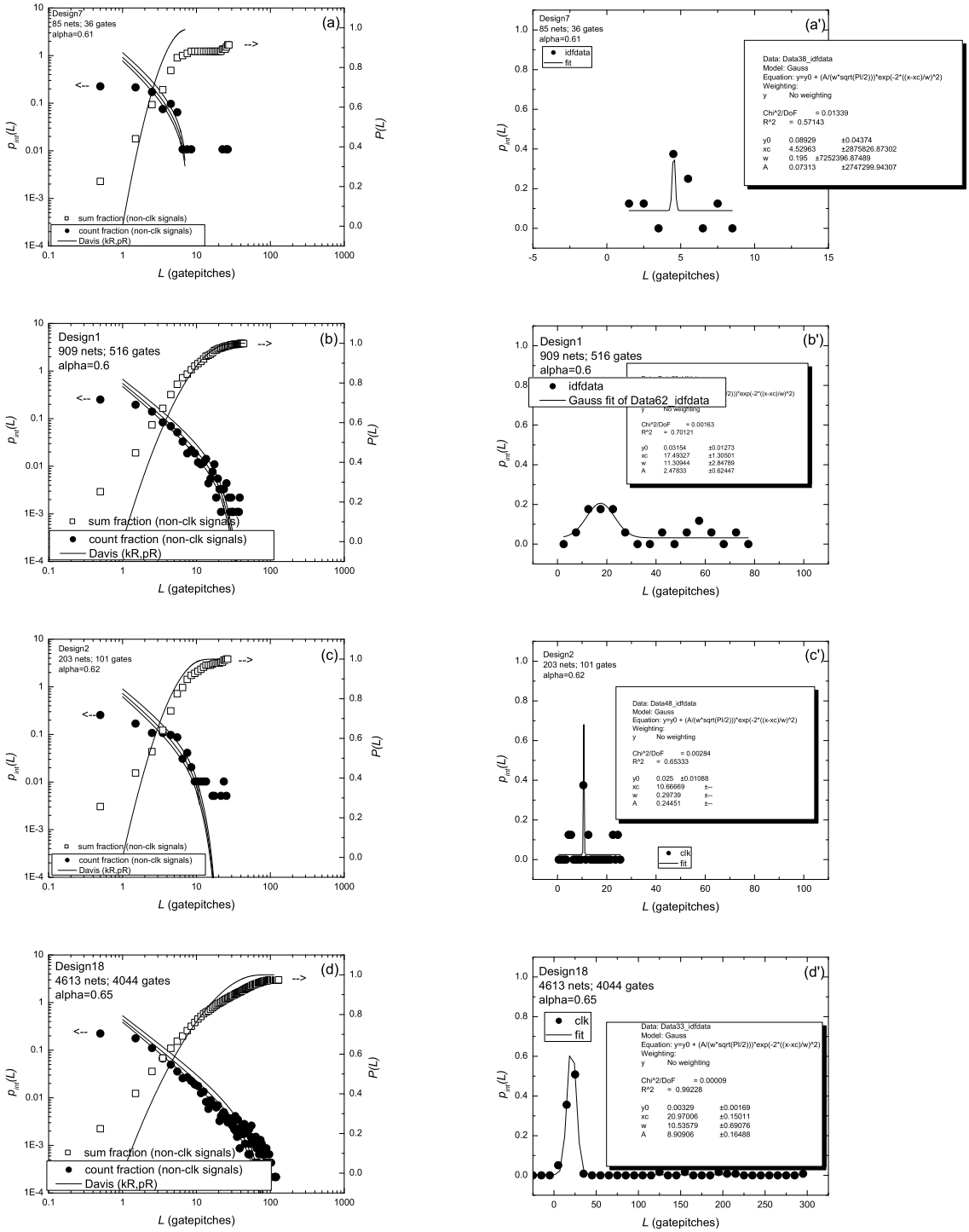

Fig. 2. Normalized probability density function $p_{int}(L)$ (solid circles) and probability density function $P(L)$ (hollow squares) for (a) design7, (b) design1, (c) design2, and (d) design18 in the POWER4 IFU. For all designs, the gatepitch is taken to be the book height d of the standard cells. For (a)-(d), the solid lines are obtained from the Davis model with $\{k_R^{function}, p_R^{function}\}$. For (a')-(d'), the solid circles indicate the normalized probability density of signals associated with synchronization circuitry in each of the designs.

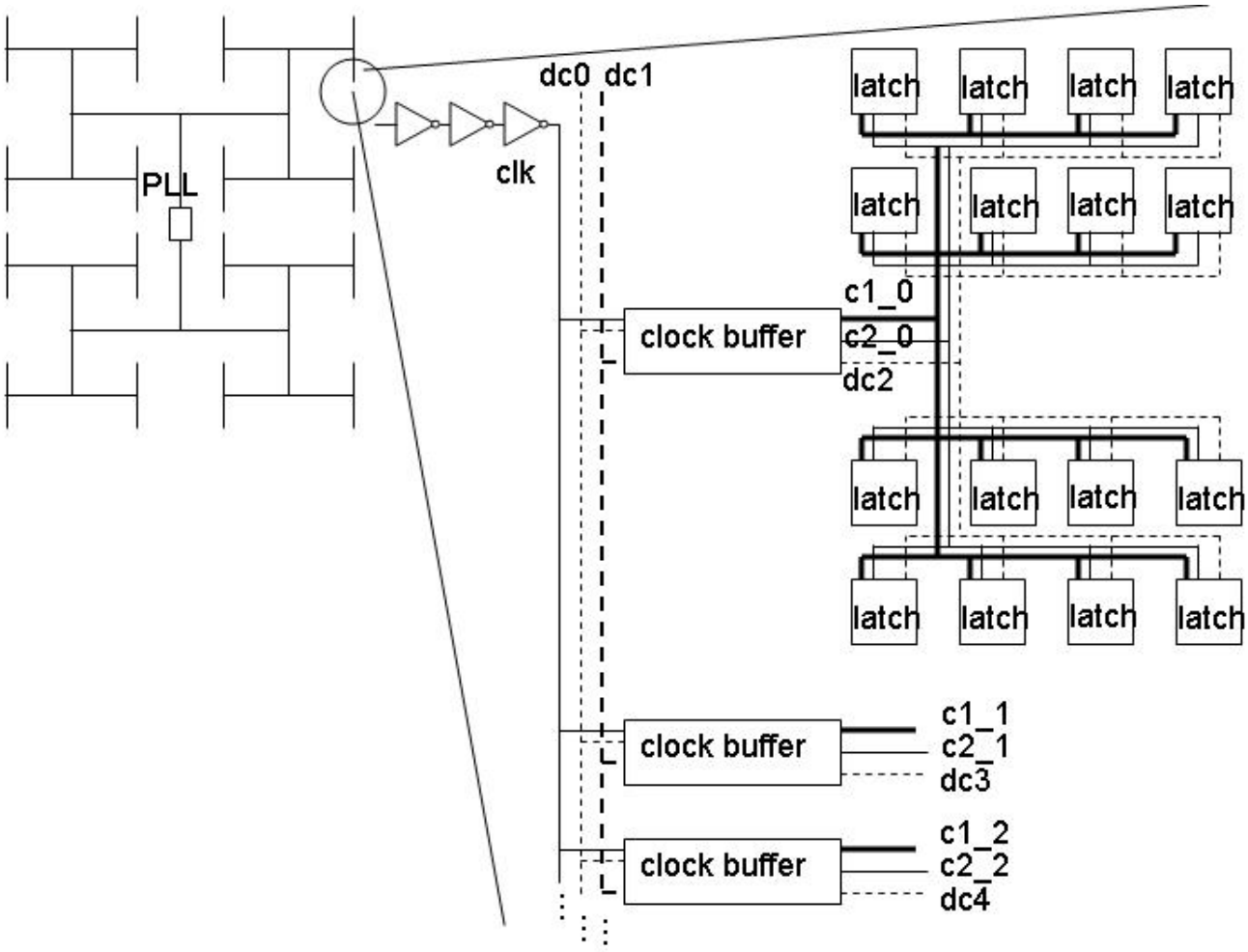

Fig. 3. Circuitry associated with a clock distribution. The global wiring is shown on the left-hand side of the figure; the local clock wiring within small regions is shown on the right-hand side of the figure, where the global clock signal clk is input into local clock buffers (LCBs) which clock the latches.

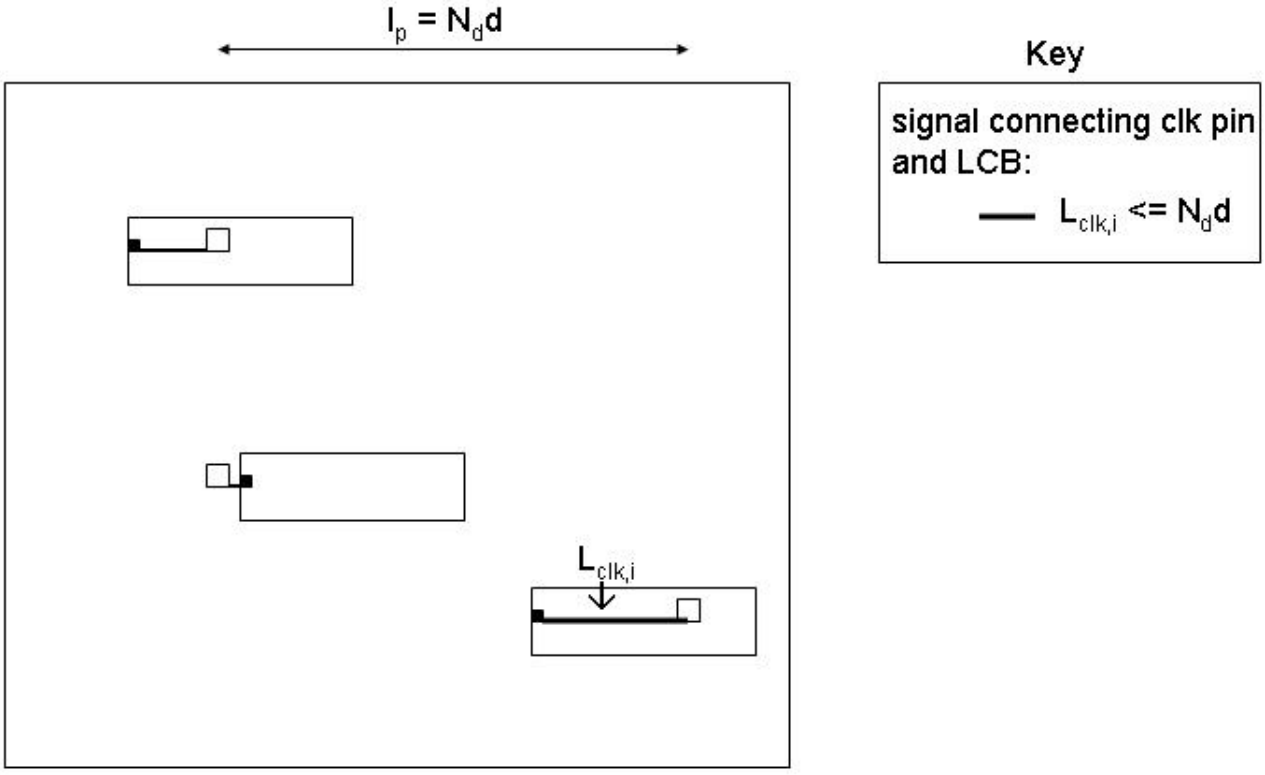

Fig. 4. Examples of routes that wire the global clock signal clk between the pins and local clock buffers.

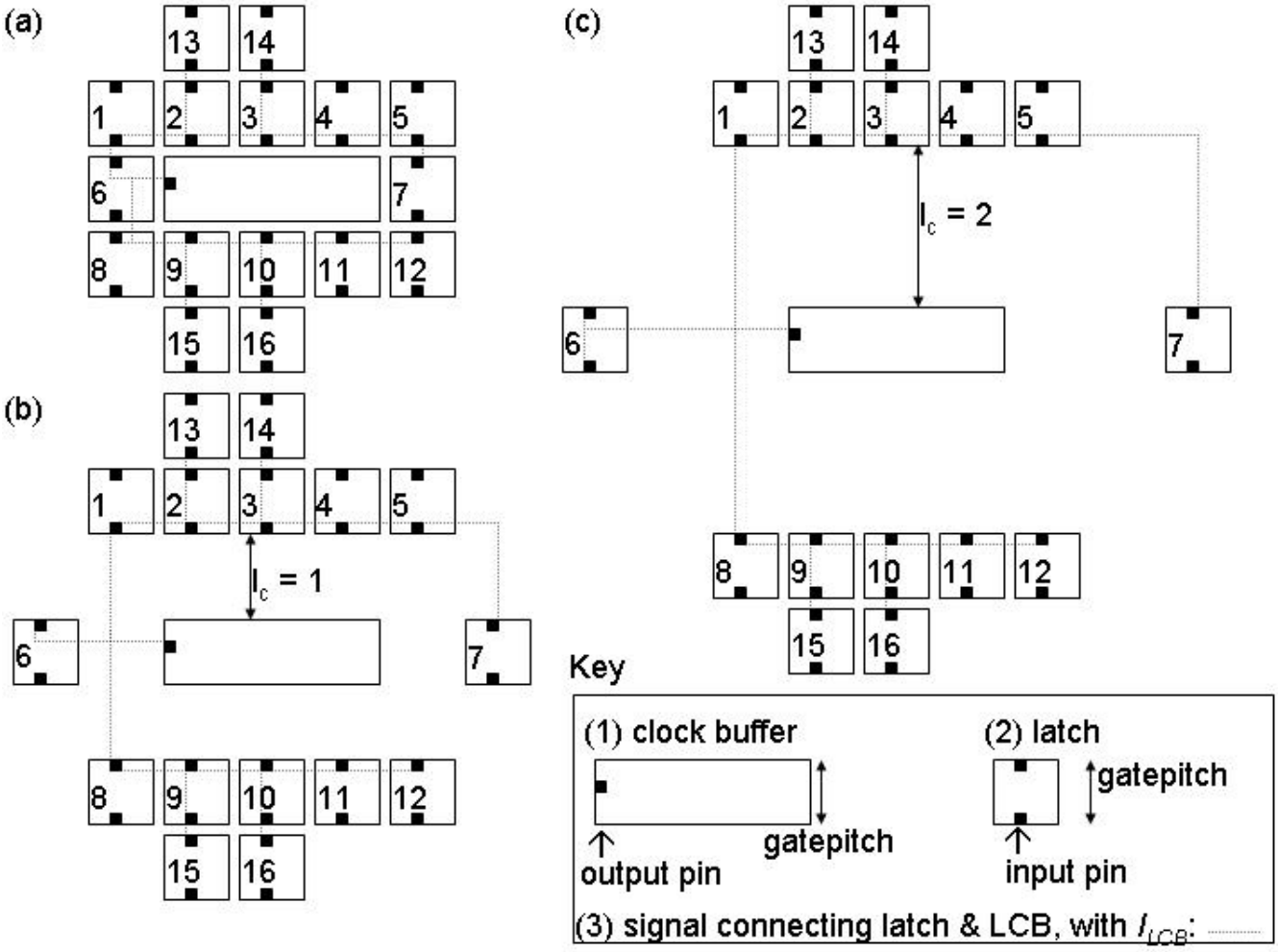

Fig. 5. Example of wire with length l_{LCB} for clock signals connecting latches clustered around each LCB, where l_{LCB} is shown as a dashed line for three different cluster distances l_c (in gatepitches); l_c represents the clustering parameter. The measured clustering parameter is represented with $\tilde{l}_c$. (a), (b), and (c) show an example of a signal route for latches that are clustered around an LCB with $l_c = 0, 1, 2$, respectively.

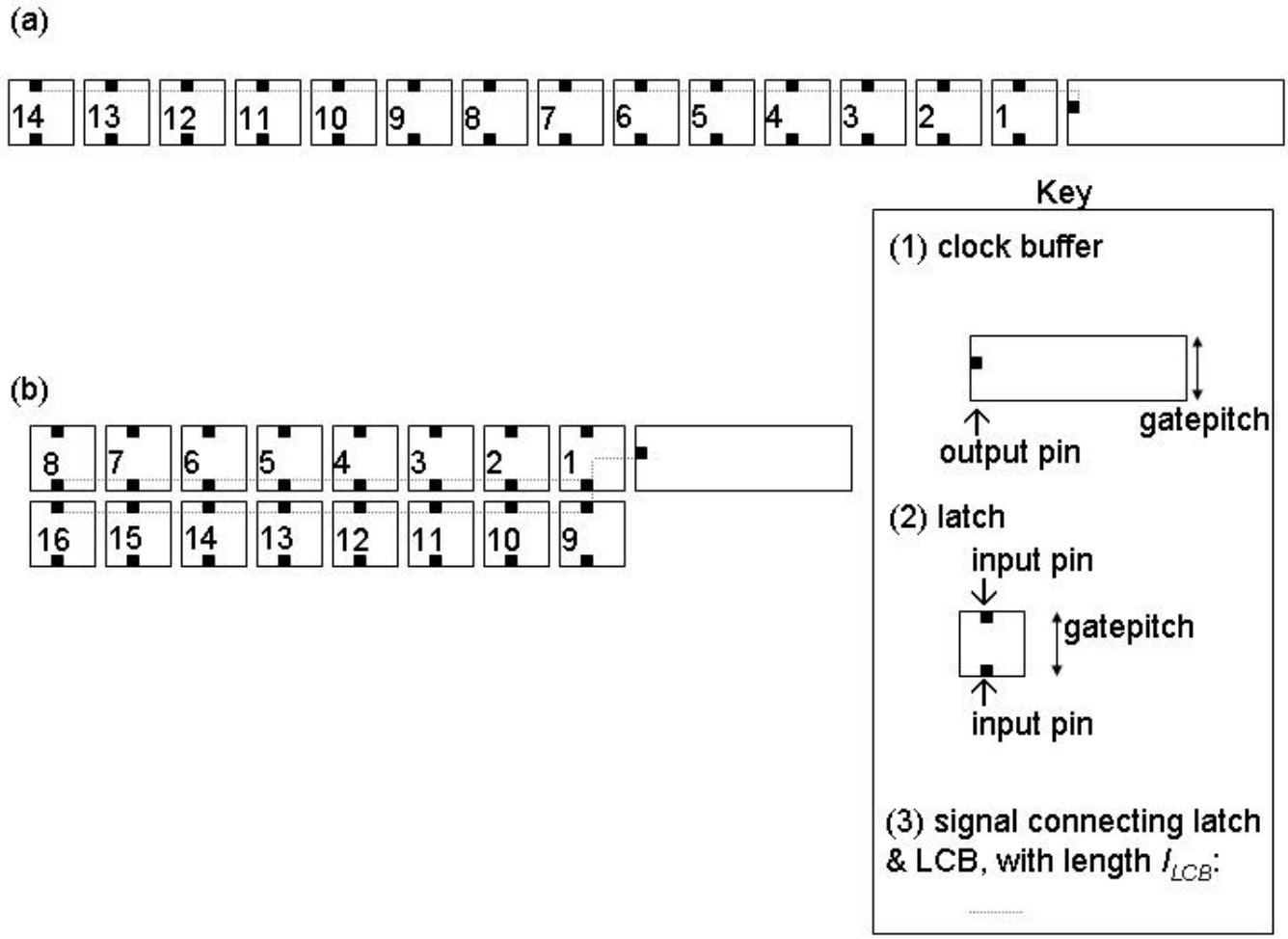

Fig. 6. Clock signal topologies in physical design. An example route length l_{LCB} for clock signals connecting latches is shown as dashed lines in (a) and (b), where the latches are stacked in single rows (a) and double rows (b) adjacent to the LCB. In control macro physical design, row placement of latches is typically more difficult than observed with clustering topologies shown in Fig. 5. The topologies shown in this figure are more typically used by designers who use manual intervention to place latches manually in custom physical designs.

TABLE I

NUMBER OF USED GATES N_{gates}^{synch}, AVERAGE FANOUT f NUMBER OF LCBS N_{LCB}, AND NUMBER OF SIGNALS $N_{synchsig}$ ASSOCIATED WITH CLOCKING CIRCUITRY IN IFU DESIGNS COMPARED WITH ESTIMATED NUMBER OF SIGNALS N_{synch} ASSOCIATED WITH SYNCHRONIZATION CIRCUITRY, WHERE $N_{synch} \sim 1 + N_{dc} + 2 \times N_{LCB}$ AND THE APPROXIMATION IS USED BECAUSE NOT ALL dc SIGNALS ARE INPUT INTO EACH LCB AND NOT ALL LCBS DRIVE TWO SIGNALS ASSOCIATED WITH THE CLOCKING CIRCUITRY.

design	N_{gates}^{synch}	f	N_{LCB}	N_{synch}	$N_{synchsig}$
i1	20	1.1	1	8	8
i4	48	4.9	3	12	10
i3	55	5.6	3	12	8
i2	61	6.6	4	14	19
i5	128	8.9	7	20	16
i7	158	7.8	11	28	47
i16	174	11.5	13	32	33
i8	182	11.0	11	28	21
i6	195	10.4	12	30	31
i10	197	11.7	11	28	20
i9	205	11.1	14	34	17
i11	261	11.9	18	42	19
i14	356	12.9	22	50	56
i12	377	12.8	24	54	58
i13	424	14.0	27	60	63
i15	436	13.9	27	60	61
i17	705	3.8	48	102	637
i18	852	14.4	52	110	118

TABLE II

VALUES FOR THE PARAMETER PAIR $\{k_R^{function}, p_R^{function}\}$ FOR EACH POWER UNIT OBTAINED BY FITTING THE DATA FOR SIGNALS NOT ASSOCIATED WITH THE DESIGN CLOCKING CIRCUITRY IN EACH UNIT IN FIG. 1(C) TO THE EXPRESSION $log(N_{conn}^{function}) = log(k_R^{function}) + p_R^{function} \times log(N_{gates}^{function})$.

unit	*macros*	$k_R^{function}$ *[range]*	$p_R^{function}$ *[range]*
ifu	18	$6.15[5.15, 7.33]$	$0.89[0.87, 0.92]$
fpu	12	$2.53[2.17, 2.96]$	$1.03[1.00, 1.06]$
fxu	4	$4.46[2.57, 7.73]$	$0.94[0.83, 1.05]$
idu	18	$2.58[1.19, 5.59]$	$1.02[0.91, 1.13]$
isu	16	$2.71[1.79, 4.12]$	$1.03[0.97, 1.09]$
lsu	32	$1.67[1.37, 2.04]$	$1.08[1.05, 1.10]$

TABLE III

TOTAL NUMBER OF GATES $N_{gates}^{function}$ NOT ASSOCIATED WITH CLOCKING CIRCUITRY, AVERAGE FANOUT f, ACTUAL NUMBER OF INTERCONNECTIONS $N_{conn}^{function}$ NOT ASSOCIATED WITH CLOCKING CIRCUITRY, AND PREDICTED NUMBER OF SIGNAL INTERCONNECTIONS $N(A_R^{function}, p_R^{function})$ NOT ASSOCIATED WITH CLOCKING CIRCUITRY, AND ERROR. HERE THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(N_{conn}^{function} - N(A_R^{function}, p_R^{function})) \times 100}{N(A_R^{function}, p_R^{function})}\%$. THE ERROR IS GIVEN IN %.

design	$N_{gates}^{function}$	f	$N_{conn}^{function}$	$N(A_R^{function}, p_R^{function})$ *[range]*	*Error*
i1	50	1.6	85	$65.7[65.1, 62.6]$	29
i2	159	1.6	299	$251.4[246.0, 242.8]$	19
i3	170	1.5	195	$267.0[261.1, 258.0]$	-27
i4	183	1.9	245	$314.7[307.5, 304.4]$	-22
i5	651	1.8	784	$1289.3[1244.2, 1263.5]$	-39
i6	769	1.7	965	$1501.4[1446.5, 1473.8]$	-36
i7	809	1.6	790	$1587.7[1528.9, 1559.3]$	-50
i9	848	1.5	909	$1618.2[1557.6, 1590.1]$	-44
i8	860	1.7	1030	$1753.0[1687.2, 1722.8]$	-41
i10	921	1.7	1127	$1860.7[1789.7, 1829.9]$	-39
i11	989	1.5	1011	$1916.3[1841.9, 1885.9]$	-47
i12	1946	1.7	2073	$4211.5[4022.8, 4172.6]$	-51
i13	2137	1.9	2224	$4883.6[4660.9, 4843.0]$	-54
i15	2310	1.7	2439	$5071.7[4837.0, 5033.3]$	-52
i14	2335	1.7	2302	$5131.1[4893.2, 5092.9]$	-55
i16	2697	2.0	3013	$6377.2[6073.7, 6338.5]$	-53
i17	4229	1.6	3728	$9579.1[9087.3, 9562.1]$	-61
i18	4607	1.6	4496	$10331.5[9793.9, 10321.6]$	-56

TABLE IV

MEASURED AVERAGE WIRELENGTH OF SIGNALS ASSOCIATED WITH FUNCTIONAL LOGIC IN IFU DESIGNS

$L_a^{function} = \frac{1}{N_{conn}^{function}} \sum_{i=1}^{N_{conn}^{function}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF THOSE SIGNAL INTERCONNECTIONS i THAT ARE NOT ASSOCIATED WITH CLOCKING CIRCUITRY. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R^{function})$) AND DONATH ($\overline{R}(p_R^{function})$) ARE ALSO SHOWN. THE ERROR FOR $L_{avg}(p_R^{function})$ IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_a^{function} - L_{avg}(p_R^{function}))\times 100}{L_{avg}(p_R^{function})}$. FOR $\overline{R}(p_R^{function})$, THE ERROR IS GIVEN BY $Error = \frac{(L_a^{function} - \overline{R}(p_R^{function}))\times 100}{\overline{R}(p_R^{function})}\%$. THE ERRORS ARE SHOWN IN %. NOTE THAT $L_a^{function}$, $L_{avg}(p_R^{function})$, AND $\overline{R}(p_R^{function})$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	$N_{gates}^{function}$	$L_a^{function}$	$L_{avg}(p_R^{function})$ [range]	Error	$\overline{R}(p_R^{function})$ [range]	Error
i1	50	3.2	2.5[2.52.5]	27	3.0[3.0, 3.1]	5
i2	159	4.8	3.4[3.33.5]	41	4.4[4.2, 4.5]	9
i3	170	3.1	3.4[3.33.5]	−9	4.4[4.3, 4.6]	−30
i4	183	3.5	3.5[3.43.6]	1	4.5[4.4, 4.7]	−22
i5	651	3.3	5.0[4.85.2]	−34	6.8[6.6, 7.1]	−52
i6	769	5.4	5.2[5.05.4]	3	7.2[6.9, 7.5]	−26
i7	809	4.6	5.3[5.15.5]	−13	7.3[7.0, 7.7]	−37
i9	848	4.1	5.4[5.15.6]	−23	7.5[7.1, 7.8]	−44
i8	860	3.5	5.4[5.25.6]	−36	7.5[7.2, 7.8]	−54
i10	921	3.1	5.5[5.35.8]	−44	7.7[7.3, 8.0]	−60
i11	989	3.5	5.6[5.45.9]	−37	7.8[7.5, 8.2]	−55
i12	1946	8.3	6.9[6.57.3]	21	9.8[9.3, 10.4]	−15
i13	2137	8.8	7.1[6.77.5]	24	10.1[9.6, 10.7]	−13
i15	2310	7.3	7.2[6.97.7]	1	10.4[9.8, 11.0]	−30
i14	2335	6.3	7.3[6.97.7]	−14	10.4[9.8, 11.0]	−40
i16	2697	10.0	7.6[7.28.0]	32	10.9[10.3, 11.6]	−8
i17	4229	7.5	8.7[8.29.3]	−14	12.7[11.9, 13.6]	−41
i18	4607	8.7	9.0[8.49.6]	−3	13.1[12.2, 14.0]	−33

TABLE V

MEASURED TOTAL WIRELENGTH $L_T^{function}$ OF SIGNALS NOT ASSOCIATED WITH CLOCKING CIRCUITRY IN IFU DESIGNS $L_T^{function} = \sum_{i=1}^{N_{conn}^{function}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF SIGNAL INTERCONNECTIONS i NOT ASSOCIATED WITH CLOCKING CIRCUITRY. ESTIMATES OF TOTAL WIRELENGTH OBTAINED BY MULTIPLYING $L_{avg}(p_R^{function})$ FROM THE DAVIS MODEL WITH THE ESTIMATED NUMBER OF INTERCONNECTIONS $N(A_R^{function}, p_R^{function})$ FROM THE DONATH MODEL. IN THIS CASE, THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_T^{function} - L_{avg}(p_R^{function}) \times N(A_R^{function}, p_R^{function})) \times 100}{L_{avg}(p_R^{function}) \times N(A_R^{function}, p_R^{function})}\%$. THE ERROR IS GIVEN IN %. NOTE THAT $L_T^{function}$ AND $L_{avg}(p_R^{function}) \times N(A_R^{function}, p_R^{function})$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	$N_{gates}^{function}$	$L_T^{function}$	$L_{avg}(p_R^{function}) \times N(A_R^{function}, p_R^{function})$ *[range]*	*Error*
i1	50	269.8	$164.6[161.9, 167.3]$	64
i2	159	1422.9	$847.2[825.8, 869.3]$	68
i3	170	747.4	$916.0[892.3, 940.5]$	-18
i4	183	869.1	$1101.1[1071.9, 1131.3]$	-21
i5	651	2572.4	$6420.3[6168.8, 6682.7]$	-60
i6	769	5389.9	$7844.5[7523.0, 8180.5]$	-31
i7	809	3829.7	$8418.4[8068.7, 8784.0]$	-55
i9	848	3937.7	$8698.7[8332.8, 9081.4]$	-55
i8	860	3582.2	$9461.9[9062.4, 9879.7]$	-62
i10	921	3463.3	$10245.9[9805.5, 10706.8]$	-66
i11	989	3700.5	$10774.5[10302.7, 11268.4]$	-66
i12	1946	17996.1	$28960.5[27464.5, 30536.6]$	-38
i13	2137	19503.3	$34546.2[32722.6, 36469.0]$	-44
i15	2310	18462.8	$36734.2[34760.4, 38816.8]$	-50
i14	2335	14925.3	$37286.4[35278.1, 39405.8]$	-60
i16	2697	30539.4	$48421.8[45728.2, 51268.3]$	-37
i17	4229	28957.7	$83548.1[78429.3, 88981.3]$	-65
i18	4607	39995.0	$92543.2[86772.0, 98674.2]$	-57

TABLE VI

ESTIMATES OF TOTAL WIRELENGTH OBTAINED BY MULTIPLYING $L_{avg}(p_R^{function})$ FROM THE DAVIS MODEL WITH THE ACTUAL NUMBER OF INTERCONNECTIONS $N_{conn}^{function}$ FROM THE DONATH MODEL. THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_T^{function} - L_{avg}(p_R^{function}) \times N_{conn}^{function}) \times 100}{L_{avg}(p_R^{function}) \times N_{conn}^{function}}\%$. THE ERROR IS GIVEN IN %. NOTE THAT $L_T^{function}$ AND $L_{avg}(p_R^{function}) \times N_{conn}^{function}$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	$N_{gates}^{function}$	$L_T^{function}$	$L_{avg}(p_R^{function}) \times N_{conn}^{function}$ [range]	Error
i1	50	269.8	213.0[209.6, 216.5]	27
i2	159	1422.9	1007.5[982.0, 1033.8]	41
i3	170	747.4	668.9[651.6, 686.8]	12
i4	183	869.1	857.1[834.4, 880.7]	1
i5	651	2572.4	3904.0[3751.1, 4063.6]	−34
i6	769	5389.9	5042.0[4835.3, 5257.9]	7
i7	809	3829.7	4188.8[4014.8, 4370.7]	−9
i9	848	3937.7	4886.2[4680.7, 5101.2]	−19
i8	860	3582.2	5559.4[5324.6, 5804.8]	−36
i10	921	3463.3	6205.7[5939.0, 6484.9]	−44
i11	989	3700.5	5684.3[5435.4, 5944.9]	−35
i12	1946	17996.1	14255.1[13518.8, 15030.9]	26
i13	2137	19503.3	15732.5[14902.1, 16608.2]	24
i15	2310	18462.8	17665.7[16716.5, 18667.2]	5
i14	2335	14925.3	16728.0[15827.0, 17678.8]	−11
i16	2697	30539.4	22877.7[21605.1, 24222.6]	33
i17	4229	28957.7	32515.5[30523.3, 34630.0]	−11
i18	4607	39995.0	40272.5[37761.0, 42940.5]	−1

TABLE VII

MEASURED TOTAL WIRELENGTH $L_T^{function}$ IN EACH UNIT OF THE POWER4 CHIP AND PREDICTED TOTAL WIRELENGTH L_{tot} (IN GATEPITCHES) FOR ALL SIGNALS NOT ASSOCIATED WITH THE CLOCKING CIRCUITRY WITH THE PARAMETER PAIR $\{k_R^{function}, p_R^{function}\}$, WHERE $L_{tot}(k_R^{function}, p_R^{function}) = \sum_{i=1}^{N_{conn}} L_{avg}(p_R^{function}) \times N_{conn}^{function}$ AND ERROR FOR ALL SIGNALS i IN EACH UNIT OF THE POWER4 CHIP, WHERE $N_{conn}^{function}$ IS THE TOTAL NUMBER OF SIGNAL INTERCONNECTIONS IN EACH UNIT NOT ASSOCIATED WITH CLOCKING CIRCUITRY. NOTE THAT $N_{conn}^{function}$ IS USED SINCE THE NUMBER OF INTERCONNECTIONS PREDICTED BY DONATH'S FORMULATION BECOMES ZERO FOR $p = 1$ AND BECOMES NEGATIVE FOR VALUES OF $p > 1$. THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_T^{function} - L_{tot}(p_R^{function})) \times 100}{L_{tot}(p_R^{function})}\%$. THE ERROR IS EXPRESSED IN %. NOTE THAT $L_T^{function}$ AND $L_{tot}(p_R^{function})$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

unit	N_{macros}	$L_T^{function}$	$L_{tot}(p_R^{function})$ *[range]*	*Error*
ifu	18	200164.4	$198263.9[187512.2, 209624.0]$	1
fpu	12	21805.1	$18848.4[18161.7, 19557.9]$	16
fxu	4	24634.4	$18626.0[14960.6, 23103.4]$	32
idu	18	140842.3	$188789.8[152420.7, 231605.0]$	-25
isu	16	286661.6	$350055.3[308689.3, 395308.6]$	-18
lsu	32	502571.6	$764213.6[720808.5, 809238.4]$	-34
core	$6units$	$1.17668E6$	$1.5388E6[1.40255E6, 1.68844E6]$	-24

TABLE VIII

ROUTE LENGTH l_{LCB} AS A FUNCTION OF THE CLUSTERING DISTANCE, l_c, AND RATIO OF LATCHES TO LCBS, N_{lat}/N_{LCB}, FOR CLOCK SIGNALS CONNECTING LATCHES CLUSTERED AROUND EACH LOCAL CLOCK BUFFER (LCB), WHERE l_{LCB} IS SHOWN FOR THREE DIFFERENT CLUSTER DISTANCES l_c (IN GATEPITCHES).

N_{lat}/N_{LCB}	l_{LCB} $(l_c = 0)$	l_{LCB} $(l_c = 1)$	l_{LCB} $(l_c = 2)$
	(gatepitches)	*(gatepitches)*	*(gatepitches)*
10	9	14.5	19
11	10	15.5	20
12	11	16.5	21
13	11	16.5	21
14	12	17.5	22
15	13	18.5	23
16	14	19.5	24

TABLE IX

NUMBER OF USED GATES, NUMBER OF LCBS, RATIO OF TOTAL NUMBER OF LATCHES TO THE TOTAL NUMBER OF LCBS, MEAN ROUTE LENGTH $\tilde{L}_{synch}$ AND STANDARD ERROR (SE) FOR SIGNALS ASSOCIATED WITH SYNCHRONIZATION CIRCUITRY IN IFU DESIGNS, WHERE $\tilde{L}_{clk}$ AND SE ARE OBTAINED FROM A GAUSSIAN FIT TO THE SIGNAL DISTRIBUTION ASSOCIATED WITH CLOCKING CIRCUITRY IN EACH DESIGN. FROM $\tilde{L}_{clk}$ AND TABLE VIII, $\tilde{l}_c$ CAN BE OBTAINED.

design	N_{gates}^{synch}	N_{LCB}	N_{lat}/N_{LCB}	$\tilde{L}_{synch}$ (se)	$\tilde{l}_c$
				(gatepitches)	*(gatepitches)*
i1	20	1	15.0	46 (0.2)	$<<1$
i4	48	3	13.7	178 (0.4)	1
i3	55	3	16.0	107 (0.3)	≤ 1
i2	61	4	12.3	18.5 (1.9)	≥ 1
i5	128	7	16.4	18.4 (1.2)	≤ 1
i7	158	11	13.0	12 (1.87)	≤ 1
i16	174	13	12.1	12.1 (1.4)	≥ 0
i8	182	11	15.0	199 (1.08)	≥ 1
i6	195	12	14.4	197 (6.2)	≥ 1
i10	197	11	16.4	18.5 (1.3)	≤ 1
i9	205	14	13.4	17.5 (1.13)	≥ 1
i11	261	18	13.3	187 (2.3)	≥ 1
i14	356	22	15.0	196 (4.3)	≥ 1
i12	377	24	14.5	186 (1.26)	1
i13	424	27	14.6	237 (7.4)	≥ 2
i15	436	27	15.0	213 (8.7)	≤ 2
i17	705	48	13.6	$--$ ($--$)	$--$
i18	852	52	15.3	21 (10.5)	≤ 2

TABLE X

TOTAL WIRE REQUIREMENTS L_T^{synch} FOR SIGNALS ASSOCIATED WITH CLOCKING CIRCUITRY, ESTIMATE OF TOTAL WIRE REQUIREMENT L_{tot}^{synch}, AND ERROR, FOR DESIGNS IN IFU. ALSO SHOWN ARE THE NUMBER OF GATES ASSOCIATED WITH CLOCKING CIRCUITRY N_{gates}^{synch}, TOTAL NUMBER OF GATES N_{gates}, NUMBER OF LCBS N_{LCB}, RATIO OF NUMBER OF LATCHES TO NUMBER OF LCBS N_{lat}/N_{LCB}, CLUSTERING PARAMETER $\tilde{l}_c$, WIRELENGTH l_{LCB} FOR EACH LCB SIGNAL. IN THIS CASE, THE ERROR IS GIVEN BY THE EXPRESSION, $Error = \frac{(L_T^{synch} - L_{tot}^{synch}) \times 100}{L_{tot}^{synch}}\%$. THE ERROR IS GIVEN IN %. ALL WIRELENGTHS ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	N_{gates}^{synch}	N_{gates}	N_{LCB}	N_{lat}/N_{LCB}	$\tilde{l}_c$	l_{LCB}	L_T^{synch}	L_{tot}^{synch}	Error
i1	20	70	1	15	1	16	35.7	116.8	−69
i4	48	231	3	13.7	1	15	142.1	245.4	−42
i3	55	225	3	16	1	17	100.2	255.4	−61
i2	61	220	4	12.3	1	14	322.9	264.8	22
i5	128	779	7	16.4	1	18	427.1	539.0	−21
i7	158	967	11	13	1	14	901.5	631.3	43
i16	174	2871	13	12.1	0	9.5	1005.2	797.4	26
i8	182	1042	11	15	1	16	678.9	687.2	−1
i6	195	964	12	14.4	1	16	828.4	708.0	17
i10	197	1118	11	16.4	1	18	677.4	742.7	−9
i9	205	1053	14	13.4	1	15	535.2	760.2	−30
i11	261	1250	18	13.3	1	15	612.4	913.8	−33
i14	356	2691	22	15	1	16	1629.8	1247.5	31
i12	377	2323	24	14.5	1	16	1798.8	1277.0	41
i13	424	2561	27	14.6	2	21.5	2262.7	1697.4	33
i15	436	2746	27	15	2	21.5	1855.8	1715.4	8
i17	705	4934	48	13.6	–	−−	9076.3	−−	−−
i18	852	5459	52	15.3	2	22.5	3772.3	3137.5	20

APPENDIX

This appendix contains tables with model estimates and actual data for all other units in the POWER4 core (FPU, FXU, IDU, ISU, LSU). The five tables show $L_a^{function}$, $L_{avg}(p_R^{function})$, and $\overline{R}(p_R^{function})$ (in units of gatepitches).

TABLE XI

MEASURED AVERAGE WIRELENGTH FOR FPU DESIGNS $L_a^{function} = \frac{1}{N_{conn}^{function}} \sum_{i=1}^{N_{conn}^{function}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R^{function})$) AND DONATH ($\overline{R}(p_R^{function})$) ARE ALSO SHOWN. FOR $L_{avg}(p_R^{function})$, THE ERROR IS GIVEN BY $\frac{(L_a^{function} - L_{avg}(p_R^{function})) \times 100}{L_{avg}(p_R^{function})}\%$. FOR $\overline{R}(p_R^{function})$, THE ERROR IS GIVEN BY $\frac{(L_a^{function} - \overline{R}(p_R^{function})) \times 100}{\overline{R}(p_R^{function})}\%$. THE ERROR IS GIVEN IN %. NOTE THAT $L_a^{function}$, $L_{avg}(p_R^{function})$, AND $\overline{R}(p_R^{function})$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	$N_{gates}^{function}$	$L_a^{function}$	$L_{avg}(p_R^{function})$	Error	$\overline{R}(p_R^{function})$	Error
f1	41	3.0	$2.6[2.5, 2.6]$	17	$3.0[3.0, 3.1]$	-1
f2	46	2.6	$2.7[2.6, 2.7]$	-4	$3.2[3.1, 3.2]$	-19
f3	133	4.4	$3.7[3.6, 3.8]$	20	$4.7[4.5, 4.8]$	-6
f5	176	4.0	$4.0[3.9, 4.1]$	-1	$5.2[5.0, 5.3]$	-23
f4	201	5.1	$4.2[4.1, 4.3]$	21	$5.4[5.3, 5.6]$	-6
f6	236	4.6	$4.4[4.3, 4.6]$	5	$5.8[5.6, 5.9]$	-20
f7	257	5.6	$4.5[4.4, 4.7]$	25	$5.9[5.8, 6.1]$	-5
f8	300	5.0	$4.8[4.6, 4.9]$	6	$6.3[6.1, 6.5]$	-20
f9	356	5.8	$5.0[4.9, 5.2]$	15	$6.7[6.5, 6.9]$	-14
f10	398	6.9	$5.2[5.0, 5.4]$	32	$7.0[6.8, 7.3]$	-1
f11	484	4.9	$5.6[5.4, 5.8]$	-13	$7.5[7.3, 7.8]$	-35
f12	555	7.1	$5.9[5.6, 6.1]$	22	$7.9[7.6, 8.3]$	-10

TABLE XII

MEASURED AVERAGE WIRELENGTH FOR FXU DESIGNS $L_a^{function} = \frac{1}{N_{conn}^{function}} \sum_{i=1}^{N_{conn}^{function}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R^{function})$) AND DONATH ($\overline{R}(p_R^{function})$) ARE ALSO SHOWN. FOR $L_{avg}(p_R^{function})$, THE ERROR IS GIVEN BY $\frac{(L_a^{function} - L_{avg}(p_R^{function})) \times 100}{L_{avg}(p_R^{function})}\%$. FOR $\overline{R}(p_R^{function})$, THE ERROR IS GIVEN BY $\frac{(L_a^{function} - \overline{R}(p_R^{function})) \times 100}{\overline{R}(p_R^{function})}\%$. THE ERROR IS GIVEN IN %. NOTE THAT $L_a^{function}$, $L_{avg}(p_R^{function})$, AND $\overline{R}(p_R^{function})$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	$N_{gates}^{function}$	$L_a^{function}$	$L_{avg}(p_R^{function})$ [range]	Error	$\overline{R}(p_R^{function})$ [range]	Error
x1	5	1.4	$1.5[1.5, 1.5]$	-10	$1.4[1.4, 1.4]$	-5
x2	10	3.5	$1.8[1.7, 1.8]$	100	$1.8[1.8, 1.9]$	93
x3	283	6.9	$4.2[3.6, 4.8]$	66	$5.5[4.8, 6.3]$	25
x4	1868	9.4	$7.5[6.0, 9.4]$	25	$10.7[8.4, 13.2]$	-12

TABLE XIII

MEASURED AVERAGE WIRELENGTH FOR IDU DESIGNS $L_a^{function} = \frac{1}{N_{conn}^{function}} \sum_{i=1}^{N_{conn}^{function}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R^{function})$) AND DONATH ($\overline{R}(p_R^{function})$) ARE ALSO SHOWN. FOR $L_{avg}(p_R^{function})$, THE ERROR IS GIVEN BY $\frac{(L_a^{function} - L_{avg}(p_R^{function})) \times 100}{L_{avg}(p_R^{function})}\%$. FOR $\overline{R}(p_R^{function})$, THE ERROR IS GIVEN BY $\frac{(L_a^{function} - \overline{R}(p_R^{function})) \times 100}{\overline{R}(p_R^{function})}\%$. THE ERROR IS GIVEN IN %. NOTE THAT $L_a^{function}$, $L_{avg}(p_R^{function})$, AND $\overline{R}(p_R^{function})$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	$N_{gates}^{function}$	$L_a^{function}$	$L_{avg}(p_R^{function})$	Error	$\overline{R}(p_R^{function})$	Error
d1	86	2.2	$3.2[2.9, 3.5]$	-29	$3.9[3.6, 4.3]$	-43
d2	206	3.6	$4.2[3.7, 4.7]$	-13	$5.4[4.8, 6.0]$	-33
d3	423	6.0	$5.3[4.5, 6.1]$	14	$7.1[6.1, 8.1]$	-15
d4	444	5.3	$5.3[4.6, 6.2]$	-2	$7.2[6.2, 8.2]$	-27
d5	493	2.7	$5.5[4.7, 6.5]$	-50	$7.5[6.4, 8.6]$	-63
d6	593	4.3	$5.9[5.0, 7.0]$	-27	$8.0[6.8, 9.3]$	-46
d7	755	5.3	$6.4[5.3, 7.6]$	-17	$8.8[7.4, 10.3]$	-40
d8	1115	7.5	$7.3[6.0, 8.9]$	3	$10.2[8.4, 12.1]$	-26
d9	1290	7.1	$7.7[6.2, 9.4]$	-8	$10.8[8.8, 12.9]$	-34
d10	1298	5.9	$7.7[6.3, 9.4]$	-24	$10.8[8.8, 12.9]$	-46
d11	1301	6.8	$7.7[6.3, 9.4]$	-12	$10.8[8.8, 12.9]$	-37
d12	1357	5.0	$7.8[6.3, 9.6]$	-36	$11.0[9.0, 13.2]$	-55
d13	1386	5.5	$7.9[6.4, 9.7]$	-30	$11.1[9.0, 13.3]$	-50
d14	1697	5.4	$8.5[6.8, 10.5]$	-37	$12.0[9.7, 14.5]$	-55
d15	1791	6.5	$8.7[6.9, 10.7]$	-25	$12.3[9.8, 14.8]$	-47
d16	2082	4.9	$9.1[7.2, 11.4]$	-46	$13.0[10.3, 15.8]$	-62
d17	2091	4.9	$9.2[7.2, 11.4]$	-46	$13.0[10.4, 15.9]$	-62
d18	2685	5.6	$10.0[7.8, 12.7]$	-44	$14.4[11.3, 17.7]$	-61

TABLE XIV

MEASURED AVERAGE WIRELENGTH FOR ISU DESIGNS $L_a^{function} = \frac{1}{N_{conn}^{function}} \sum_{i=1}^{N_{conn}^{function}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R^{function})$) AND DONATH ($\overline{R}(p_R^{function})$) ARE ALSO SHOWN. FOR $L_{avg}(p_R^{function})$, THE ERROR IS GIVEN BY $\frac{(L_a^{function} - L_{avg}(p_R^{function})) \times 100}{L_{avg}(p_R^{function})}\%$. FOR $\overline{R}(p_R^{function})$, THE ERROR IS GIVEN BY $\frac{(L_a^{function} - \overline{R}(p_R^{function})) \times 100}{\overline{R}(p_R^{function})}\%$. THE ERROR IS GIVEN IN %. NOTE THAT $L_a^{function}$, $L_{avg}(p_R^{function})$, AND $\overline{R}(p_R^{function})$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	$N_{gates}^{function}$	$L_a^{function}$	$L_{avg}(p_R^{function})$	Error	$\overline{R}(p_R^{function})$	Error
s1	246	3.5	$4.5[4.2, 4.8]$	-22	$5.8[5.5, 6.2]$	-41
s2	269	5.2	$4.6[4.3, 4.9]$	13	$6.0[5.7, 6.4]$	-14
s3	281	2.8	$4.7[4.3, 5.0]$	-39	$6.1[5.7, 6.5]$	-54
s4	533	4.5	$5.8[5.3, 6.3]$	-22	$7.8[7.2, 8.4]$	-42
s5	847	7.4	$6.8[6.1, 7.4]$	10	$9.3[8.5, 10.2]$	-20
s6	1019	6.3	$7.2[6.5, 8.0]$	-12	$10.0[9.1, 11.0]$	-37
s7	1081	5.7	$7.4[6.7, 8.2]$	-23	$10.3[9.3, 11.2]$	-44
s8	1459	5.2	$8.2[7.4, 9.1]$	-36	$11.5[10.4, 12.7]$	-55
s9	1521	7.7	$8.3[7.5, 9.3]$	-8	$11.7[10.5, 12.9]$	-34
s10	1552	7.0	$8.4[7.5, 9.4]$	-17	$11.8[10.6, 13.0]$	-41
s11	2004	6.4	$9.2[8.2, 10.3]$	-30	$13.1[11.7, 14.5]$	-51
s12	2103	7.5	$9.4[8.3, 10.5]$	-20	$13.3[11.9, 14.8]$	-44
s13	2745	8.5	$10.3[9.1, 11.7]$	-18	$14.8[13.1, 16.5]$	-43
s14	3408	10.8	$11.2[9.8, 12.7]$	-3	$16.1[14.2, 18.1]$	-33
s15	3458	4.0	$11.3[9.9, 12.8]$	-65	$16.2[14.3, 18.2]$	-75
s16	5496	12.3	$13.4[11.6, 15.4]$	-9	$19.6[17.1, 22.2]$	-37

TABLE XV

MEASURED AVERAGE WIRELENGTH FOR LSU DESIGNS $L_a^{function} = \frac{1}{N_{conn}^{function}} \sum_{i=1}^{N_{conn}^{function}} L_i$, WHERE THE SUM IS TAKEN OVER THE MEASURED LENGTH L_i OF ALL INTERCONNECTIONS i IN THE DESIGN. ESTIMATES OF AVERAGE WIRELENGTH OBTAINED WITH MODELS BY DAVIS ($L_{avg}(p_R^{function})$) AND DONATH ($\overline{R}(p_R^{function})$) ARE ALSO SHOWN. FOR $L_{avg}(p_R^{function})$, THE ERROR IS GIVEN BY $\frac{(L_a^{function} - L_{avg}(p_R^{function}))\times 100}{L_{avg}(p_R^{function})}\%$. FOR $\overline{R}(p_R^{function})$, THE ERROR IS GIVEN BY $\frac{(L_a^{function} - \overline{R}(p_R^{function}))\times 100}{\overline{R}(p_R^{function})}\%$. THE ERROR IS GIVEN IN %. NOTE THAT $L_a^{function}$, $L_{avg}(p_R^{function})$, AND $\overline{R}(p_R^{function})$ ARE EXPRESSED IN UNITS OF GATEPITCHES.

design	$N_{gates}^{function}$	$L_a^{function}$	$L_{avg}(p_R^{function})$	Error	$\overline{R}(p_R^{function})$	Error
l1	90	1.9	3.4[3.3, 3.5]	−44	4.2[4.1, 4.3]	−54
l2	205	6.1	4.4[4.3, 4.6]	38	5.7[5.6, 5.9]	7
l3	235	6.3	4.6[4.5, 4.8]	35	6.0[5.8, 6.2]	4
l4	401	5.4	5.6[5.4, 5.8]	−3	7.4[7.2, 7.7]	−27
l5	457	5.7	5.8[5.6, 6.1]	−3	7.8[7.5, 8.1]	−27
l6	502	5.3	6.0[5.8, 6.3]	−12	8.1[7.8, 8.4]	−34
l7	584	5.5	6.4[6.1, 6.6]	−14	8.6[8.3, 8.9]	−36
l8	825	4.8	7.2[6.9, 7.5]	−33	9.9[9.5, 10.3]	−52
l9	835	5.0	7.3[6.9, 7.6]	−32	9.9[9.5, 10.3]	−50
l10	1014	4.7	7.8[7.4, 8.2]	−40	10.7[10.3, 11.2]	−56
l11	1055	4.9	7.9[7.6, 8.3]	−37	10.9[10.4, 11.4]	−55
l12	1200	5.4	8.3[7.9, 8.7]	−35	11.5[11.0, 12.0]	−53
l13	1291	5.5	8.5[8.1, 9.0]	−35	11.8[11.3, 12.4]	−53
l14	1375	9.4	8.7[8.3, 9.2]	8	12.2[11.6, 12.7]	−22
l15	1396	6.5	8.8[8.4, 9.2]	−26	12.2[11.7, 12.8]	−47
l16	1466	8.9	9.0[8.5, 9.4]	−1	12.5[11.9, 13.0]	−29
l17	1516	6.1	9.1[8.6, 9.5]	−33	12.6[12.1, 13.2]	−52
l18	1600	8.5	9.3[8.8, 9.7]	−8	12.9[12.3, 13.5]	−34
l19	1637	9.7	9.3[8.9, 9.8]	4	13.1[12.5, 13.7]	−26
l20	1847	4.4	9.8[9.3, 10.3]	−55	13.7[13.1, 14.4]	−68
l21	1874	7.8	9.8[9.3, 10.4]	−20	13.8[13.2, 14.5]	−43
l22	1947	10.2	10.0[9.5, 10.5]	2	14.0[13.4, 14.7]	−27
l23	1988	5.1	10.1[9.5, 10.6]	−49	14.1[13.5, 14.8]	−64
l24	2027	7.6	10.1[9.6, 10.7]	−25	14.3[13.6, 14.9]	−47
l25	2180	6.6	10.4[9.9, 11.0]	−36	14.7[14.0, 15.4]	−55
l26	3000	7.0	11.8[11.1, 12.5]	−40	16.8[15.9, 17.6]	−58
l27	3061	10.7	11.9[11.2, 12.6]	−10	16.9[16.0, 17.8]	−36
l28	3140	8.1	12.0[11.3, 12.7]	−33	17.1[16.2, 18.0]	−53

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