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Laterally-Scaled $Si/Si_{0.7}Ge_{0.3}$ n-MODFETs with $f_{max} \geq$ 200 GHz and Low Operating Bias

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ABSTRACT

We report on the dc and rf characterization of laterally-scaled, Si/SiGe n-MODFETs. Devices with L_g = 80 nm and L_{ds} = 300 nm had f_T = 80 GHz and f_{max} = 210 GHz. Separate devices with L_g = 70 nm also had f_T values as high as 92 GHz. The MODFETs displayed enhanced f_T at reduced drain-to-source voltage, V_{ds}, compared to Si MOSFETs with similar f_T at high V_{ds}.

Index Terms: Silicon germanium, high mobility, MODFET

I. INTRODUCTION

SiGe MODFETs are attractive devices for future rf and mixed-signal communications applications, where low cost and compatibility with CMOS logic circuits are required. MODFETs offer the potential for high-speed [1] and low-power operation [2], as well as low noise [3] both at high and low frequencies. In the past, MODFETs have demonstrated performance improvement compared to Si MOSFETs with similar gate lengths [4]-[5]. Recently, however, Si MOSFET scaling has outpaced that of MODFETs. Si MOSFETs with gate lengths < 10 nm [6] and f_T over 200 GHz have been reported [7], while it has only been recently that sub-100 nm gate-length SiGe MODFETS have been demonstrated [8]-[10]. In this paper, we report on the dc and rf results of $Si/Si_{0.7}Ge_{0.3}$ n-MODFETs with gate lengths as small as 70 nm. The devices display record f_T and f_{max} values for SiGe MODFETs, including f_{max} values over 200 GHz, and show enhanced rf operation at low drain-to-source voltage compared to MOSFETs with similar f_T at high drain bias.

II. DEVICE FABRICATION

The modulation-doped heterostructure used in this work was grown on an 8" Si wafer by ultra-high vacuum chemical vapor deposition (UHV-CVD). The as-grown layer structure consisted of a relaxed $Si_{1-x}Ge_x$ buffer layer, step-graded from $x = 0$ to a constant Ge composition of $x = 0.3$, a 9 nm strained Si quantum well, a 5 nm $Si_{0.7}Ge_{0.3}$ spacer layer, an 8 nm phosphorous-doped n-type $Si_{0.7}Ge_{0.3}$ supply layer and finally a 2 nm n-Si capping layer. The room-temperature electron sheet density was 2.2×10^{12} cm^{-2}, with a corresponding Hall mobility of 1700 cm^2/Vs.

A schematic cross-sectional diagram of the device structure is shown in Fig. 1. The fabrication started with the formation of SiO_2-filled shallow-trench isolation regions. Next, resist openings were patterned, and after a Ge pre-amorphization implant, phosphorous ions were implanted with a dose of 5 x 10^{15} cm^{-2} and an energy of 12 keV. The implants were then activated by rapid thermal annealing at 700 ^{o}C for 1 minute. The drain-to-source spacing, L_{ds}, defined as the distance between the drain and source implants, was kept at a constant value of 300 nm. Next, non-self-aligned silicide regions were formed by depositing SiO_2 and TiN, patterning resist and then etching the TiN in the patterned regions. Then, 12 nm of Ni and 20 nm of TiN were sputtered deposited and annealed at 500 ^{o}C for 1 minute. The unreacted Ni, as well as the TiN, were then removed using a selective etch. The NiSi regions were configured such that they were offset by 100 nm from the edge of the source and drain implants. After defining electron-beam alignment marks, T-shaped gates were formed by using electron-beam lithography to pattern PMMA/P(MMA/MAA) dual layer resist, followed by evaporation and lift off Ir/Ti/Au (20/20/240 nm) metal. Devices with gate lengths, L_g, ranging between 70 and 100 nm were fabricated. The top of the T-gate was kept at a constant width of 400 nm. The gate was not self-aligned to the source and drain, but no performance degradation was observed to result from minor misalignments. Finally, the process was completed by patterning and lifting off Ti/Au (20/350 nm) pad metallization.

III. DC CHARACTERISTICS

The dc output characteristics of a typical MODFET with L_g = 80 nm and L_{ds} = 300 nm are shown in Fig. 2. At a drain-to-source bias, V_{ds}, of +1 V, the device had a peak transconductance, g_m, of 286 mS/mm. The corresponding output conductance, g_d, was 48 mS/mm, leading to a dc

voltage gain, $A_v \equiv g_m/g_d$, of 6.0. The relatively high output conductance of these devices is due to the fact that no p-well doping was utilized. Significant improvement in A_v is expected by using a buried p-well layer, which can suppress the deep source-to-drain leakage current without degrading the channel mobility [11]. The gate leakage in these devices, on the other had, was very low. Despite the proximity of the gate to the source and drain implants, the gate current, I_g, at V_{ds} = +1 V was 43 μA/mm at V_g = -1 V and only 1.2 μA/mm at V_{gs} = -0.02 V, the gate bias for peak g_m.

IV. RF CHARACTERISTICS

The rf characteristics were measured using devices configured in a two-finger pi-geometry, with total gate width, W_g, of either 20 μm or 40 μm. An optimized gate pad geometry was used to eliminate resistance arising from the overlap of the pad metal with the T-gate metal [9]. S-parameter measurements were performed using an HP8510C network parameter analyzer, on both the active devices as well as open-circuit and short-circuit geometries. After *y*- and *z*-parameter de-embedding, the f_T and f_{max} values were determined by -20 dB/dec extrapolation of $|h_{21}|^2$ and Mason's unilateral gain, MUG, respectively.

The results of the s-parameter analysis described above are shown in Fig. 3(a) for a 20 μm-wide device with L_g = 80 nm and L_{ds} = 300 nm. The bias voltages were V_{gs} = -0.1 V and V_{ds} = +1.8 V. The devices showed nearly ideal roll off behavior for both $|h_{21}|^2$ and MUG, and extrapolated values of f_T = 80 GHz and f_{max} = 210 GHz were determined. To our knowledge, this is the first reported demonstration of a SiGe MODFET with f_{max} over 200 GHz. The drain bias dependence of f_T and f_{max} is shown in Fig. 3(b). Both f_T and f_{max} remain high at reduced drain bias; for instance, at V_{ds} = +0.4 V, the extrapolated f_T and f_{max} values were 71 GHz and 143

GHz, respectively. The gate resistance was an important factor in achieving high f_{max}. For the device shown in Fig. 3(a), R_g was only 2 Ω, while previous devices with R_g = 6 Ω, also shown in Fig. 3(b), had f_{max} of only 175 GHz [9].

The RF measurement results for devices with L_g = 70 nm are shown in Fig. 4. At bias conditions of V_{gs} = 0 and V_{ds} = +1 V, the device with W_g = 20 μm produced f_T and f_{max} values of 90 GHz and 185 GHz, respectively. At V_{ds} = +1.8 V, f_{max} increased to 200 GHz, while f_T dropped to 85 GHz. The f_T increase compared to L_g = 80 nm is attributed to the reduced gate capacitance, while the reduced f_{max} is likely due to the higher g_d at short gate length. The figure also shows the results for 70 nm gate-length devices with W_g = 40 μm. At V_{gs} = 0 and V_{ds} = +1 V, these devices had slightly higher f_T of 92 GHz, but f_{max} decreased to 150 GHz, a direct result of the increased gate resistance in the wider device.

The 40 μm-wide devices described above were analyzed further to compare the bias-dependence of f_T with Si MOSFETs. The MOSFETs used for this study were partially-depleted SOI MOSFETs with W_g = 16.8 μm and L_{poly} = 0.13 μm. This gate length was chosen because it produced devices with an f_T similar to that of the MODFETs at V_{ds} = +1 V. A plot of f_T vs. V_{ds} for the two devices is shown in Fig. 5. The plot shows that at reduced V_{ds}, the MODFET produced significantly higher f_T than the MOSFET. While the MODFET had only a 5% higher f_T at V_{ds} = +1 V, at V_{ds} = +0.25 V, the MODFET f_T was 30% higher, and at V_{ds} = +0.1 V, the improvement increased to 50%.

V. DISCUSSION AND CONCLUSIONS

The results described in this paper represent the first demonstration of SiGe MODFETs with f_{max} over 200 GHz, and further demonstrate the potential of utilizing the high mobility that MODFETs offer for enhanced performance at low voltages. The results suggest that the observed f_T improvement compared to Si MOSFETs at low drain bias is a direct result of the higher channel mobility, since MODFETs are predicted to reach velocity saturation at a lower lateral electric field [12]. However, the MODFET results reported here still fall short of the best Si MOSFET results [7], suggesting that considerable improvement of the MODFET device design is possible. Previous simulation results confirm this [13], and indicate that in order to achieve enhanced performance with reduced gate lengths, the MODFET layer structure needs to be scaled vertically. A shallower quantum well will reduce the effect of fringing capacitance effects that can degrade f_T, and reduce the drain impact on the channel potential which leads to high output conductance. The low gate current of the present devices indicate that further vertical scaling of the layer structure should be possible before the gate-leakage limit is ultimately reached. In addition, the utilization of p-well doping, or a buried insulating layer [11] will also be useful to control output conductance and off-state leakage, and allow L_{ds} to be further reduced to minimize series resistance.

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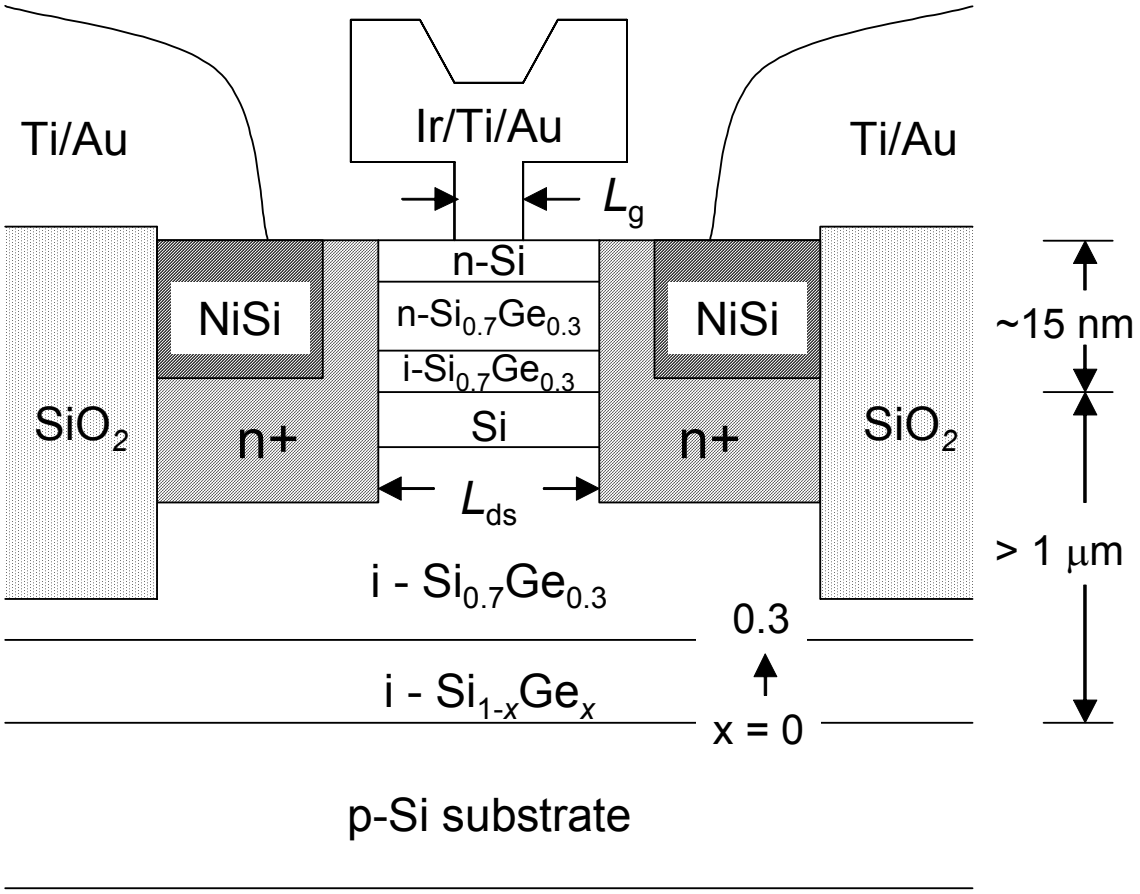

Figure 1. Cross-sectional diagram of the completed Si/SiGe n-MODFET device structure.

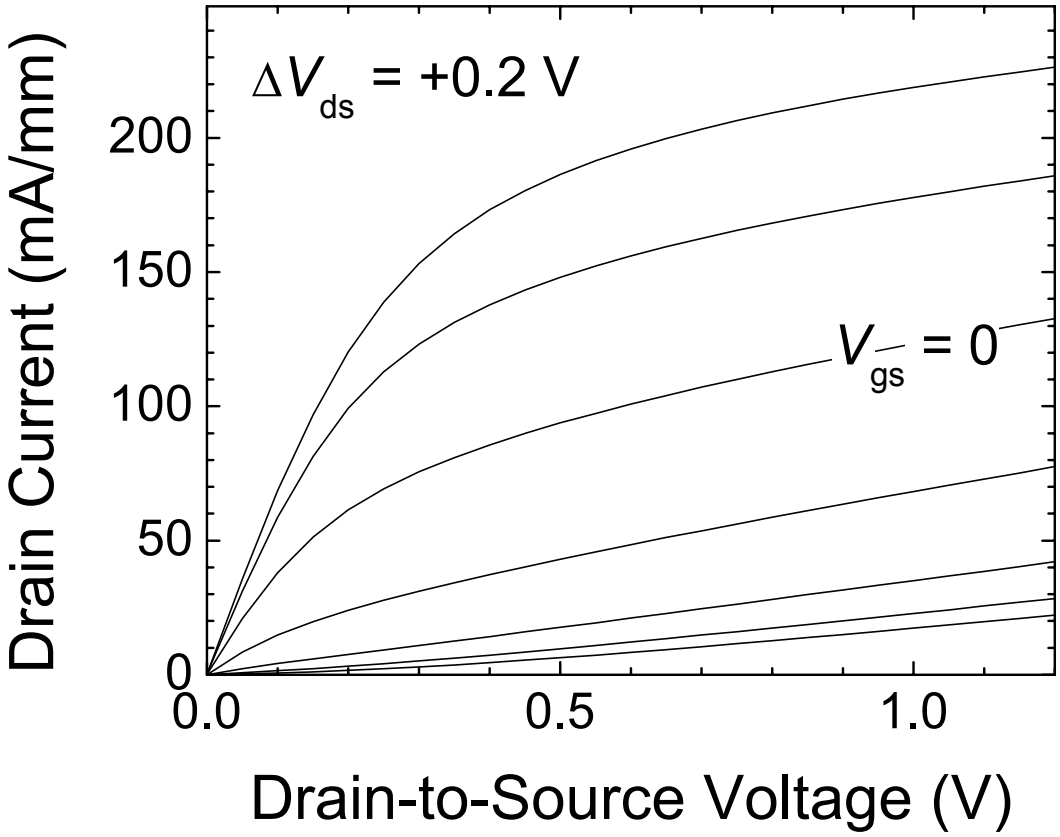

Figure 2. Output characteristic of a Si/SiGe n-MODFET with L_g = 80 nm.

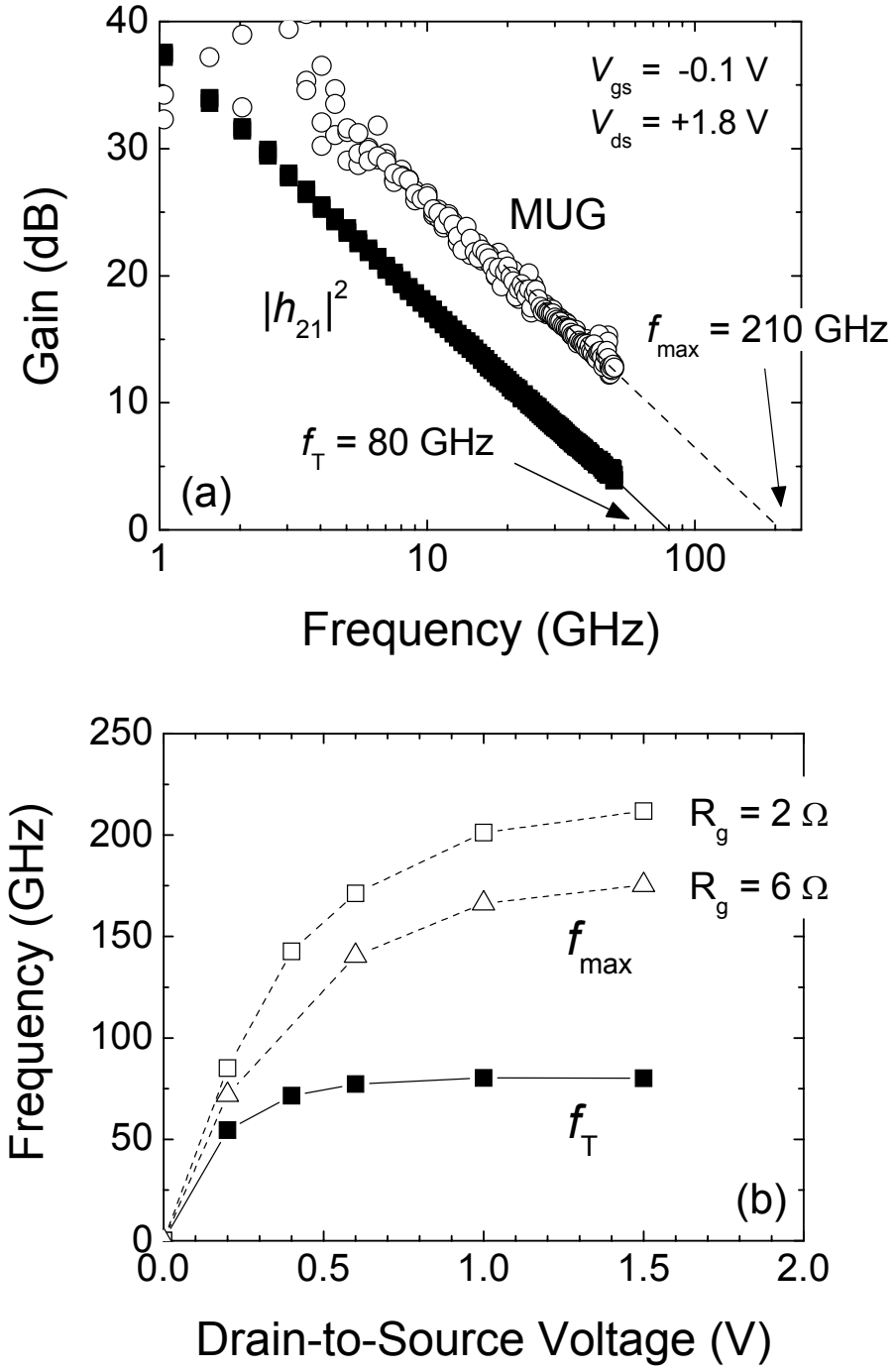

Figure 3. (a) De-embedded $|h_{21}|^2$ and MUG plotted vs. frequency for a Si/SiGe n-MODFET with L_g = 80 nm and W_g = 20 μm. (b) Squares: plot of f_T and f_{max} vs. V_{ds} for same device as in (a) with gate resistance, R_g, of 2 Ω. Triangles: f_{max} vs. V_{ds} for similar devices with R_g = 6 Ω.

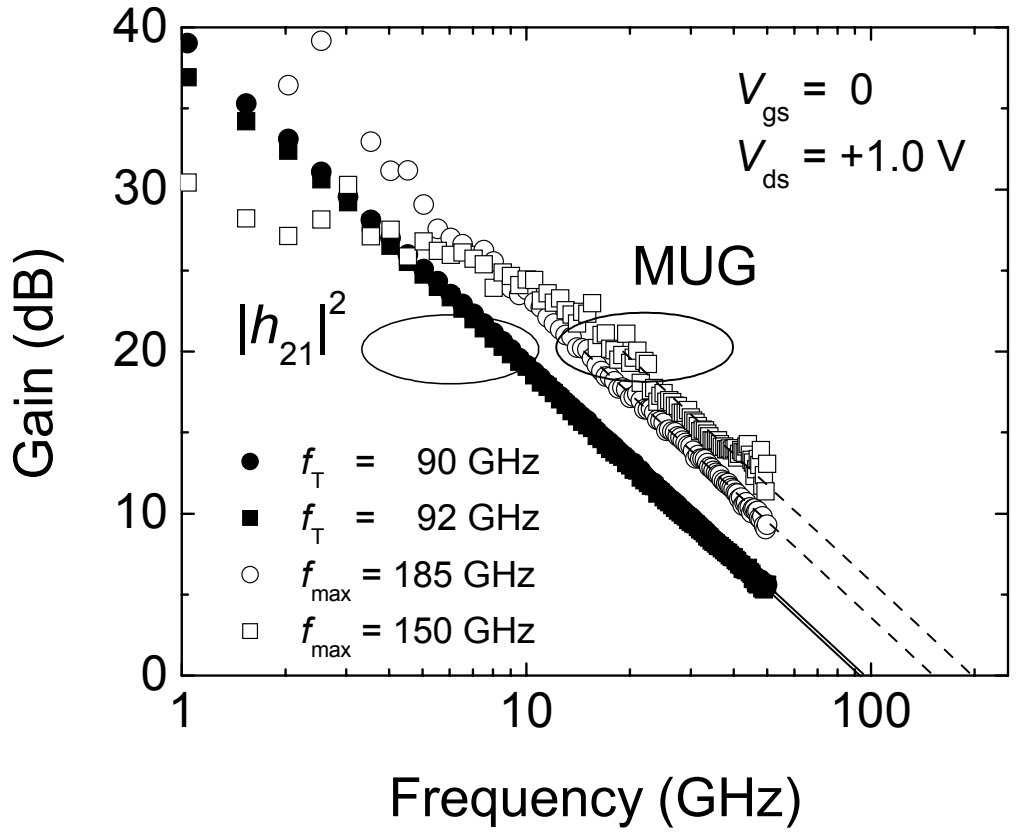

Figure 4. De-embedded $|h_{21}|^2$ and MUG vs. frequency for a Si/SiGe n-MODFET with L_g = 70 nm and W_g = 20 μm (circles) and 40 μm (squares). The extrapolated f_T and f_{max} values are indicated in the legend.

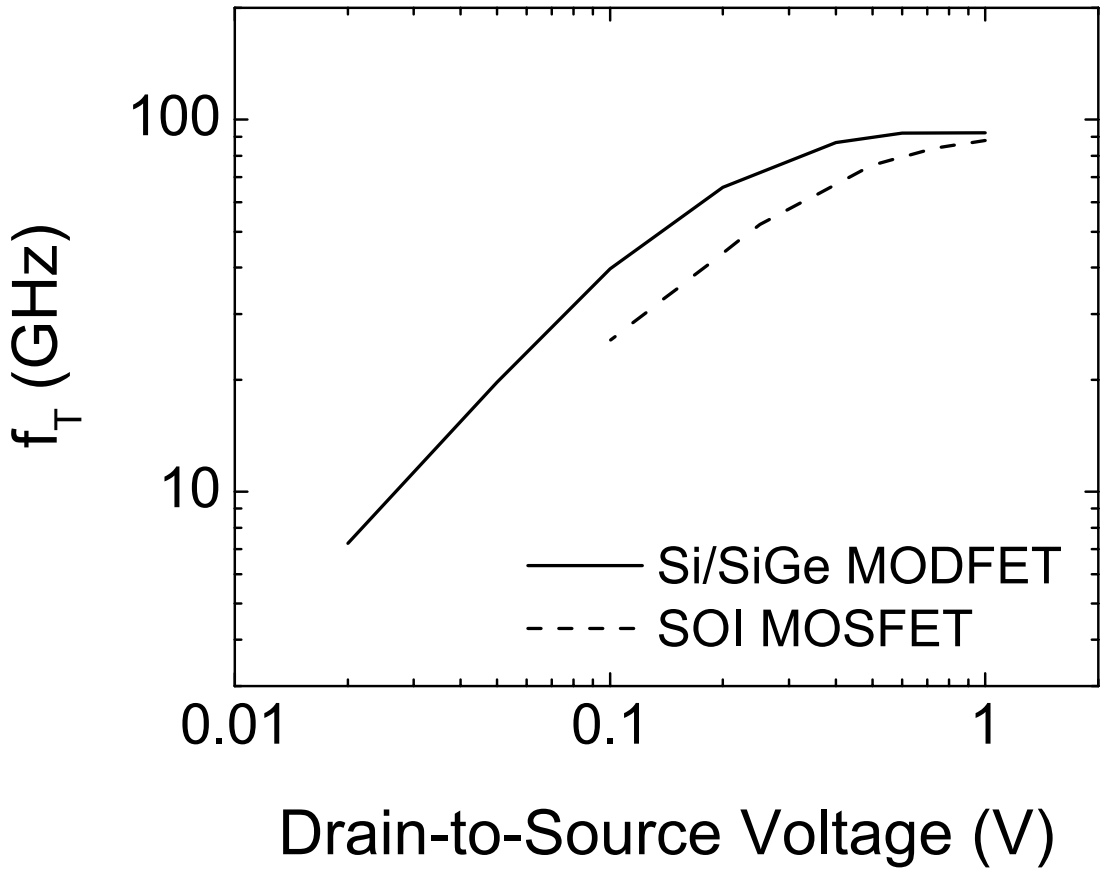

Figure 5. Log-log plot of f_T vs. V_{ds} for a Si/SiGe n-MODFET (solid line) and an SOI Si MOSFET (dashed line).