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K. L. Saenger, J. P. de Souza, K. E. Fogel, J. A. Ott, A. Reznicek, C.-Y. Sung, H. Yin*, D. K. Sadana
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

*IBM Semiconductor Research and Development Center
Microelectronics Division
Hopewell Junction, NY 12533

Research Division
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Amorphization/templated recrystallization (ATR) methods for hybrid orientation substrates

K.L. Saenger[1], J.P. de Souza[1], K.E. Fogel[1], J.A. Ott[1], A. Reznicek[1], C.Y. Sung[1], H. Yin[2], and D.K. Sadana[1]
[1]IBM Semiconductor Research and Development Center, T. J. Watson Research Center, Yorktown Heights, NY 10598
[2]IBM Semiconductor Research and Development Center Microelectronic Division, Hopewell Junction, NY 12533

ABSTRACT

Hybrid orientation substrates make it possible to have a CMOS technology in which nFETs are on (100) Si (the Si orientation in which electron mobility is the highest) and pFETs are on (110)-oriented Si (the Si orientation in which hole mobility is the highest). This talk will describe a new amorphization/templated recrystallization (ATR) method for fabricating bulk hybrid orientation substrates. In a preferred version of this method, a silicon layer with a (110) orientation is directly bonded to a Si base substrate with a (100) orientation. Si regions selected for an orientation change are amorphized by ion implantation and then recrystallized to the (100) orientation of the base substrate. After an overview of the ATR technique and its various implementations, we will describe some of the scientifically interesting materials and integration challenges encountered while reducing it to practice.

INTRODUCTION

The desire for improved CMOS device performance coupled with concerns about the limits of scaling is driving renewed interest in new materials (e.g., high-k gate dielectrics and metal gates) and structural variations of old materials (e.g., hybrid orientation substrates and strained Si) for field effect transistors (FETs). Hybrid orientation substrates, generally comprising a set of first semiconductor regions with a first crystal orientation and a second set of semiconductor regions with a second crystal orientation, are of interest because they allow a CMOS technology in which nFETs are on (100) Si (the Si orientation in which electron mobility is the highest) and pFETs are on (110)-oriented Si (the Si orientation in which hole mobility is the highest).

Hybrid orientation substrates have previously been fabricated with a bonding/epitaxial growth method in which regions of a bonded layer of Si having a first orientation are etched away and then replaced with epitaxially-grown Si having a second orientation matching that of the underlying Si substrate [1,2]. This paper describes an alternative amorphization/templated recrystallization (ATR) method for fabricating bulk hybrid orientation substrates [3], in which a silicon layer with a first orientation is directly bonded to a Si base substrate with a second orientation to form a direct-silicon-bonded (DSB) wafer. Regions in the bonded DSB layer selected for an orientation change are amorphized by ion implantation and then recrystallized to the orientation of the base substrate.

After illustrating the basic feasibility of the ATR method and showing examples of some simple integration schemes, we will describe a selection of the scientifically interesting materials and integration challenges encountered while reducing the method to practice. Particular attention will be directed towards problems and progress in three areas: initial substrate preparation; the quality of the changed-orientation ATR'd material; and "edge defects" associated with patterned ATR. Experimental details not included in the next section will be introduced in the individual topic sections as needed.

EXPERIMENTAL DETAILS

Amorphization for ATR was effected by ion implantation of Si^+ or Ge^+ ions, with the energy and dose selected to insure complete amorphization from the substrate's top surface to a depth below the DSB interface. All implants utilized a 7° tilt (to minimize channeling effects) and 10 ^{o}C substrate cooling. The thicknesses of the amorphized layer and the highly damaged crystalline layer just below it (located at the end-of-range (e-o-r) of the implanted ions) were determined by cross-section scanning electron microscopy (SEM) on Cr-coated samples Secco-etched after cleaving.

Templated recrystallization was typically performed at temperatures between 650 and 900 ^{o}C for times ranging from 1 to 10 min, though additional defect removal anneals (at 1300 to 1325 ^{o}C for 3 to 5 hours) were also performed after deposition of protective oxide capping layers. Plan view SEM (after Secco etching) was used to evaluate areal defect densities and to identify defective regions at the edges of patterned ATR'd regions. Cross section transmission electron microscopy (XTEM) was used to examine the samples at various stages of processing, with microdiffraction used to verify the expected Si orientation.

ATR: BASIC METHOD AND INTEGRATION SCHEMES

The basic ATR technique is shown schematically in Fig. 1. The starting DSB substrate (Fig. 1a) comprises a handle Si wafer of a first orientation (j'k'l') and a DSB Si device layer of a second orientation (jkl). The DSB layer is amorphized by ion implantation (I/I) to create an amorphous Si (a-Si) layer extending from the substrate surface down to a depth below the bonded interface (Fig. 1b), and then recrystallized to the orientation of the underlying handle wafer (Fig. 1c). For convenience, we will designate wafers with (110) DSB layers on (100) substrates as DSB-A, and wafers with (100) DSB layers on (110) substrates DSB-B.

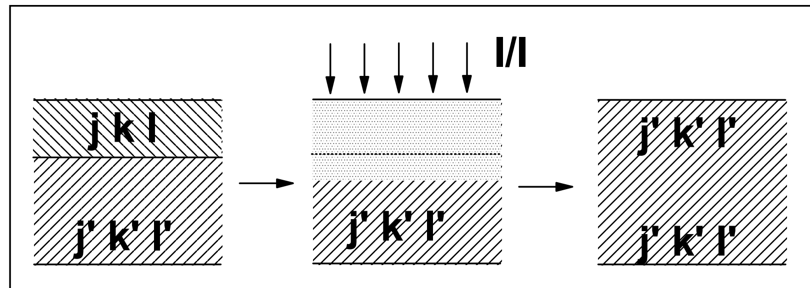

Figure 1. A schematic of the basic ATR technique.

Fabrication of hybrid orientation substrates requires Si orientation changes in selected regions only (i.e., patterned ATR vs. the maskless ATR of Fig. 1). Fig. 2 shows two versions of

patterned ATR. In the first, the ATR is performed without shallow trench isolation (STI). In the second, the ATR is performed after STI formation. A priori, the ATR-with-STI version might appear preferable because the trenches provide alignment marks (a necessity, since the differently-oriented Si regions are optically indistinguishable) and eliminate the possibility of lateral templating.

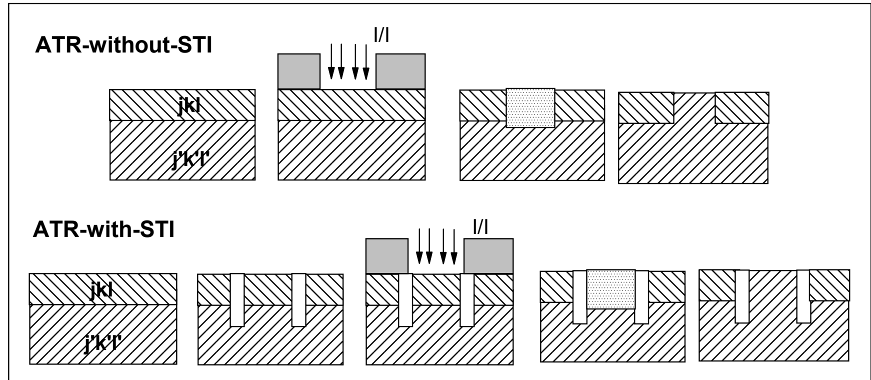

Figure 2. Two versions of patterned ATR.

INITIAL REDUCTION TO PRACTICE

We have performed blanket ATR to achieve both (110)-to-(100) and (100)-to-(110) conversions in DSB-A and DSB-B wafers respectively. The DSB-A conversion is illustrated in the Fig. 3 with XTEM images of a 50 nm-thick (110)-oriented DSB overlayer on a (100)-oriented Si substrate before (a) and after (b) a blanket ATR process that changed the DSB layer orientation to (100). In this case the amorphization implant was 2.0 x 10^{15} /cm^2 220 keV Ge^+ and the recrystallization anneal was at 900 ^oC for 1 min. No sign of the bonded interface remains after ATR. As will be discussed in more detail later, the ATR'd Si is relatively free of defects, though a band of dislocation loops remains at the position of the end-of-range (e-o-r) damage layer.

The XTEM images of Fig. 4 show the results for selected-area ATR on substrates patterned with oxide-filled trenches using the ATR-with-STI integration scheme of Fig. 2. Fig. 4(a) shows the substrate after a region of the 200 nm-thick (110) DSB layer to the left of the STI has been amorphized by an implant of 2.5 x 10^{15} /cm^2 120 keV Si^+, and Fig. 4(b) shows the

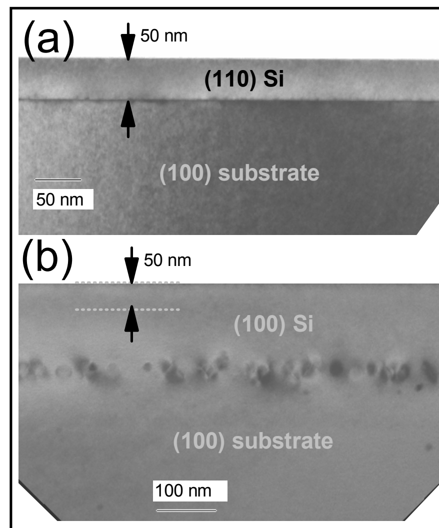

Figure 3. XTEM images showing the (110)-to-(100) orientation change of a 50-nm-thick Si layer on a (100)-oriented Si substrate: before ATR, (a); after ATR, (b).

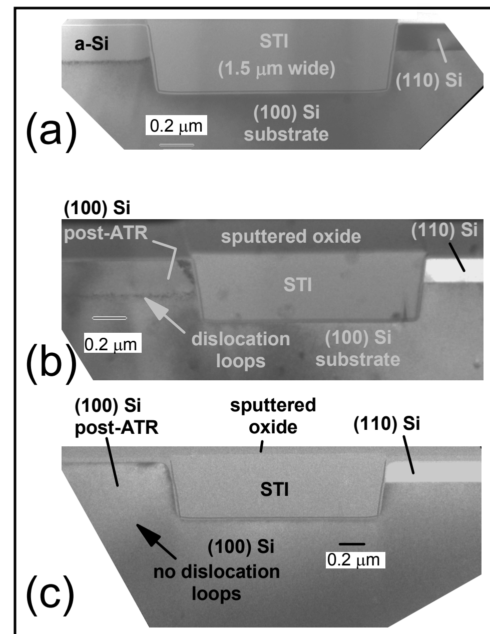

Figure 4. XTEM images showing the selected area (110)-to-(100) orientation change of a 200-nm-thick DSB layer on a (100)-oriented Si substrate.

substrate after the amorphized region has undergone a templated recrystallization to the (100) orientation of the underlying handle wafer by an anneal at 650 ^{o}C for 5 min. Clearly visible are the e-o-r damage layer at the amorphous/crystalline boundary in Fig. 4(a), and the resulting band of dislocation loops in Fig. 4(b). As will be discussed below, these damage regions may be removed by high-temperature annealing, as shown in Fig. 4(c). As expected, DSB regions to the right of the STI remain with the original (110) orientation.

MATERIALS AND INTEGRATION ISSUES

Substrate Preparation

Si wafer bonding techniques are generally either hydrophobic (in which H-terminated surfaces are bonded) or hydrophilic (in which OH-terminated, oxide-like surfaces are bonded). Hydrophilic bonding is now a mature technology, in large part due to industry demand for silicon-on-insulator (SOI) wafers. These SOI wafers typically comprise a Si layer disposed on a buried oxide (box) layer, with the box layer thickness being determined by the amount of surface oxide on the two starting wafers.

The desired box layer thickness for DSB wafers subjected to orientation-changing ATR is zero. In principle, such wafers would best be fabricated by hydrophobic bonding. However, hydrophobic bonding techniques are both more difficult (in part due to the propensity of H-terminated surfaces to attract particulates that interfere with bonding) and less commonly practiced (since they are not needed for SOI wafers).

For reasons that will become apparent in the next section, most of our work has been with DSB-A wafers. These DSB-A wafers, with DSB layers 50 to 200 nm in thickness, were typically purchased from vendors. However, our first demonstration of ATR-induced orientation change was performed on a DSB-B wafer prepared in-house with a new method in which standard hydrophilic bonding and wafer grinding techniques were used to create mixed orientation wafers having thin box layers that were subsequently removed *in situ*.

Quality of ATR'd Material

Much is known about ion implant-induced damage/amorphization [4,5] and templated recrystallization in single-orientation bulk Si [6,7], in part because ATR without an orientation change is routinely employed in CMOS processing to recrystallize amorphized or pre-amorphized source/drain regions after dopant implantation. In this section we will briefly review some of this data in the context of its relation to the quality of changed-orientation Si.

Rates of recrystallization by solid phase epitaxy (SPE) have been studied as a function of temperature [8], Si dopant [7], Ge content [8], and silicon orientation [6]. Recrystallization rates for undoped Si amorphized with Si are quite fast, about 7.3 nm/s for (100) Si at 650 ^{o}C, with an activation energy of about 2.64 eV. Recrystallization rates are orientation-dependent, with recrystallization fastest in (100)-oriented Si and slower by factors of about 2.5 for (110)-oriented Si and 10 for (111)-oriented Si. Defect densities in Si recrystallized by SPE also depend on Si crystal orientation, being lowest to highest in the order (100) $<$ (110) $<$ (111).

SPE rates of I/I-amorphized Si are also dopant dependent. For (100)-Si doped at ~2 x $10^{20}/cm^3$ (0.4 at %), the rates are faster for B (x20), P (x6), and As (x5); the same for Ge; and slower for Ar (factor of 90), O and N (factor of ~9), and C (factor of 1.6); where all rates are referenced to Si amorphized by self-implantation with Si^+.

In our own defect studies we mostly used (110) or (100) bulk wafers to avoid introducing the bonded interface as a variable. Two types of defects are the most prevalent: e-o-r damage loops (initiated by the interstitials left where the implanted ions stop), and "threads" which show up as pits in plan view SEMs after Secco etching. For the same implant and annealing conditions, pit density was always at least 10x higher in (110) Si than (100) Si, a clear reason to prefer DSB-A substrates over DSB-B. In general, surface defects are worse when the initial amorphous/crystalline Si interface is rough, so better SPE would be expected with substrate cooling during implantation, heavier ions (e.g., Ge^+ vs. Si^+) and a thinner amorphized layer (though this can only be taken so far, since the minimum amorphization depth is constrained by the thickness of the DSB layer).

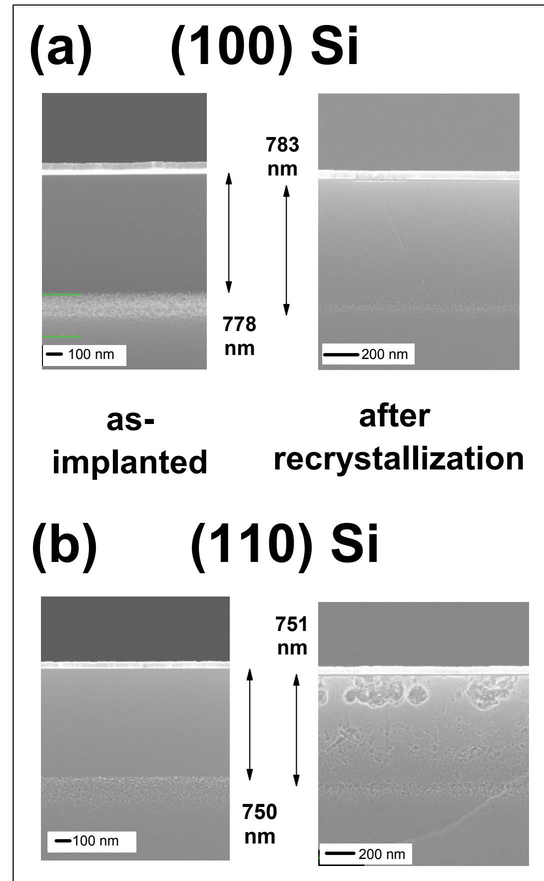

Figure 5. A comparison of blanket ATR in (100) and (110) Si showing the amorphized layer in the as-implanted samples before and after a recrystallization anneal.

Fig. 5 compares the cross section SEM images for (100) and (110) Si amorphized by a dual implant of 1.0 x $10^{15}/cm^2$ 50 keV Si^+ followed by 4.0 x $10^{15}/cm^2$ 220 keV Si^{++} (equivalent to 440 keV Si^+). This implant produced an amorphous layer about 750-780 nm in thickness bounded below by a crystalline damage layer. After recrystallization (by annealing at 650 ^oC for 5 min), a layer of e-o-r loops near the position of the initial amorphous Si/crystalline Si interface is clearly visible. Also evident is the strikingly more defective recrystallization of the (110) material. However, as discussed above, these are "worst case" ATR conditions, since the amorphizing species is a light ion (Si^+) and the amorphized layer is quite thick.

It was found that pit/thread density can be dramatically lowered and the e-o-r damage loops can be made to completely disappear by annealing at high temperature (1300 - 1325 ^oC) for several hours in an inert ambient. Normally such processing temperatures are incompatible with CMOS processing due to concerns about dopant diffusion, but this is not an issue at these early stages of substrate preparation. Our high temperature defect removal process is shown schematically in Fig. 6 and was used to remove e-o-r loops from ATR'd Si recrystallizing to a (100) orientation as shown in the XTEM sample of Fig. 4(c). This same process was also effective in reducing the defectivity of ATR'd Si recrystallizing to a (110) orientation, as can be

seen from the SEM image of Fig. 7 for a sample amorphized and recrystallized with the conditions of the samples shown in Fig. 5. However, there is no doubt that the true measure of the quality of the ATR'd material can only come from device data.

One of the most surprising results encountered during our ATR-DSB process development was the effect of this high temperature annealing on DSB-layer islands surrounded laterally by ATR'd material having the orientation of the substrate. The DSB islands were not stable and showed a spontaneous conversion from their original orientation to the orientation of the substrate. This is shown schematically in Fig. 8(a) for the case of (110)-oriented DSB-A islands in a (100)-oriented substrate. The exact reasons for this instability are not entirely clear, but a likely explanation is that the interface between the (100) and (110) Si has a high energy and is therefore unstable with respect to the reduction in interface area that would occur as the island shrinks in size. Fortunately, as shown schematically in Fig. 8(b), the interface between the (110)-oriented DSB-A islands and the (100)-oriented substrate is stable if the DSB island is bounded by STI. This may be because the DSB interface is pinned laterally by the trench oxide, and/or because a decrease in the island size would not reduce the interface area.

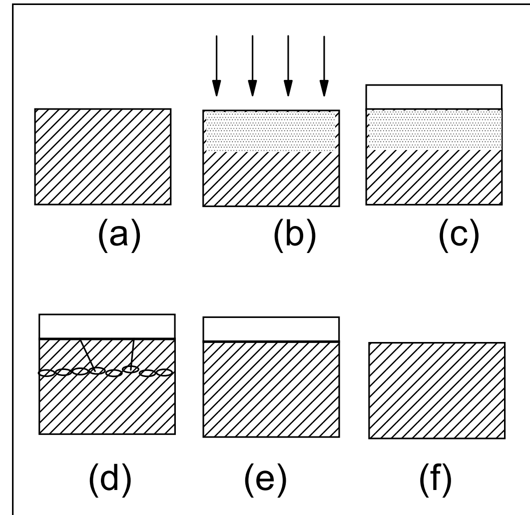

Figure 6. A schematic of the defect removal process, starting with the initial substrate, (a); continuing with implantation to make an amorphous layer, (b); deposition of a protective cap, (c); recrystallization with defects, (d); high temperature annealing to remove defects, (e); and cap removal, (f).

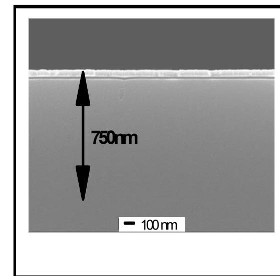

Figure 7. The (110) sample of Fig. 5(b) after the high temperature defect removal process shown in Fig. 6.

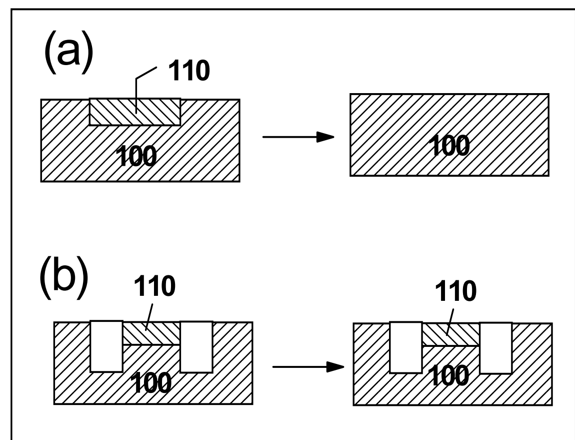

Figure 8. A schematic showing the stability (or instability) of (110)-oriented DSB-A islands in a (100)-oriented substrate to high temperature annealing: islands not bounded by STI, (a); islands bounded by STI, (b).

Defects with Patterned ATR

In this section we will discuss defects peculiar to patterned ATR: the trench-edge defects seen with ATR-with-STI, and the border region morphology seen with ATR-without-STI.

We begin with the trench-edge defects seen with ATR-with-STI. While such defects have been discussed previously [9] and are frequently present at the edges of source/drain regions that have undergone amorphizing implants, they present particular concern for ATR-DSB processes, since the FET gates crossing over to isolation regions cannot avoid passing over the defective Si edges. The problem is shown schematically in Fig. 9 for the case of (100) Si, and illustrated with examples from our own work in Fig. 10a (a higher magnification XTEM of the sample of Fig. 4b) and in Fig. 10b (SEM of a similar DSB sample amorphized with slightly different implant conditions).

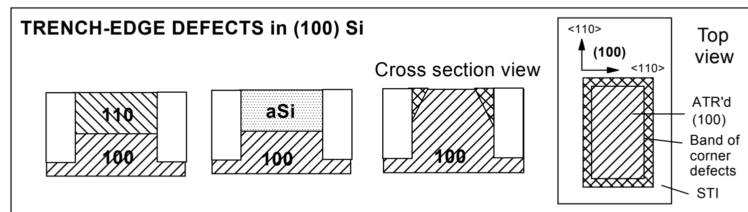

Figure 9. A schematic of trench-edge defects using ATR with DSB-A and recrystallization to the substrate (100) orientation.

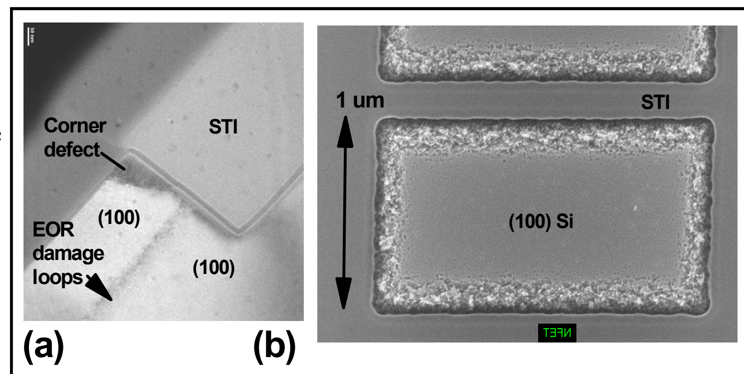

Fig. 10. XTEM image of a trench-edge defect in the sample of Fig. 4(b), (a); a plan view SEM image of a similar sample given a slightly different amorphization implant, (b).

Burbure and Jones [9] attribute these trench edge defects to poor epitaxy on (111) planes during a process sequence shown schematically in Fig. 11. Oxide-filled trenches are first formed around the boundaries of a single-crystal Si region, followed by amorphization of these trench-bounded Si regions by a maskless ion implantation. At an intermediate stage of annealing, recrystallization at the feature edges stops on (111) planes originating from the three-phase intersection of the initial amorphous/crystalline interface and the oxide-filled trench. Recrystallization of the remaining amorphous edge regions must thus templated from (111) planes (the crystal orientation on which SPE defects are the worst), producing the defective final structure shown. Since the (111) planes intersect all four oxide trench edges at a fixed 35.3^{o} angle, defects will be on all four trench edges and the lateral extent of the trench-edge defects will scale with the amorphization depth, as observed previously [9].

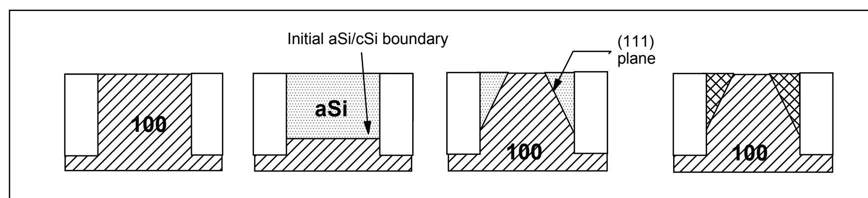

Figure 11. Process sequence for trench-edge defect formation, as described in Ref. 9.

Our own observations of trench-edge defects in (110) Si, shown schematically in Fig. 12, are consistent with this model. We see defective edge regions on two sides instead of four, and, for the same amorphization depth, wider defects on the bad edges than those in (100), because the (111) planes intersect only two trench edges and do so at a wider angle (54.7^{o} instead of 35.3^{o}).

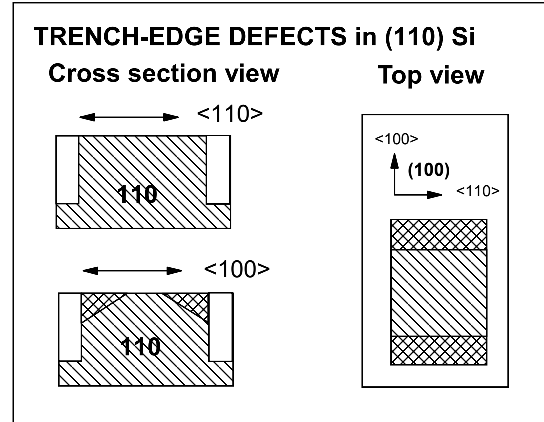

Figure 12. A schematic of trench-edge defects in (110) Si.

Process flows using ATR-without-STI avoid the issue of trench-edge defects, but introduce the possibility of lateral templating at the patterned ATR edges. While a detailed discussion of this topic is beyond the scope of his paper, it is safe to say that the location and defectivity of these border regions will depend on the competition between lateral SPE (templated from the DSB layer) and vertical SPE (templated from the base substrate). Fig. 13 shows a schematic of a border region for the case of a generic DSB substrate. Amorphized Si in the border region between the dark lines will recrystallize into some combination of the DSB layer's (jkl) orientation and the base substrate's (j'k'l') orientation, with the angles of the dark lines fixed by the growth characteristics of the specific crystal orientations contributing to the templating. Whatever this defective edge region looks like, however, it is expected that it will (i) be replaced by an STI trench, and (ii) have lateral dimensions that scale with the DSB layer thickness.

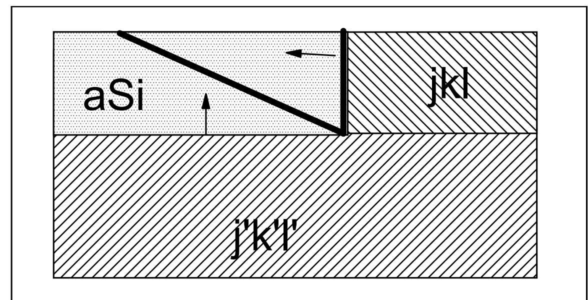

Figure 13. A schematic of a border region during patterned ATR. The amorphized Si within the dark lines will recrystallize to some combination of the (jkl) or (j'k'l') orientations.

DEVICE RESULTS

In this section we summarize some recent device measurements for bulk CMOS FETs with Lpoly = 45 nm fabricated on hybrid orientation substrates made by DSB-ATR from DSB-A wafers [10]. In this case, the nFETs are in changed-orientation (100) Si, and the pFETs are in the original (110) DSB layer, as shown schematically in Fig. 14. pFET performance was found to be the same in both the original (110) DSB layers and (110) bulk controls, implying that the DSB layer is not degraded by processing, and that the bonded interface does not interfere with the device. nFET performance was found to be the same in changed-orientation (100) ATR'd layers, (100) bulk controls, and (100) bulk wafers undergoing ATR with no orientation change (i.e., amorphization followed by recrystallization back into the substrate's original (100)

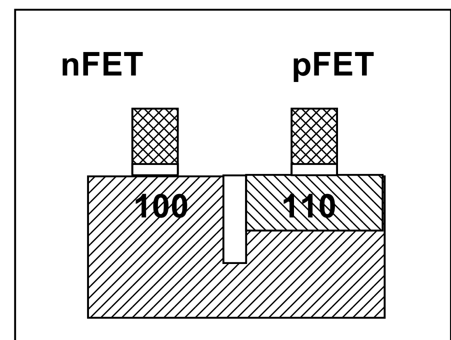

Figure 14. The preferred arrangement of nFETs and pFETs on a hybrid orientation substrate.

orientation), implying no degradation from the ATR process itself. Ring oscillators fabricated on these same wafers showed improvements of more than 20% compared with the same devices on the (100) control wafers.

SUMMARY

We have shown that the crystal orientation of single-crystal silicon layers may be changed in selected areas from one orientation to another by an amorphization/templated recrystallization (ATR) process on direct-silicon-bonded (DSB) wafers, and described practical ways in which the ATR-DSB method might be use to form hybrid orientation substrates. The materials and integration challenges encountered while reducing the method to practice have led to some interesting and unexpected results, including some which are still under investigation. Findings of particular interest include (i) observations of oxide removal from a buried interface (with applications to hydrophilic methods of forming DSB wafers), (ii) the use of high-temperature annealing to remove e-o-r damage (as well as embedded islands of differently-oriented Si), and (iii) the differences in trench edge defects between (100) Si (the case of DSB-A) and (110) Si (the case of DSB-B).

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