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Abstract

In this paper the results of an experimental comparison of popular pass-transistor logic families in 1.5V, 0.18μm CMOS technology using advanced CAD tools for circuit tuning and simulation are presented. The logic families were compared using an experimental setup designed to clarify the strengths and weaknesses of each family in a relative fashion and evaluate their individual performances under identical operating conditions. An automatic circuit tuner was used to help ensure that the test circuits from each logic family were operating at near optimum performance. It is shown that the Differential Cascode Voltage Switch with Pass-Gate (DCVSPG) logic family is the most robust with respect to an amalgamation of speed, power, area and physical design criteria. The methodology of using hybrid pass-transistor / static CMOS circuit styles is also presented.

1 Introduction

Conventional static CMOS is the most popular VLSI digital logic circuit family in use today. Static CMOS logic circuits are robust, reliable and have excellent noise tolerances. However, today's VLSI design trends are bringing requirements of increased speed and reduced power dissipation, increasing concern as to the future effectiveness of static CMOS circuits. Dynamic circuits have been shown to achieve increased speed over their static CMOS counterparts [1]-[2] but at a high cost of increased noise, reduced noise margins, increased complexity and increased difficulty in testing. As a result, many researchers have been investigating the use of pass-transistors circuit techniques to achieve the speed and noise performance of static CMOS but with reduced area and power [3]-[6]. Pass-transistor logic gates can be faster than their equivalent static CMOS logic gates due to the reduction

in the number and sizes of PMOS transistors. The major problem with pass-transistor circuits is the slower pull-up speed of the NMOS logic tree transistors, which are typically only about half as strong pulling up as they are pulling down. In many cases, inverters need to be inserted between logic stages to combat this problem.
Many authors have published results on different pass-transistor logic families, each claiming to be in one way or another superior to the competition. Many of the comparisons that have been made have not been done in a general testing environment with the help of advanced CAD tools such as automatic circuit tuners. The major purpose of this work is to try and confirm the reported results of previous authors using the latest in advanced CAD tools and deep submicron CMOS technology in addition to providing a significant clarification of the relative strengths and weaknesses of each of the popular pass-transistor logic families.
In this paper, a detailed experimental comparison of various popular pass-transistor logic families will be described using a general testing environment and an automatic circuit tuner. The objective of the experimental comparison is to clarify the strengths and weaknesses of each logic family in a relative fashion with each logic family being tested under the same conditions.

2 Overview of Pass-Transistor Logic Families

In our experimental comparison, we shall use a 3-input XOR/XNOR logic gate as the test vehicle. This logic function is very common in processor arithmetic circuits. One of the major issues we shall be concerned with in our scrutiny of the various logic families is the amount of charge required from the power supply to complete a logic evaluation. This charge flow can result from both the charging of circuit capacitance and from momentary conductance paths between the power supply and ground. Both of these phenomena are of equal importance in evaluating the quality of a particular logic family. Some logic families have larger logic gate internal capacitance but no momentary DC current paths. Other logic families have momentary DC current paths but small logic gate internal capacitance.
Another important feature to consider is the delay skew between the true and complement outputs of each logic gate. Since each logic gate in general takes true and complement inputs, delay skew between true and complement signals can also create momentary conductance paths between the power supply and ground, wasting energy and power. As such, we must pay careful attention to the delay skew introduced by each logic family. Also, we are interested in seeing which logic families exhibit skew-correcting properties at their true and complement outputs.
Shown in Fig. 1 are the static CMOS [2], DCVSPG [4], DCVSPGB [8], SRPL [6], CPL [3], CPLHL [10], TGL [2] and DPL [5] logic gates used in this comparison.

3 Experimental Procedure and Results

In this section, we shall describe the experimental procedure used in the logic family comparison. As previously stated, the logic gate chosen for the comparison between logic families was the 3-input XOR gate. This logic function enjoys great popularity in a wide variety of processor circuits. The gate was connected in two test circuit configurations. The first

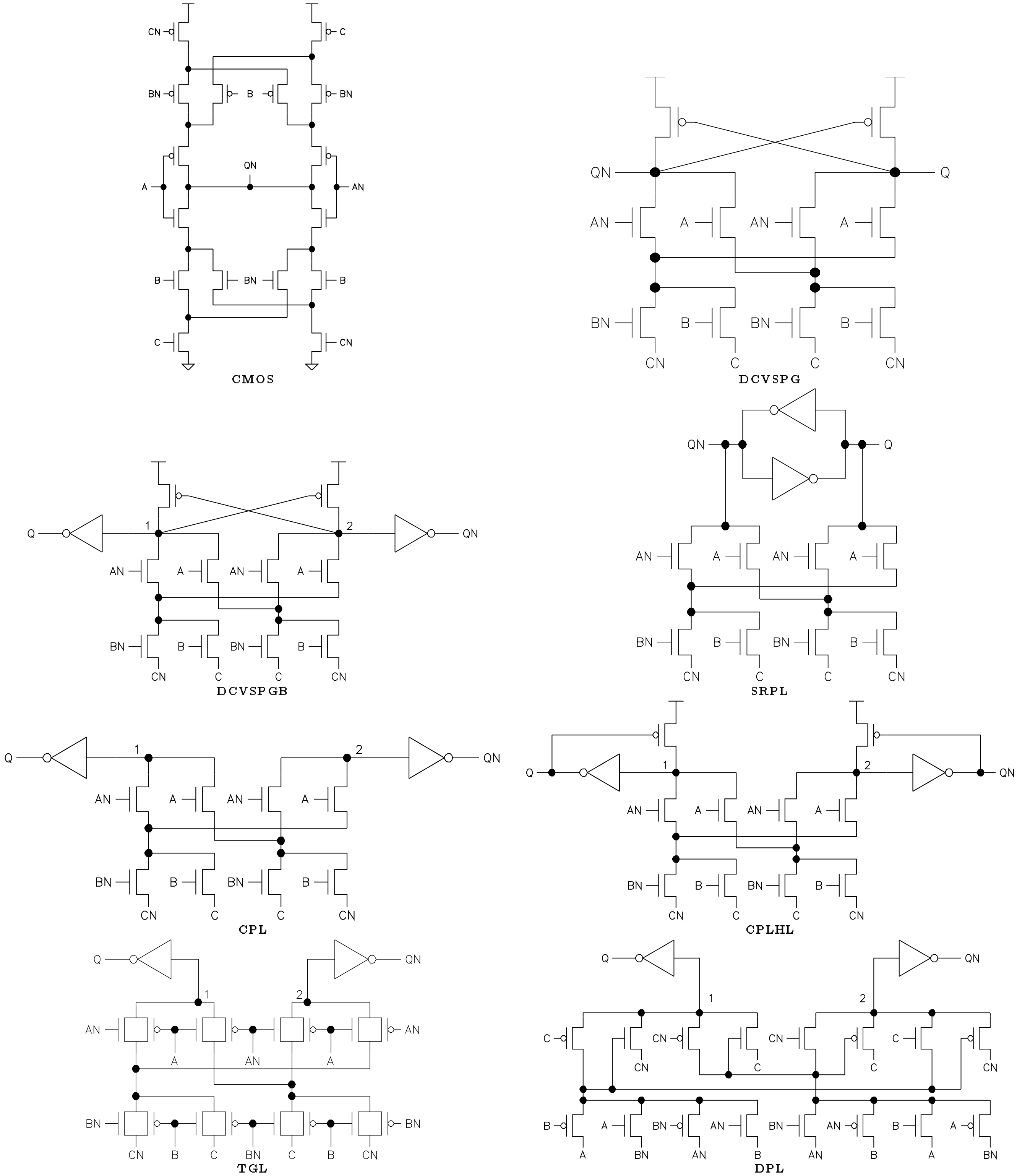

Figure 1: 3-input XOR gates used in this comparison.

was a 9-stage ring oscillator that measured the ability of the gate to to both be driven by and to drive an identical gate. Note that only those logic families with DC conductance paths to ground in each gate could be used in the ring oscillator experiment. This excludes DCVSPG but includes DCVSPGB. For each logic family, the sizes of the transistors in the 3-input XOR/XNOR gate were adjusted to maximize the oscillator frequency. This was done by keeping the sizes of the NMOS transistors in the logic trees the same from family to family and adjusting the buffer, cross-coupled and latching NMOS and PMOS transistors to maximize the operating frequency of the oscillator. For the second test configuration, the 3-input XOR/XNOR gate from each logic family is driven by fixed inverter drivers and the sizes of all of the transistors in the gate were adjusted to minimize the delay through the *entire* circuit from the input of the drivers to the output loads. The gates were tuned in this manner for a variety of output load strengths. All simulations were done in 1.5V, 0.18μm CMOS technology.

Shown in Table 1 are the results from the ring oscillator experiment after frequency scaling and normalization. A discussion of the performance of the logic families relative to conventional static CMOS will now be given.

DCVSPGB tied with DPL for being the fastest logic family in the ring oscillator experiment. DCVSPGB was slightly worse than DPL in the areas of power, power-delay and total channel width. When compared to CPL, it is clear that the cross-coupled PMOS transistors in DCVSPGB both improved the delay and reduced power.

CPL showed the highest power dissipation of any of the families considered. This is due to the voltage threshold drop from the NMOS logic tree and the fact that the PMOS transistors in the output inverters are not fully turned off, which is very undesireable. The introduction of latching devices in CPLHL helps to reduce the power dissipation slightly at the expense of slightly increased delay. The reason the power dissipation for CPLHL was not reduced further lies in the fact that during transitions there still DC current paths between the power supply and ground through the latching PMOS transistors.

TGL shows delay results similar to CPL and power results similar to CPLHL. The big drawback with TGL appears to be the extra area occupied by the logic tree PMOS transistors, which in the experiment appeared to contribute more to level restoration of the logic tree outputs than to the switching speed of the gate. This makes intuitive sense as any increase in drive provided by the PMOS logic tree transistors is offset by the additional capacitance they add to the tree nodes.

DPL also performed very well in the ring oscillator experiment, posting slightly better numbers for power, power-delay product and channel width than DCVSPGB.

SRPL exhibited very poor delay performance in the ring oscillator experiment (worse than CMOS). Buffers were applied to SRPL to help its performance but the automatic circuit tuner moved the channel widths of the cross-coupled NMOS transistors to zero during the tuning process, in which case the SRPL gate became a DCVSPGB gate. As a result of these observations, SRPL is not included in Table 1 as a competitive logic family for the ring oscillator experiments.

Shown in Fig. 2 and tables 2-3 are the results from the fixed driver experiment. For the extremes of the loading spectrum, the sizes of the logic tree transistors relative to static CMOS are shown in Table 2. From this table, we can understand the mechanics of the logic families and how the logic tree transistors (NMOS versus PMOS) are affecting their performance. For example, it is noticed that the PMOS tree transistors in TGL appear not to be contributing as much to the gate performance in terms of delay as those in DPL, since they are in general much smaller relative to their NMOS counterparts. In addition, one can see that the DPL NMOS tree transistors are much smaller than those of the other logic families, indicating the effectiveness of their PMOS counterparts.

Conventional static CMOS comes in with the worst delay ranking for both ends of the loading spectrum. This was expected as the load placed on the fixed drivers by the CMOS 3-input XNOR gate was quite large due to the large PMOS transistors in the logic tree. These transistors were required to be large as they were series connected in a three-transistor-high pull-up stack, a very undesireable feature.

DCVSPG scored the best delay for low loading situations. For higher loads, DCVSPGB with its buffers had the second best delay. The crossover point for the technology considered was about 40fF. Thus, one can use either DCVSPG or DCVSPGB and be assured of getting a good delay, independent of circuit load. The principle reasons for the performance of DCVSPG and DCVSPGB were the significant reduction in loading on the fixed drivers due to the elimination of PMOS transistors from the logic tree and the assistance of the cross-coupled PMOS transistors in maintaining adequate rise times and minimizing delay skew at the outputs. In addition, during the circuit tuning process, it was noticed that the presence of the cross-coupled PMOS transistors enabled the relative sizes of the NMOS and PMOS transistors in the output inverters for DCVSPGB to be more balanced, leading to improved noise margins as opposed to CPL which will be discussed shortly.

SRPL followed the same data curve trajectory as DCVSPG but with a higher delay. This seems to indicate that the cross-coupled NMOS transistors are degrading the overall performance of the gate instead of helping it. In fact, the cross-coupled NMOS transistors are turning on too late to be effective in pulling down the outputs of the gate. The cross-coupled PMOS transistors, on the other hand, are turning on early enough to help pull up the outputs, reduce the rising edge delays and minimize delay skew at the outputs, which is taken advantage of by DCVSPG and DCVSPGB. During the circuit tuning process, the automatic circuit tuner tried to move the channel widths of the cross-coupled NMOS transistors to zero to improve the circuit delay, further confirming our conclusions about the limitations of these elements.

CPL was found to be more effective for larger loads than for smaller ones. This was primarily due to the extra delay introduced by the output inverters for small loads. In addition, it was noticed during the circuit tuning process that the NMOS transistors in the output inverters became much larger than their PMOS counterparts, an undesireable result from the standpoint of noise margin. CPL was unable to beat DCVSPG for small loads and DCVSPGB for larger loads, indicating the usefulness of the cross-coupled PMOS transistors in DCVSPG and DCVSPGB in improving the circuit delay. CPLHL was only slightly slower than CPL for all loading conditions.

TGL posted good delay numbers for the spectrum of loads considered but was still slower than DCVSPG for small loads and DCVSPGB for larger loads. This makes sense as it was found during the circuit tuning process that the automatic circuit tuner made the PMOS logic tree transistors smaller than the NMOS logic tree transistors, minimizing the loading effect of the PMOS transistors on the fixed drivers and internal logic tree nodes. The PMOS logic tree transistors were also effective in providing faster restoration of the logic tree outputs

to the power supply voltage than the latching transistors of CPLHL.
DPL showed good small load performance and the best larger load performance of all of the logic families. During the circuit tuning process, the automatic circuit tuner made the PMOS logic tree transistors at least as large as their NMOS counterparts. This indicates that these PMOS transistors provide increased drive in pulling up the logic tree output nodes as opposed to in TGL where they are only effective in restoring the logic tree output nodes to the power supply voltage.
Conventional static CMOS was found to be one of the worst energy consumers, only being outdone by CPL for larger loads. The energy consumption of static CMOS is due to the significant amount of charge supplied by the fixed drivers to drive the gate inputs due to the large PMOS logic tree transistors and also the significant logic tree capacitance. DCVSPG consumed the least amount of energy for both small loads and larger loads. This was expected since DCVSPG requires the least amount of charge from the power supply to operate. DCVSPGB required only slightly more energy than DCVSPG due to the inverter buffers at its outputs.
SRPL was close to DCVSPGB in its energy consumption. This is attributed to the slighly larger logic tree transistors that were necessary to adequately drive the NMOS cross-coupled loads and the charge taken by the NMOS and PMOS cross-coupled loads. CPL was a significant energy consumer, being only bested by CMOS at smaller loads. This is primarily due to the DC currents flowing in the output inverters as a result of the voltage threshold drop in the NMOS logic tree. CPLHL was better than CPL but still ranked in the top 50% of the energy consumers. TGL was worse than DCVSPG, DCVSPGB and SRPL over the spectrum of load variations. This was expected as the PMOS logic tree devices and the capacitance they introduce required additional charge to be supplied by the fixed drivers.
DPL was the second best energy consumer over the spectrum of loads considered, being only outdone by DCVSPG. This was due again to the unique structure of the DPL logic tree.
DCVSPG and DPL posted the best energy-delay products over the spectrum of loads while CMOS has by far the worst energy-delay product.
With respect to area, static CMOS was the worst and DCVSPG and DPL were the best with DCVSPGB occupying the number three position.

4 Hybrid Approaches

In this study of pass-transistor logic families an XOR/XNOR gate was used as the test vehicle due to its high frequency of occurance in many arithmetic circuits that require addition, comparisons and parity checking. In general VLSI applications it is often very desireable to mix pass-transistor and conventional static CMOS logic together [10] to achieve the best speed, power and area performance. An example of a 9-bit parity generator using both DCVSPG and static CMOS gates is shown in Fig. 3.

5 Summary and Conclusion

In this work, the performance relative to static CMOS of several, popular, dual-rail, pass-transistor logic families was compared experimentally using 1.5V, 0.18μm CMOS technology

Table 1: Frequency-scaled, normalized ring oscillator experiment results.

Gate	Delay	Power	Power-delay	Channel Width
CMOS	1.00	1.00	1.00	1.00
DCVSPGB	0.52	0.79	0.41	0.41
CPL	0.55	1.51	0.85	0.38
CPLHL	0.62	1.21	0.75	0.54
TGL	0.54	1.24	0.68	0.7
DPL	0.52	0.76	0.40	0.4

Table 2: Normalized logic tree transistor sizes from fixed driver experiment.

	C_{load} = 10fF		C_{load} = 50fF	
Family	NMOS	PMOS	NMOS	PMOS
CMOS	1.00	1.30	1.00	1.33
DCVSPG	0.80		0.89	
DCVSPGB	0.60		0.50	
SRPL	0.90		0.89	
CPL	0.60		0.56	
CPLHL	0.80		0.61	
TGL	0.50	0.20	0.50	0.11
DPL	0.30	0.30	0.22	0.27

Table 3: Rankings of logic families in fixed-driver experiments (1 = best, 8 = worst).

	Delay		Energy	
Logic Family	$C_{load} \leq$ 10fF	$C_{load} \geq$ 50fF	$C_{load} \leq$ 10fF	$C_{load} \geq$ 50fF
CMOS	8	8	8	7
DCVSPG	1	6	1	1
DCVSPGB	5	2	3	4
SRPL	2	7	4	3
CPL	6	4	7	8
CPLHL	7	5	6	6
TGL	4	3	5	5
DPL	3	1	2	2

	Energy-Delay Product		Area	
Logic Family	$C_{load} \leq$ 10fF	$C_{load} \geq$ 50fF	$C_{load} \leq$ 10fF	$C_{load} \geq$ 50fF
CMOS	8	8	8	8
DCVSPG	1	2	1	2
DCVSPGB	4	3	3	3
SRPL	3	4	5	4
CPL	7	7	4	6
CPLHL	6	6	7	7
TGL	5	5	6	5
DPL	2	1	2	1

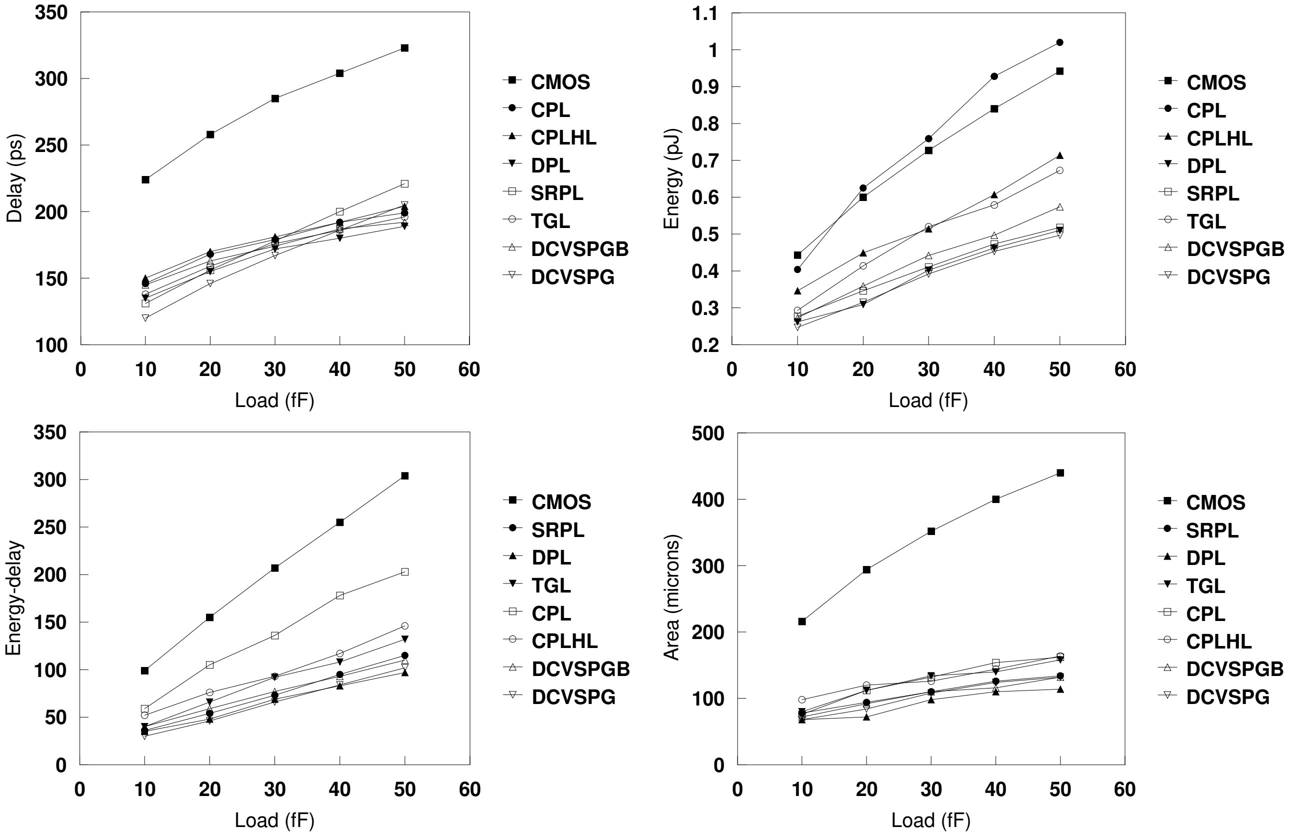

Figure 2: Results for delay, energy, energy-delay product and area for fixed-driver, variable-load experiment.

and automated circuit tuning. It was found that in general DCVSPG and DCVSPGB were the best logic family choices for high-speed, low-power, VLSI and ULSI applications. CPL was found to suffer from high power dissipation, while having larger delays than DCVSPG and DCVSPGB. The addition of PMOS latching transistors to CPL (CPLHL) improved performance with respect to power dissipation but degraded delay. SRPL was found to be worse than DCVSPG and DCVSPGB in all aspects. TGL suffered from the extra area occupied by the PMOS logic tree transistors which increased power dissipation and did little to improve performance except for voltage level restoration. DPL was shown to be slightly better than DCVSPG and DCVSPGB in the areas of power dissipation and total channel width but its complex logic tree interconnections can add performance degrading parasitics and significant physical design complications.

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References

[1] K. Bernstein et al.,"High Speed CMOS Design Styles", Kluwer Academic Publishers, 1998.

[2] N. Weste and K. Eshrachian, "Principles of CMOS VLSI Design", 2nd Edition, Addison Wesley, 1993.

[3] K. Yano, T. Yamanaka, T. Nishida, M. Sato, K. Shimohigashi and A. Shimizu, "A 3.8 ns CMOS 16×16 Multiplier using Complementary Pass-Gate Transistor Logic," *IEEE Journal of Solid-State Circuits*, vol. 25, 1990, pp. 385-388.

[4] F.S. Lai and W. Hwang, " Differential Cascode Voltage Switch with Pass-Gate Logic Tree for High Performance CMOS Digital Systems ," *1993 Int. Symp. VLSI Technology Systems Applications*, 1993, pp. 358-362.

[5] M. Suzuki, N. Ohkubo, T. Yamanaka, A. Shimizu and K. Sasaki, "A 1.5 ns 32b CMOS ALU in Double Pass-Transistor Logic," *Dig. Tech. Papers, ISSCC*, 1993, pp. 90-91.

[6] A. Parameswar, H. Hara and T. Sakuri, "A Swing Restored Pass-Transistor Logic-Based Multiply and Accumulate Circuit for Multimedia Applications", *IEEE J. Solid-State Circuits*, Vol. 31, No. 6, pp. 804-809, June 1996.

[7] D. Somasekhar and K. Roy, "Differential Current Switch Logic: A Low Power DCVS Logic Family",*IEEE J. Solid-State Circuits*, Vol. 31, No. 7, pp. 981-991, July 1996.

[8] F.S. Lai and W. Hwang, "Design and Implementation of Differential Cascode Voltage Switch with Pass-Gate (DCVSPG) Logic Tree for High Performance Digital Systems",*IEEE J. Solid-State Circuits*, Vol. 32, No. 4, pp. 563-573, April 1997.

[9] R. Zimmermann and W. Fichtner,"Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic",*IEEE J. Solid State Circuits*, Vol. 32, No. 7, pp. 1079-1090, July 1997.

[10] S. Yamashita, K. Yano, Y. Sasaki, Y. Akita, H. Chikata, K. Rikino and K. Seki, "Pass-transistor/CMOS Collaborated Logic: The Best of Both Worlds", 1997 Symposium on VLSI circuits, Digest of Tech. Papers, pp. 31-32, 1997.

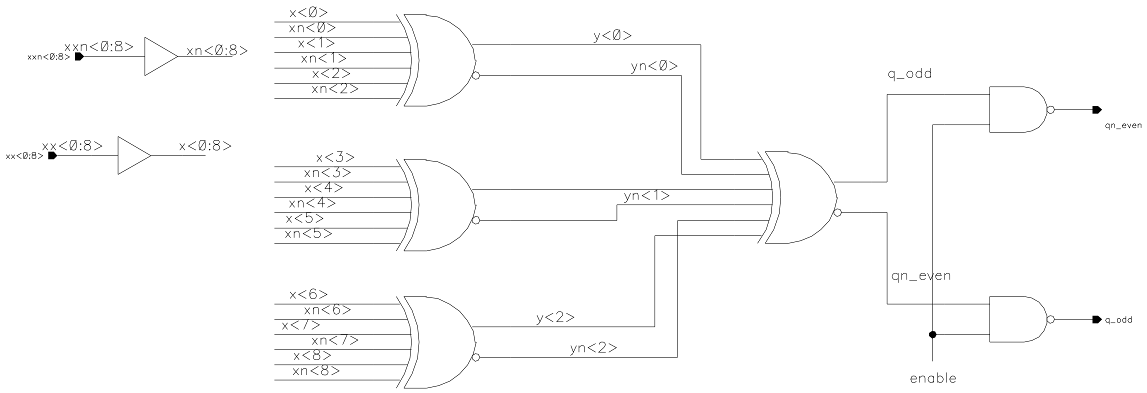

Figure 3: Hybrid implementation of 9-bit parity checker.