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Research Report

AM-OLED pixel circuits suitable for TFT array testing

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ABSTRACT

We have created new easily testable pixel circuits for AM-OLEDs. The TFT array testing process is very important to improve yield in mass-production because the cell process heavily influences the manufacturing cost and time. However, conventional AM-OLED pixel circuits are very difficult to test. One reason is that the pixel circuits in TFT arrays do not have the OLED yet. Therefore we cannot drive the pixel circuits to measure the current through the driver TFT that drives the OLED in the pixel. Our new design interleaves the common lines in a new way, and adding one or two transistors to the pixel allows testing each of the pixels before the OLED fabrication.

INTRODUCTION

Recently AM-OLED mass production has started and in the near future it will greatly increase. For mass-production, the yield is very important, and TFT array testing has an especially important role because the OLED cell process is more expensive than the TFT array process. However, it is quite difficult to test TFT arrays because the OLED has not been added to it yet, and cannot conduct any current. Various test methods are now being investigated, but they are not satisfactory to measure the threshold voltage (V_{th}) and the mobility of the driver TFT. In this paper, we propose new pixel circuits suitable for TFT array testing, which use an additional 1 or 2 transistors and dual common lines. It is easy to add more TFTs in the poly-silicon process without much decreasing the aperture ratio. By using dual common lines, we do not need to have additional lines for testing.

INSPECTION OF DRIVER TFT

In inspection of the TFT array involves the open/short wiring test, the storage capacitance leak test, and characterization of the driver TFT. For the test of the driver TFT, the I_d-V_{gs} characteristics of the driver TFT are measured and its V_{th} and mobility are estimated from

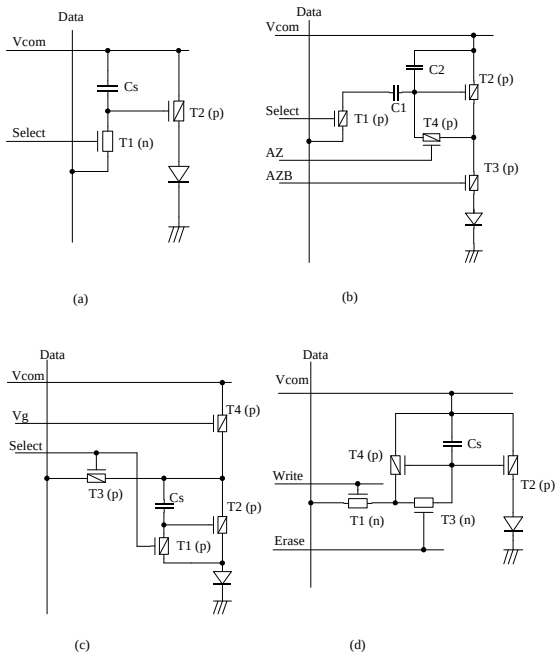

Fig. 1. Various AM-OLED pixel circuits. (a) simple V-prog. circuit (b) V_{th} compensated V-prog. circuit (c) I-prog. circuit (d) current mirror circuit

the result. When the V_{th} or the mobility of driver TFT varies, the screen quality (uniformity and contrast) is degraded. If V_{th} and the mobility can be measured immediately after the array has been fabricated, the manufacturing costs will be reduced substantially, since TFT arrays with defects can be rejected before the cell process. The conventional pixel circuits are shown in Fig. 1. In the inspection of TFT array, since the OLED is not present, there is no transmission of drain current (I_d) through the driver TFT (T2). Therefore, I_d cannot be measured even if the gate-source voltage (V_{gs}) is supplied to the driver TFT. In order to measure the I_d of driver TFT, it is necessary to add a path for the current other than the OLED. At the same time, it is important to avoid decreasing the aperture ratio and increasing the wiring process.

CONCEPT OF TESTABLE PIXEL CIRCUIT

Discussing the simplest pixel circuit in Fig. 1 (a), the easiest way to test the driver TFT is by adding another transistor (T3) and the independent lines shown in Fig. 2. We can then test the driver TFT (T2) by turning on the bypass TFT (T3). Of course this circuit has more TFTs and lines, which causes a decrease not only in the aperture ratio but also in the yield. To reduce the number of lines, the gate of T3 can be connected to a select line.

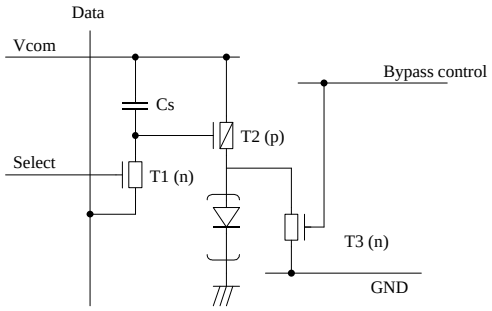

Fig. 2. Pixel circuit with one additional transistor, a bypass control line, and a GND line on the basis of Fig. 1(a). T1 and T3 are on at the same time when testing.

We suggest a new pixel circuit to reduce the extra lines by employing dual common lines. We can remove the extra GND line in Fig. 2 and connect the source of T3 to the next V_{com} line. In addition, the V_{com} line is split into two independent lines, for example even and odd lines, placed like the teeth of a comb. The conventional V_{com} layout is shown in Fig. 3 and our new V_{com} layout is shown in Fig. 4. The equivalent pixel circuits are shown in Fig. 5. An example pixel circuit with bypass switches is shown in Fig. 6. In display mode, V_{com1} and V_{com2} are linked to a power source, V_{dd} (i.e. 10-15 V). A typical waveform in the display mode is shown in Fig. 7. In inspection mode, V_{com1} and V_{com2} are connected to V_{dd} and GND, respectively, when the odd lines are being inspected, as shown in Fig. 8. In this state, we can detect the current at the electrode pad of V_{com2} that bypasses through T3. Since T3 is fully on when testing, there is no problem with the characteristics of T3. For the even lines, V_{com1} and V_{com2} are switched to GND and V_{dd}, respectively, in the inspection mode.

There are several variations of the T3 design. The gate

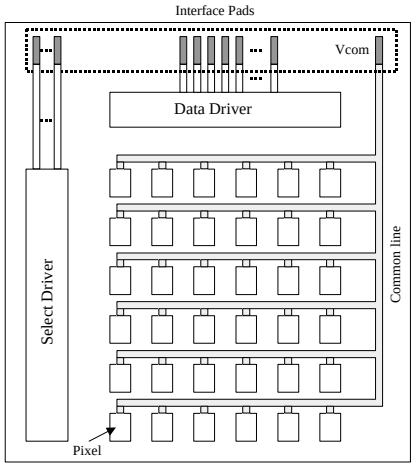

Fig. 3. Conventional V_{com} layout.

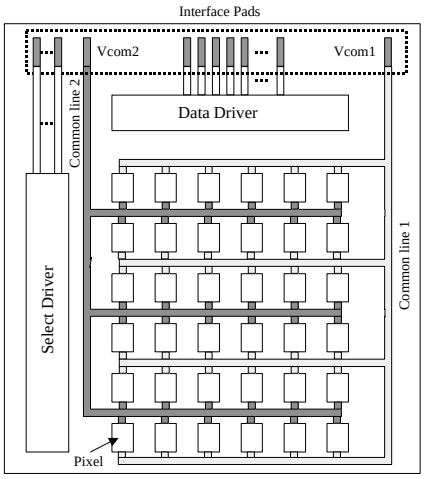

Fig. 4. New V_{com} layout (Dual common lines).

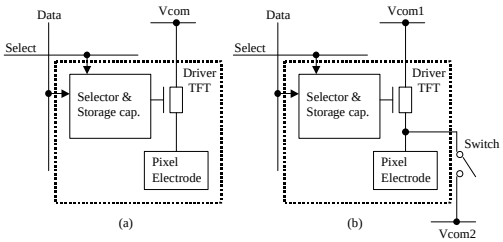

Fig. 5. Equivalent pixel circuit of Fig. 3 & Fig. 4. (a) Conventional pixel circuit, (b) New pixel circuit.

electrode of T3 is connected to the select line that is in the same pixel in Fig. 6. However, we can connect it to another select line, such as the line before or after that pixel. It could be connected to the drain in order to use T3 as a diode although its test sequence becomes a little bit complicated.

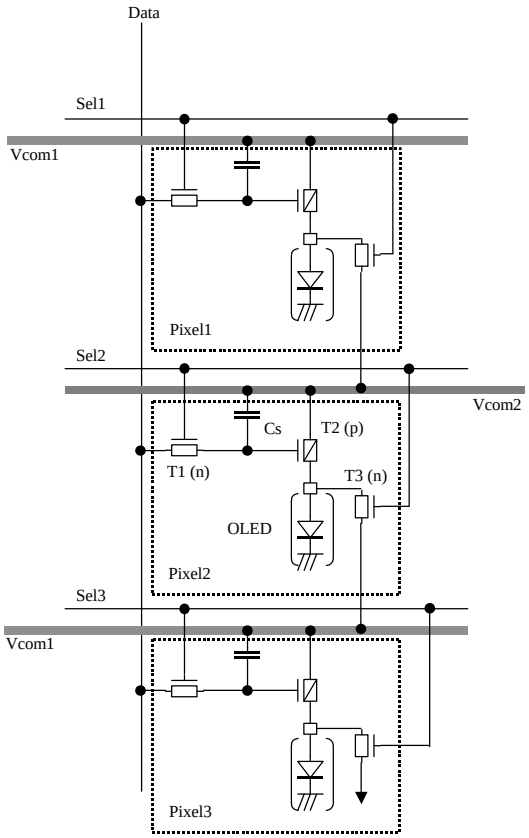

Fig. 6. New pixel circuit design with dual common lines V_{com1}/V_{com2}. Pixel2 above the gate of test transistor TFT T3 is connected to a select line and the source is connected to V_{com1}.

The dual common lines design is so useful in testing that we need no extra lines but only 1 additional TFT. However it still has one problem when in display mode except the case that T3 works as a diode. When setting a value in a pixel, there is a moment when both the select line and T3 are on, so that the OLED on a pixel electrode is fully emitting for that moment. This harms the contrast ratio and OLED lifetime.

PRACTICAL PIXEL CIRCUIT DESIGN

In the pixel design shown in Fig. 6, the pixel is fully emitting for a moment as it is set. To avoid this, we must use two additional TFTs per pixel, not one, as shown in Fig. 9. For Pixel2 in Fig. 9, the additional TFTs T3 and T4 are connected in series. The gate of T3 is connected to the select line (Sel2) of the same pixel and that of T4 is connected to the previous select line (Sel1). In display mode Sel1 and Sel2 do not turn on at the same time, so the OLED is not emitting even when setting the pixel. In

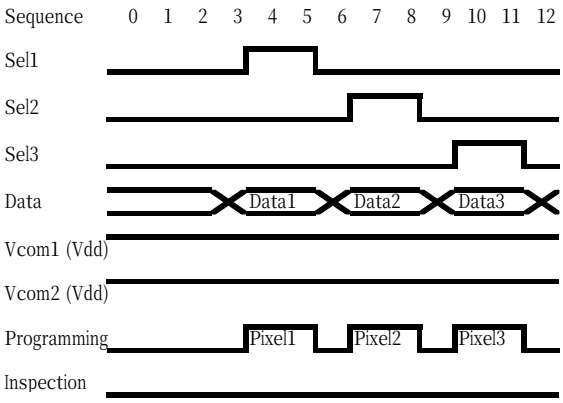

Fig. .7 Normal driving signals for dual common lines shown in Fig. 6. V_{com1} and V_{com2} are tied to V_{dd}.

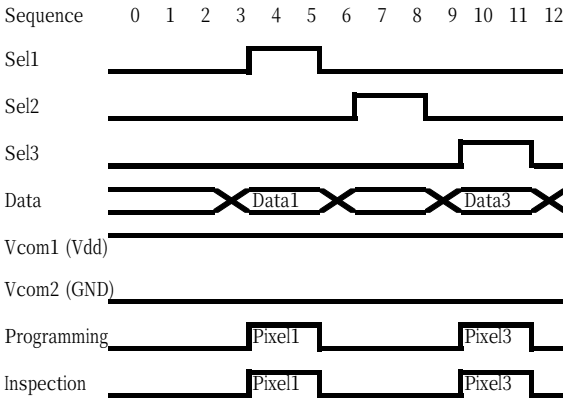

Fig. 8. Testing signals for dual common lines shown in Fig. 6. V_{com1} and V_{com2} are tied to V_{dd} and GND in testing mode for the odd lines.

inspection mode, we only have to apply two select pulses in 1 refresh period to turn on both TFTs, as shown in Fig. 10. When we would like to test the leakage of storage capacitance after we have set the data in all of the pixels, we can do this by checking the current through the driver TFT at the V_{com} line, which is GND, after 1 refresh period. It is also possible to measure the I_d-V_{gs} characteristics in 1 refresh period by switching V_{com1} and V_{com2} as shown in Fig. 11, so we strongly recommend separating the inspection sequence into two phases, inspections for odd lines and for even lines, in order to measure accurately, because the voltage switching would affect the data programmed in the storage capacitance.

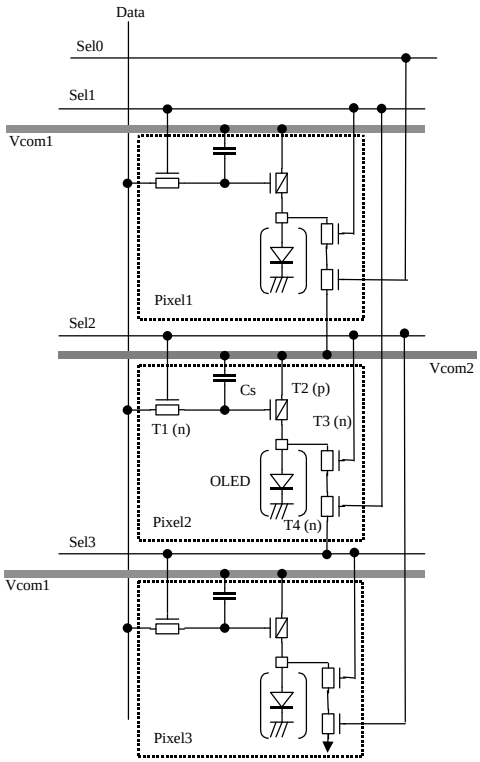

Fig. 9. Two TFTs for testing are placed in a circuit. In Pixel2 above, the gate of T3 is connected to the select line of itself and that of T4 is connected to the previous select line. Such placement prevents the OLED from fully emitting when setting the pixel.

SUMMARY

We created a new pixel design for easier array testing during mass production. It needs only 1 TFT with two gates and does not need any extra lines. By applying it to the pixel circuit we can test TFT arrays without an expensive TFT array tester. As the yield of TFT array increases, such circuits oriented to testing are becoming more important. In addition, the idea of dual common lines has the potential to produce other useful pixel circuits or driving schemes. For example, it may be possible to discharge the OLED capacitance, to shut off the current more quickly, and so on. In the development of AM-OLED, the necessity for TFT array testing is expected to increase more and more.

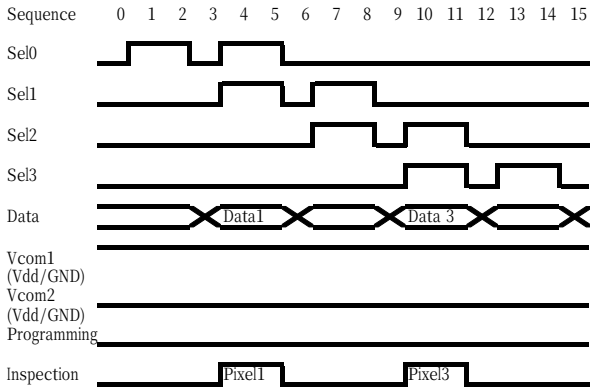

Fig. 10. Test sequence to measure even and odd lines in turn. While V_{com1} and V_{com2} are tied toV_{dd} and GND, respectively, we can test the odd lines. After all tests for the odd lines, V_{com1} and V_{com2} are switched and we repeat the same sequence for the even lines.

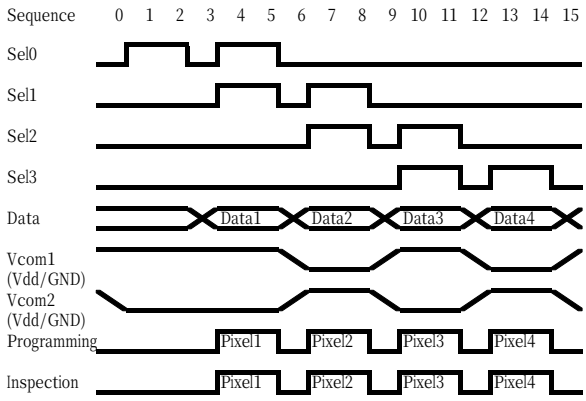

Fig. 11. Test sequence to measure all of the lines in one refresh period. The I_d-V_{gs} characteristics can be measured by using this sequence.

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