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Research Report

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F. Menges, F. Motzfeld, H. Schmid, P. Mensch, M. Dittberner, S. Karg, H. Riel, and B. Gotsmann

IBM Research – Zurich
8803 Rüschlikon
Switzerland

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[1]IBM Research – Zurich, Switzerland, email: bgo@zurich.ibm.com

***Abstract*—**Hot spots with dimensions of only a few nanometers form in numerous nanoelectronic devices. Based on recent advances in spatial resolution, these hotspots can now be studied by means of Scanning Thermal Microscopy (SThM). Here, we discuss SThM for nanoscale thermometry in comparison with other established thermometry techniques. In situ measurements of semiconductor channels for logic, and phase change memory devices are used to demonstrate today's measurement capabilities. Temperature fields characterize not only energy dissipation in in-tact devices but can also serve to identify device failure and fabrication issues.

1. INTRODUCTION

High power densities and hot spot formation are growing concerns in integrated electronics. Prevention of local hot spot formation at the device level requires thermal design, where both layout [1] and materials choice [2] are subject to constraints. The requirements are defined by the application; for high performance logic, good thermal coupling to a heat sink is desired, whereas for phase-change memory applications, enhanced insulation from the thermal reservoir can be a design goal. The demand for better thermal design is a strong motivation for *in situ* nanoscale thermometry of operating devices.

Table 1 compares selected thermometry techniques in terms of generic requirements for thermometry of nanoscale devices. We note that the specific demands depend on the exact application and further methods may be relevant [3,4]. Specifically, temperature mapping with a lateral resolution in the nm-range [1], temperature resolution better than 1 K, and in some cases, temporal resolution up to GHz operation frequencies is desired. Further, the method should be applicable on the wafer scale and to various materials, including metals, semiconductors and dielectrics. Common device geometries and, ideally, buried structures, should be accessible. Furthermore, the method should be non-interfering and quantitative.

Optical methods by far field imaging are quantitative, reliable, sensitive and can be non-interfering. However, although readily used to measure self-heating of microelectronic devices [1-4], their lateral resolution is fundamentally diffraction-limited. A recent electron microscopy based nanoscale thermometry approach achieves higher spatial resolutions, but faces limitations in materials choice and sample geometry. Non-imaging, thermometry techniques are very sensitive and fast, but constrained to certain niches as they lack important information about the local temperature field distribution. SThM [5] can in principle meet most of the aforementioned requirements. As discussed below, a recently introduced scanning probe thermometry technique enables overcome systematic errors and resolution limitations previously considered detrimental.

2. II. SCANNING THERMAL MICROSCOPY (STHM)

In SThM, a cantilevered temperature-sensitive heater-sensor, equipped with a nanoscale sharp tip, is raster scanned over the sample surface in mechanical contact (Fig. 1a). The local temperature (Fig. 3) or thermal conductance (Fig. 4) of the sample can be inferred from the measured thermal interaction. Until recently, the thermal interaction had to be strong for enabling sufficient sensitivity. This raised questions on the non-interfering nature of the method [3,4].

The lateral resolution of SThM is generally limited by the tip apex geometry and increases with the sharpness of the probing tip. Therefore, a gain in spatial resolution leads to an increased thermal resistance R_{ts} between the tip and the sample. While this reduction of the contact area reduces any interfering interaction, it prevents equilibration of the tip with the sample (see Figs. 1(b) and 3), which means that the sensor signal is proportional to a heat flux. This heat flux is not only a function of the temperature difference between sample and probe but of R_{ts}, which is sensitive to the local properties of the sample, like thermal conductivity, topography, elasticity and roughness (see Fig. 2). Accordingly, knowledge of $R_{ts}(x,y)$ at every location on the sample is necessary (see Fig. 4) to infer the local temperature of the sample temperature. To resolve device structures on the nanoscale tip apex diameters below 10 nm are typically needed, and R_{ts} lies in the range of 10^8 to 10^9 K/W. As the thermal insulation of the sensor to the reservoir R_{cl} is typically only $10^4 – 10^5$ K/W, dedicated measurement equipment is required.

We have developed a method [6] tackling these issues using a vacuum-based microscope [7] in a low-noise environment [8]. As shown in Fig. 1, the sensor temperature $T_{heater/sensor}$ is measured through its electrical resistance R_{heater}, and R_{cl} is known through calibration. In our method, the sample temperature is periodically modulated (e.g. via a device current), such that both a DC and AC signal amplitude can be extracted simultaneously and without any prior assumption on $R_{ts}(x,y)$. Depending on how the chosen modulation frequency compares to the thermal time constant of the device under investigation, either a quasi-static case or non-equilibrium situations can be studied.

The method has been applied to study self-heating of semiconductor nanowires [6], metal interconnects [7], phase change memory devices (below), and spin valves [9]. The resolution demonstrated is <10 nm laterally and ~mK thermally with a bandwidth of 1 kHz [7]. The method allows for discrimination of temperature changes due to Joule heating and Peltier effects [6]. Through comparison with numerical simulations in model systems, it was shown that the method can operate quantitatively and non-interfering. In the following, we provide examples of measure-ments on operating nanodevices and use SThM to detect device failure and manufacturing issues.

3. III. Examples

Indium Arsenide (InAs) nanowires (NWs) have been considered as a channel material in tunneling field effect transistors (TFETs), for opto-electronic applications and for thermoelectrics. Here, we studied the local self-heating properties of simple devices fabricated from InAs NWs. Devices were prepared by the following steps: The NWs where grown by metal-organic chemical vapor deposition. After depositing of the NWs on the substrate, contacts were defined by electron beam lithography Between stripping of the resist and deposition of the Au/Ni contacts, a BHF etching step was performed on the exposed contact areas of the NW. Although the etching step did not alter the electrical properties measurably, it can strongly affect the heat dissipation properties as illustrated by SThM studies on NW devices of different channel length (Figs. 6 and 7).

The NW in Fig. 6(a) is located on a back-gated SiO_2 substrate. An alternating voltage bias is applied between the two contacts and the change in temperature due to Joule (along the nanowire) and Peltier effects (at the contacts) are quantified by SThM. Fig. 6(b) shows height profiles along the NW length direction extracted from 6(e). The spatial variation in topography relates to rather strong variations in R_{ts} (c,f). These variations, however, do only weakly interfere with the derivation of the local temperature from the collected data. From the measured local temperature fields (g,h), the thermal conductance into the substrate can be extracted, regarded from the deviation from a parabolic and linear temperature profile (d) for Joule and Peltier effects, respectively. Even heat spreading in the dielectric substrate is visible (h) and carries information about the device's thermal coupling to the underlying substrate.

Apart from quantifying temperature in operational devices, SThM-based thermometry can also be used to detect manufacturing issues. An example is given in Fig. 7(a) were a NW with locally reduced substrate coupling in the contact region is studied (see also height profiles in Fig. 7 (b)). The reduced substrate coupling is due to the BHF etching step and leads to an entirely different temperature profile compared to the expected (parabolic) case shown in Fig. 6(d). Also the Joule heat dissipation along the NW may be homogenous (ideal case), processing-induced variations can strongly influence the device thermal properties on very local scale (see Fig. 8). So far, no other method was able to spatially resolve these local (Joule) hot spots and interface-located Peltier effects at this spatial resolution and thermal sensitivity.

In a final example (Fig. 9), we illustrate self-heating of phase-change memory material. A single-crystalline thin film of vanadium dioxide (VO_2) with a thickness of 15 nm was deposited onto a titanium dioxide (TiO_2) substrate using pulsed laser deposition. Rectangular structures of the film were then defined with photolithography (NH415 resist and Ag/CF4 reactive ion etching). Finally, Au/Cr contacts were defined to form thin-film resistor structures. VO_2 features a current-induced metal-insulator transition leading to an S-shaped current-voltage (IV) characteristics. Because of its unique characteristics, VO_2 resistors have been considered for spiking neuron devices [10]. In contrast to crystalline-amorphous phase-change materials, the nucleation of current filaments in thin films is not well studied. In this example, self-heating around current filaments is measured as shown in Fig. 9. For the same current, and depending on the number and diameter of the current filaments, the temperature rise may vary by an order of magnitude as observable in the two segments of VO_2 observed.

4. IV. Conclusion and Outlook

The examples show that SThM has the capability to resolve temperature fields at <10 nm and mK resolution with outstanding versatility. The notion of equilibrium thermometry is replaced by the dynamic measurement of heat flux through a tip-sample contact with variable thermal resistance. The SThM method is yet far from its fundamental physical limitations. We expect further improvements in lateral resolution to the single nanometer and an increase in bandwidth beyond 1 MHz.

Interestingly, the temperature maps carry information on thermal conductance properties at various interfaces and boundaries of nanoscale devices, even if these interfaces are buried inside device structures. (However, like any other mapping technique, SThM does not resolve deeply buried structure.) Finally, device failure mechanisms and processing issues can be detected in thermal maps with information far exceeding what is possible analyzing electronic transport data alone.

Acknowledgment

This work was supported by the European Union FP 7th project NANOHEAT (Grant Agreement No. 318625), by the Swiss National Science Foundation (Project No. 134777), by the Swiss Federal Office of Energy under Grant Agreement No. SI/501093-01, and by the European Union H2020 project CONNECT (Project No. 688612).

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Technique: / Demand:	Imaging techniques			Local techniques	
	Optical methods • Raman thermometry [1] • IR-microscopy [2] • Thermoreflectance[3]	**Electron microscopy**	**Scanning probe microscopy** • SThM * • SJEM • SNOM	**Self-sensing thermometry** • 3-Omega • Voelklein	**Contact** • **fluorescent particle and opt. readout** • **thermo elements**
Lateral resolution <10 nm	X	✓	✓*	n.a.	n.a.
Temperature resolution	mK	mK	mK	µK	mK
Temporal resolution	DC - GHz	DC - MHz	DC - MHz	DC - GHz	DC - GHz
Materials: works on all materials (semiconductor, metal, dielectrics, organics …)	X[1] ✓[2,3]	X	✓*	X	X
Flexible wrt device geometry (e.g. devices on wafer surfaces)	✓	X	✓*	n.a.	✓
Buried structures	X	X	X	✓	X
Non-interfering	✓	✓	✓*	n.a.	(✓)
Quantitative	✓	✓	✓*	✓	✓

Table 1. Different thermometry techniques evaluated for requirements of nanodevice characterization. A more detailed comparison may depend on the exact application. Moreover, considering the complexity and the recent activity of the field [3,4], table1 may be incomplete. Aspects marked with * are discussed in this article.

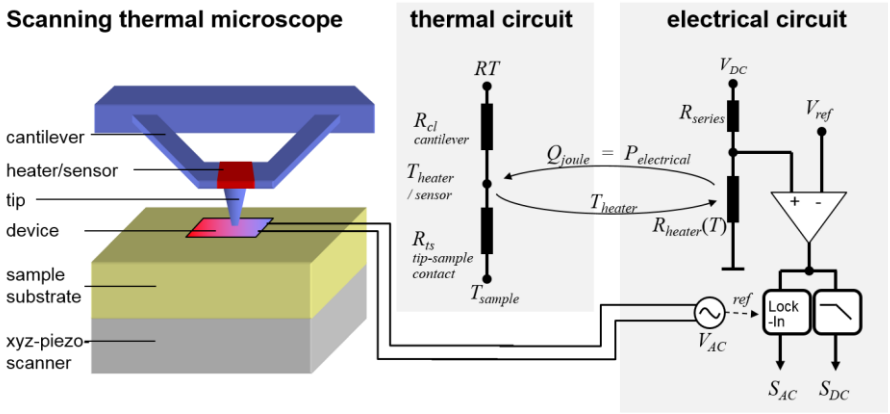

Fig. 1. Experimental arrangement of SThM applied to in-situ thermometry of nanodevices. Schematically, the mechanical setup, and the thermal and electrical circuits are shown.

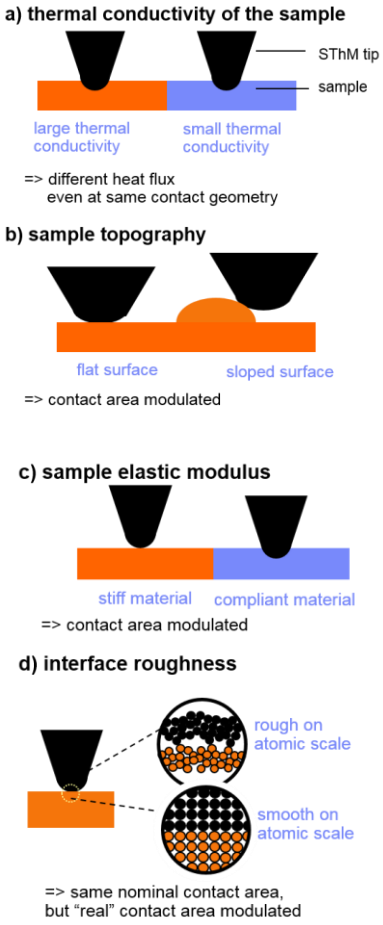

Fig. 2. Factors influencing the thermal resistance of the tip surface contact R_{ts}. Contributions to R_{ts} from tip, interface and sample scale in different ways on the properties of the contact.

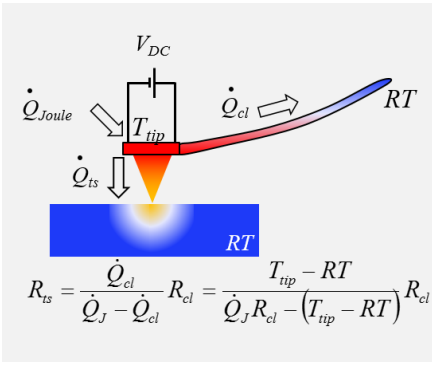

Fig. 3 Passive SThM measurement mode: Conventionally used to measure thermal resistance of the tip-surface contact R_{ts}. For interpretation, the contributions of the tip and the interface to R_{ts} need to be considered.

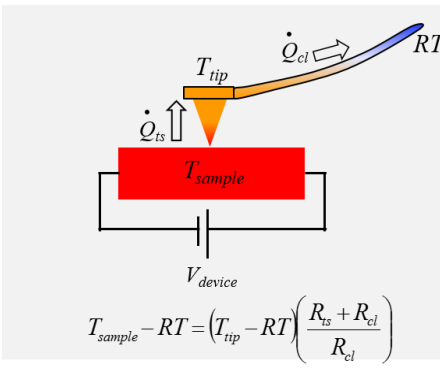

Fig. 4. Active SThM measurement mode: Conventionally used to measure the sample temperature. However, knowledge of the thermal resistance between tip and sample R_{ts} at each sample location is required.

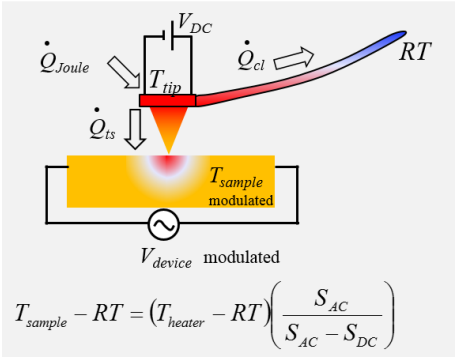

Fig. 5. Novel operation mode presented combining both active and passive mode and able to measure device temperatures free from common topography influences (as shown in Fig. 2.) extracting both R_{ts} and T_{sample}.

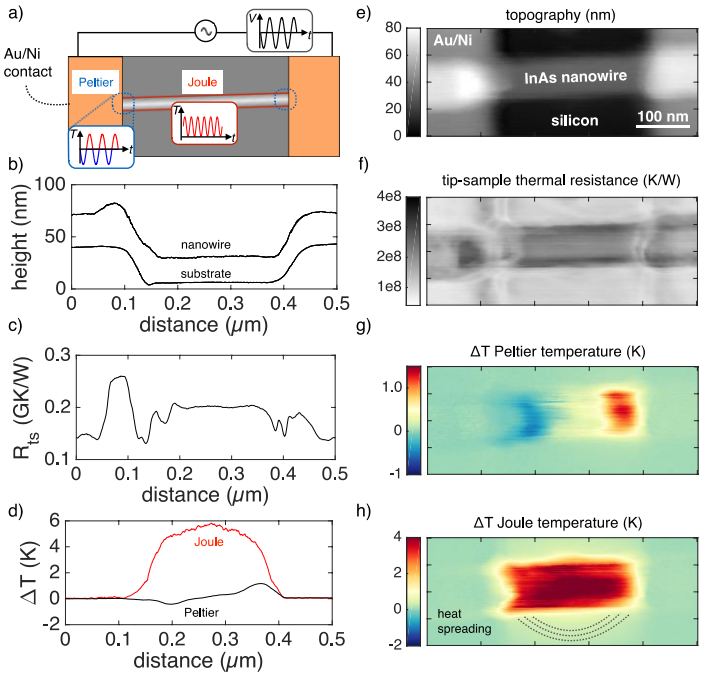

Fig. 6: (a) Illustration of the experiment (b) height profiles of an InAs nanowire (23 nm diameter) on a silicon oxide substrate contacted by Au/Ni electrodes, (c) tip-sample thermal resistance profile, (d) Peltier and Joule temperature profiles along the nanowire, (e) height and (d) thermal resistance images compared to (g) temporal snapshot of the Peltier temperature field at maximum excitation amplitude, (h) amplitude of the Joule temperature field with heat spreading into the substrate.

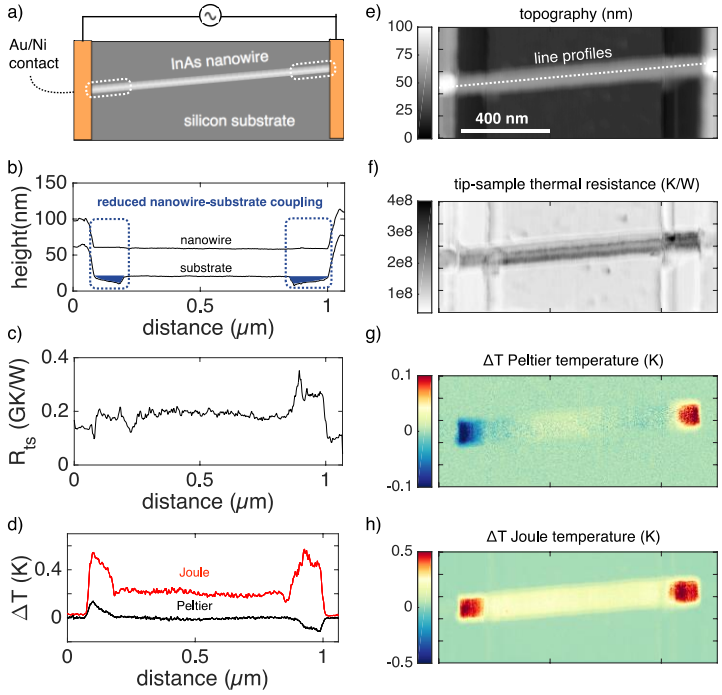

Fig. 7: (a) Illustration of the NW with locally reduced substrate coupling near the contacts due to BHF etching (b) height profiles of an InAs nanowire (40 nm diameter) on a silicon oxide substrate contacted by Au/Ni electrodes, (c) tip-sample thermal resistance profile, (d) Peltier and Joule temperature profiles along the nanowire length direction, (e) height and (f) thermal resistance images compared to (g) temporal snapshot of the Peltier temperature field at maximum excitation amplitude, (h) amplitude of the Joule temperature field with heat spreading into the substrate

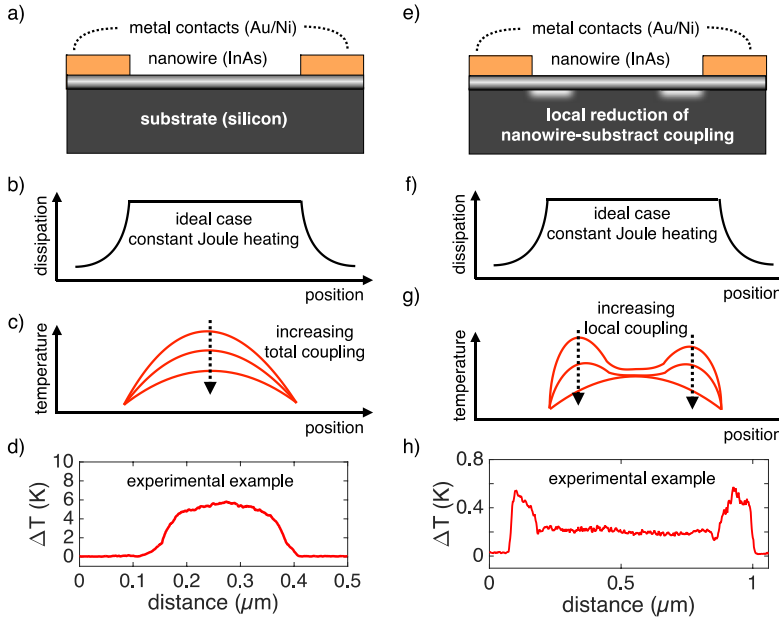

Fig. 8: Temperature profiles along InAs NW channels for different situations. (a) Schematic of layout of NW sample on substrate with contacts. (b) Ideal case: homogenous heating leads to bell-shaped temperature profile. The shape carries information on substrate coupling (c) which could be inferred from experimental data like that in (d). In comparison (e) shows the case for a NW with locally reduced substrate coupling due to a BHF etching step. Assuming same heat dissipation along the NW as in (a), increase of local temperature near the contacts as shown in the experiment (h) can be observed.

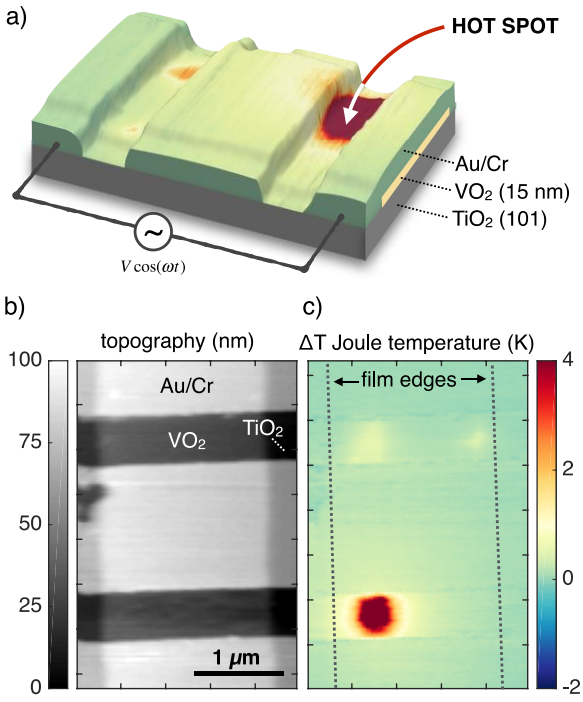

Fig. 9: Self-heated vanadium dioxide (VO_2) phase change resistor (a) Illustration of the experiment with the VO_2 phase change film contacted by Au/Cr electrodes (b) height image of the structure (15 nm VO_2 film thickness) on a titanium oxide substrate (c) steady-state Joule temperature field with a hot spot formed between two electrodes and increased heat dissipation near the film edges.