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Research Report

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***Abstract*— Tunnel diodes are of interest to gain insights into the limitations of tunnel field effect transistors (TFETs) as they enable us to distinguish effects of the heterojunction from device parasitics found in a three terminal device. In the present work, we report on InAs/GaSb nanowire heterojunction tunnel diodes monolithically integrated on silicon-on-insulator substrate (SOI). The nanowires were grown using template-assisted selective epitaxy (TASE). Temperature dependent I-V measurements show a change in the conductance slope due to the presence of defects at the heterojunction. Comparison with TFETs results shows a similar temperature dependence of the slope, but with smaller absolute values. We further performed room temperature pulsed I-V measurements on the same diodes to analyze trap contributions and we observed no significant dependence on pulse time down to 10µs.**

Keywords-III-V; diode; nanowire; TFET; conductance slope; tunneling;

I. INTRODUCTION

The tunnel field effect transistor (TFET) is a promising solid-state switch for ultra-low power operation [1-2].

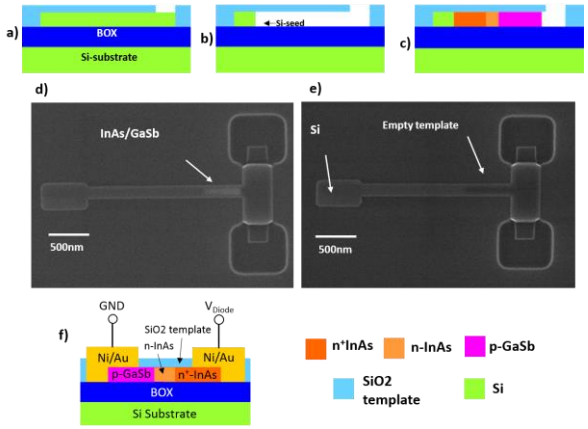

Figure 1. Process flow of n^+-n-p InAs/GaSb diodes fabricated by TASE. Lateral section schematic of a) Si nanowires covered by 80 nm thick SiO_2 template b) TMAH Si etch-back, c) III-V grown by MOCVD, d-e) SEM top-view of step b-c), f) finished device including Ni/Au contacts.

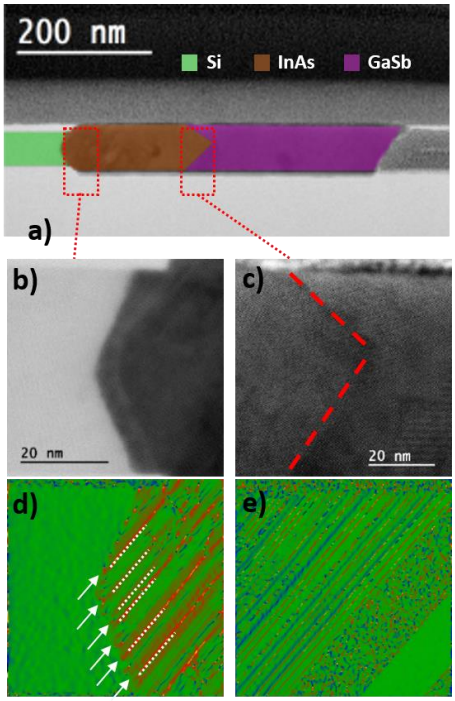

Figure 2. STEM images of InAs/GaSb hetero-structures from [6]. a) Lateral bright-field false colored STEM image of the nanowire. Magnification of the b) Si/InAs interface, c) InAs/GaSb interface, and corresponding Geometrical Phase Analysis (GPA) d), e). A V-groove <111> shape of Si is seen in b), as well as the presence of misfit dislocations highlighted with white arrows at the Si/InAs nucleation interface d). The InAs/GaSb interface is characterized by presence of planar defects propagating over the GaSb segment e).

TFETs are based on band-to-band tunneling (BTBT), which works very efficiently in InAs/GaSb heterojunctions because of the broken band alignment combined with the small effective tunneling mass, typical of III-V semiconductors. This current transport mechanism could enable in principle subthreshold swings steeper than 60 mV/dec at room temperature, representing instead the intrinsic limit for MOSFET devices based on thermionic emission. Achieving low-power switching with sub-60 mV/dec operation is

nowadays a key target for beyond-CMOS steep-slope devices. Investigation of two-terminal diodes is useful to understand the impact of the junction band alignment and heterojunction defects, as non-idealities related to gating and oxide traps may be neglected. Agarwal et al. [3] introduced the conductance slope (C_{slope}) concept, in analogy to the subthreshold swing (SS) of a TFET. This quantity allows to correlate the negative differential resistance (NDR) region of a tunnel diode to the reverse bias region of a TFET, by means of the existing relationship between the tunneling joint density of states and the absolute conductance I/V. Although quantitatively different, the steepness of both provides an estimate of the interface quality and the impact of traps on the tunneling mechanism. In the present work, we fabricate and characterize n^+-n-p^+ InAs/GaSb tunnel diodes and discuss their electrical behavior through temperature dependence measurements and pulsed I-V measurements. We also show a preliminary evaluation of the passivating effect provided by the oxide template on the III-V surfaces.

II. DEVICE STRUCTURE

The InAs/GaSb nanowire tunnel diodes investigated in this work are fabricated on SOI substrates using TASE. A schematic of the process flow is shown in Fig. 1 whereas the detailed fabrication steps are reported elsewhere [4-5]. The nanowires are patterned by HSQ and e-beam lithography on the SOI substrate and covered by 100 nm SiO2 template, obtained with ALD and PECVD TEOS (Fig.1a). Small opening windows in the SiO_2 are patterned at one end of the nanowires with e-beam lithography and etched by BHF. The silicon inside the tubes is back etched with a 2% TMAH solution (Fig. 1b). Before growing the III-V, a short DHF dip is needed to get rid of the native oxide covering the silicon seed. On the same chip, different diameter structures were patterned, but the highest yield was achieved only for the thickest nanowires.

The p-n-n+ (GaSb/InAs/InAs) diodes were grown by metal-organic chemical vapor deposition (MOCVD) in one single growth run, first InAs on Si and then GaSb on InAs (Fig.1c). The nanowire cross section is 30nm×80nm. Both segments were doped using Silane (Si2H6) as precursor. The estimated doping levels are $4{\cdot}10^{18}$ cm^{-3} for the n^+-InAs, $1{\cdot}10^{17}$ cm^{-3} for the unintentionally doped InAs and low $5{\cdot}10^{17}$ cm^{-3} for the p-GaSb. Scanning transmission electron microscopy (STEM) analysis of the heterointerface on measured diodes is shown in Fig. 2. As expected, misfit dislocations are present at the Si/InAs interface because of the high lattice mismatch, while planar defects propagating in the GaSb segments originate from the InAs/GaSb interface. After the growth and prior to contacting, a sulphur passivation step is used to obtain a better contact resistance. Ni/Au contact pads and wiring were fabricated by e-beam evaporation and lift-off. In

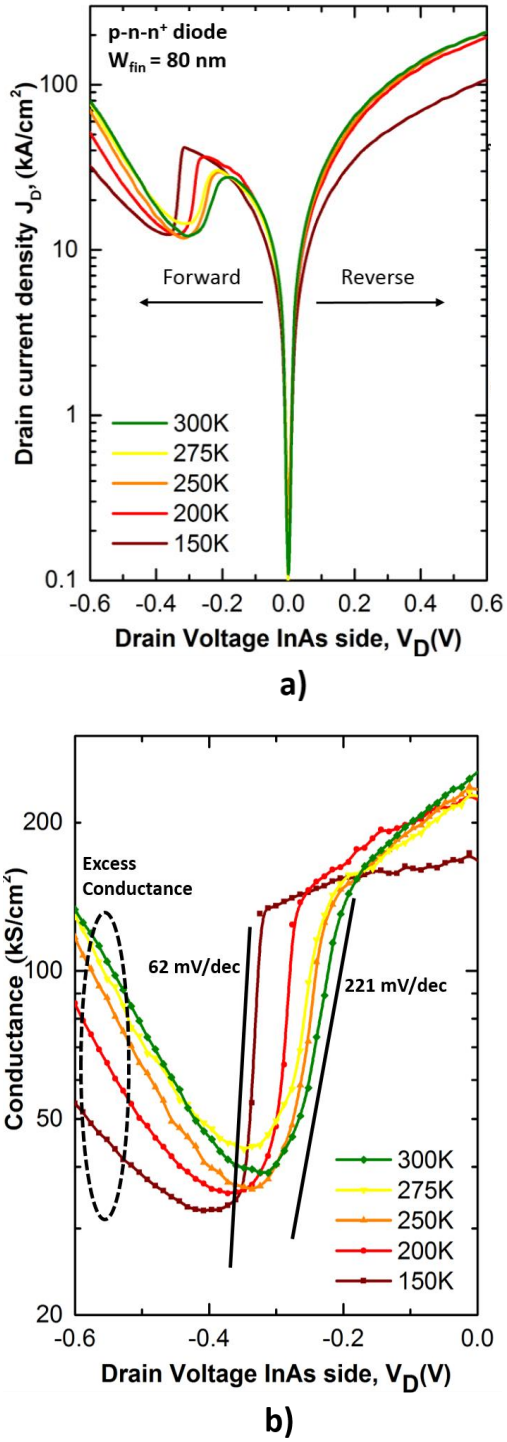

Figure 3. Temperature dependent electrical measurement of a p-n-n^+ diode with nanowire width 80 nm. a) I-V characteristic in semilog-scale. b) Absolute conductance vs. applied bias from the same diode. For 300 K and 150 K plots an average conductance slope is extracted from I_{peak} to I_{valley} and marked by black bars. For lower temperatures, there is an improvement in the conductance slope and less excess current contribution.

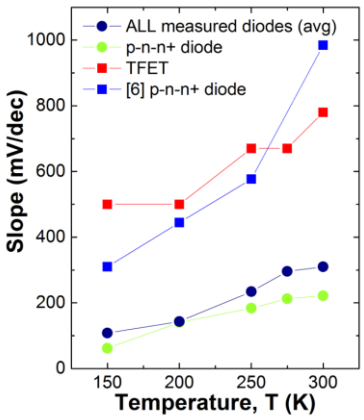

Figure 4. Comparison of the C_{slope} trend with the temperature for the diode in Fig. 3 (green line), average of all the measured diodes in present batch (blue line), diode reported in [6] (light blue line), with the SS trend of the InAs-GaSb n-TFET in [7] (red line). The slope for the diodes presented in this work is four times lower than the one obtained for TFETs, while the trend is the same in all cases. The improvement of the conductance slope with respect to our previous diodes is also evident.

the electrical DC measurements shown in the following sections, a bias is applied to the n-InAs "drain" side of the nanowire while the "source" side (p-GaSb) is grounded; consequently, the negative voltage branch corresponds to the diode forward region and vice versa.

III. Experimental Results

Temperature-dependent I-V measurements were performed on these devices, down to 150K. Fig. 3a shows that the peak-to-valley current ratio (PVCR) increases from 2.3 to 3.4 by lowering the temperature. In Fig. 3b the conductance slope is plotted and shows that it improves from 221 mV/dec at 300K to 62 mV/dec at 150 K. The temperature dependence of the C_{slope} indicates that impurities are limiting the steepness of the tunneling mechanism at the heterojunction and that they contribute less for lower temperatures. In the forward bias region (high negative voltage), the excess current

Ref.	Growth	Substrate	Geometry	NDR	J_{peak} [kA/cm²]	PVCR
[8]	MOVPE	GaAs	50 nm vertical NW	yes	67.0	2.1
[9]	MBE	GaSb	1 µm² area	yes	500.0	3.4
[10]	MBE	GaAs	0.875 µm² area	no	-	-
[11]	MOCVD	GaSb	InAs film, 10µm diam.	yes	12.0	1.1
This work	MOCVD	Si	80 nm lateral NW	yes	26.6	2.3

Figure 5. Benchmark for InAs/GaSb based tunnel diodes with focus on key technology parameters, i.e. PVCR, peak current density and integration on Si. Our tunnel devices are monolithically integrated on Si and compared to other works they show lower current densities but good PVCR.

contribution is decreasing with the temperature and this effect contributes to give a steeper tunneling slope. The peak current in the NDR region is higher for lower temperatures, as reported in previous works [11], where this is attributed to the lower effect of thermal tails that allow more carriers to be in the tunneling energy window. Compared to previous diode structures from our group [6], the C_{slope} is three times steeper at room temperature due to an increased doping level. Fig. 4 compares the C_{slope} of diodes to SS of TFETs from [7]: both improve with decreased temperature, but C_{slope} of the new diodes is significantly steeper. A benchmarking of InAs/GaSb tunnel diodes reported in literature up to now is shown in Fig. 5. The diodes presented in this work have good PVCR compared to other works, while the current density could be still improved. On the other side, our technology platform allows to monolithically integrate these devices directly on SOI substrates. Pulsed I-V characteristic is shown in Fig. 6a. Pulsing can reduce the contribution of some parasitic tunneling mechanisms which is expected to give a lower excess current. However, an apparent improvement in C_{slope} is only detected in few devices (Fig. 6b) and needs more investigations. The excess current is not changing with the pulse duration. The settling time depends on the measurement range so appropriate wait time must be considered to obtain accurate results. In this case, the current range allowed only 10us as minimum pulsing time. The low absolute current of the single nanowire devices limited the ability to go to higher frequencies, which can be circumvented by using nanowire arrays in the future.

In the previous work about InAs/GaSb n-TFET from our group [7], the gated nanowire devices never show an NDR tunneling feature in forward operation. The TFET

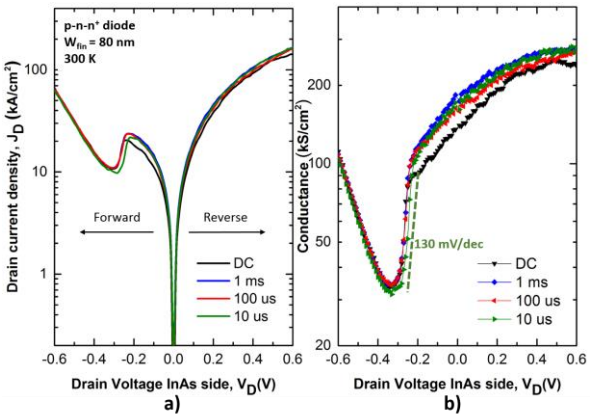

Figure 6. Pulsed I-V measurement of a p-n-n+ diode with nanowire width 80 nm. a) I-V characteristic in semilog-scale. b) Absolute conductance vs. applied bias of the same diode. The characteristics show a slight improvement in PVCR (1.92 to 2.27) and independent slopes for this device. The excess current does not show a significant pulse duration dependence as well.

fabrication process flow requires the strip of the oxide template prior to gate and contacts processing. In Fig. 7a is reported the room temperature DC characteristics of different tunneling diodes (p+/n+) with and without the template (red and blue lines respectively). The SiO_2 was wet etched in BHF. The diodes protected by the oxide shell always show an NDR, while this feature is less evident when their surfaces are exposed to air. The absence of the NDR can be related to the higher excess current contribution or to a change in the Fermi level position induces by surface reconstruction processes; the effect of keeping the oxide template on the device acts as passivation, by preserving surfaces pristine and with reduced dangling bonds. This preliminary investigation might be pursued by measuring this effect on the same device, where the template would be first removed and then re-deposited.

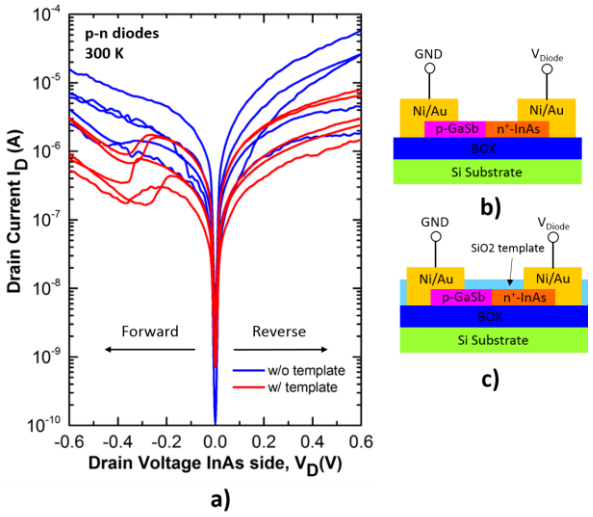

Figure 7. a) I-V characteristic in semilog-scale of different p-n^+ diodes with the template (red lines) and without the template (blu lines). The devices without the template are not showing NDR. The SiO_2 shell provides a passivation of the dangling bonds on III-V surfaces. b-c) schematic of the two diodes considered in this comparison. The two devices types have been fabricated on two different chips.

IV. Conclusion

In conclusion, we have investigated the electrical properties of monolithically integrated InAs/GaSb tunnel devices on SOI substrate. Analysis of the temperature dependence of the C_{slope} and of the PVCR reveals that defects at the heterointerface and non-abrupt band edges are limiting performance similarly to TFETs, but that C_{slope} achieved in the two-terminal device is steeper than SS. Furthermore, the oxide template provides a good passivation for the III-V surface and this has direct impact on the electrical characteristic of these structures.

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