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Research Report

Monolithic integration of III-V nanostructures for electronic and photonic applications

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Monolithic integration of III-V nanostructures for electronic and photonic applications

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We have recently developed a novel III-V integration scheme, where III-V material is grown directly on top of Si within oxide nanotubes or microcavities which control the geometry of nanostructures. This allows us to grow III-V material non-lattice matched on any crystalline orientation of Si, to grow arbitrary shapes as well as abrupt heterojunctions, and to gain more flexibility in tuning of composition. In this talk, applications for electronic devices such as heterojunction tunnel FETs and microcavity III-V lasers monolithically integrated on Si will be discussed along with an outlook for the future.

Introduction

Silicon is the material of choice for the electronics industry, and this technology has been optimized to perfection throughout the past half century. However, as we move beyond conventional silicon CMOS there is a rising interest in integrating other materials on the Si substrate. In particular, co-integrated III-V materials could strongly enhance electronic properties by providing increased electron mobility or tunable heterostructures, or add additional functionality for silicon photonics via integrated direct bandgap materials.

We have developed a method for monolithic III-V on Si growth, where we grow the III-V material within lithographically defined oxide cavities [1-4]. This provides us with a high degree of control and versatility, while eliminating some of the constraints associated with either buffer layers or traditional selective area growth of nanowires. This method has been employed to demonstrate various electronic devices ranging from high performance InGaAs nFET [4], complementary III-V heterostructure TFETs [5] to ballistic transport in one-dimensional InAs NWs [6]. Recently, we have also expanded this technology to optically active devices, enabling monolithically integrated μ-cavity GaAs lasers showing lasing at room temperature [7] and providing the potential for more complex photonic structures by developing this technology as a virtual substrate approach [8-9].

Here, I will primarily cover the fabrication method in its various embodiments, including the ability to achieve heterostructures and their use for tunneling devices. The requirements specific to photonic structures will be discussed and the most recent results in this domain will be shown.

Template Assisted Selective Epitaxy (TASE)

The implementations of TASE in a planar orientation and using a substrate seed is illustrated in Fig. 1, a more detailed description can be found in references [3-4]. A hollow SiO_2 template structure is fabricated by a series of lithographic and etching steps. It contains a small Si seed area either at one extremity of the hollow or via a small opening to the underlying substrate. The template is epitaxially filled using metal-organic chemical vapor deposition (MOCVD). The growth starts from the Si seed, which assures a single nucleation point. Since the resulting large crystal is expanded from one nucleation point, typical defects found in planar epitaxy are absent. Furthermore, the oxide template guides the growth and hence controls the geometry of the final nanostructure directly. The presence of the template also prevents the lateral overgrowth often associated with NW growth. By changing the precursor flow during growth, we may incorporate homo- or heterojunctions in the III-V material.

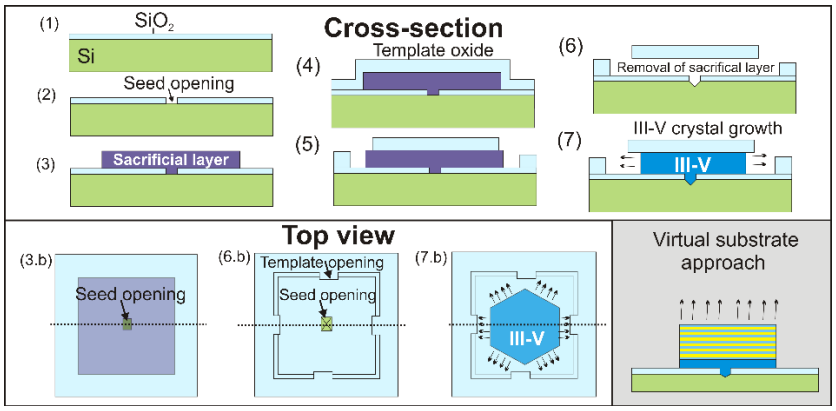

Figure 1 Schematics illustrating the concept of TASE as implemented on a conventional Si substrate using a substrate seed. The cavity is defined by patterning a sacrificial layer and covering it with oxide. The sacrificial layer is then subsequently removed to reveal the seed and III/V material is regrown. The inset in the bottom right corner illustrates the virtual substrate approach.

Materials, heterojunctions and devices

For different applications, we have explored TASE growth of the In(Ga)As and In(Ga)Sb families as well as InP for virtual substrates. Misfit dislocations which relax the strain between the materials are present and confined to the Si/III-V interface. In the smaller electronic structures, we do not observe propagating dislocations or anti-phase boundaries. By consecutively opening different templates it is possible to serially grow different III-V materials or combinations thereof on the same wafer. This approach is illustrated in Fig. 3.a, where first InAs NWs were grown and then covered by a protective oxide. Neighboring templates were opened and the Si was etched back to the seed, followed by a second MOCVD growth of GaSb [11].

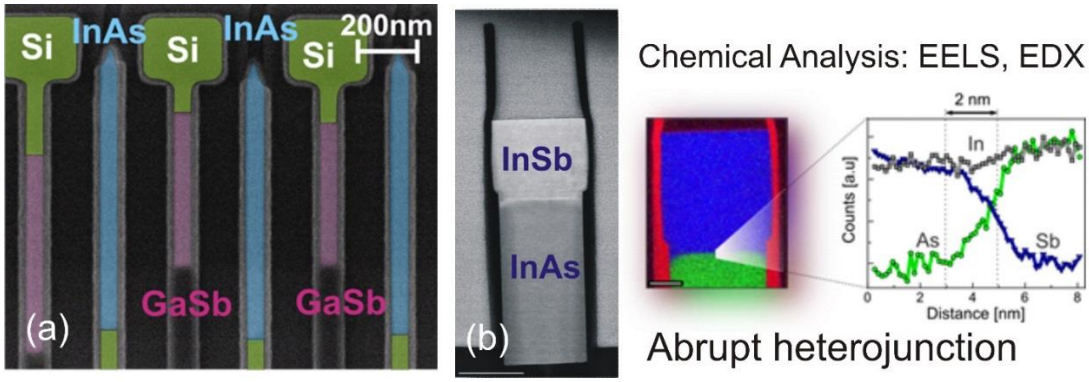

Figure 2 (a) Integration of two different III-V materials by consecutive growth sequences, InAs is grown first, then covered by a protective oxide, and then GaSb is grow in the neighboring oxide tubes [11]. (b) Using this approach, very abrupt heterojunctions may be achieved, here it is illustrated by a HRTEM image of a vertical Insb/InAs – EELS and EDX is performed by L. Gignac, IBM Research Yorktown.

A further advantage is the ability to achieve very sharp homo- and heterojunctions due to the lack of catalysts. This is illustrated in Fig. 2.b for the case of InSb/InAs junctions.
The steep junctions are particularly important for tunneling devices, such as the InAs/Si p-TFET shown in Fig. 3. Fig. 3.c shows the subthreshold swings of two identical devices designated as DF41 and FF41, it can be observed that the devices still do not achieve sub-thermionic switching as it is limited by traps associated with the InAs/Si heterojunction. Nevertheless, we demonstrated what we believe to still be the only scalable planar III-V heterojunction TFET.

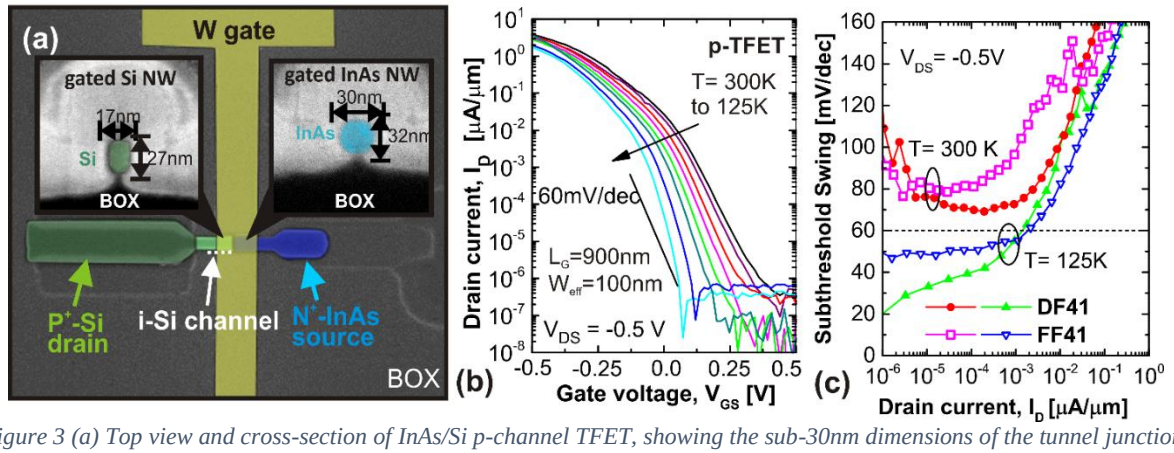

Figure 3 (a) Top view and cross-section of InAs/Si p-channel TFET, showing the sub-30nm dimensions of the tunnel junction. The n-channel counterpart consist of a gated InAs/GaSb heterojunction, [5].(b) Transfer characteristic as a function of temperature for a typical p-TFET. (c) subthreshold swing as a function of current for two representative TFETs, also from [5]..

Recently we have expanded this work to focus on optically active devices grown monolithically on Si. Fig. 4.a-c, illustrates work on devices based on a virtual substrate approach, where the virtual substrate is grown by TASE followed by subsequent μ-cavity or QW growth. Another route corresponds to directly growing a μ-disc laser as illustrated in Fig. 4.d. The GaAs mushroom shaped structure nucleates at a single seed on the Si substrate. In this device, GaAs grows into a single crystal and forms a microdisc cavity. Subject to increased optical excitation, a strong lasing peak emerges from the broad spontaneous emission background as shown in Fig. 4e). The Input-Output characteristics depicted in the lower panel of Fig. 4e) exhibits a characteristic S-shape recorded at 300K and demonstrates room temperature operation of the device. The larger geometries of the photonic structures sometimes result in crystal defects, suppressing lasing in some devices.

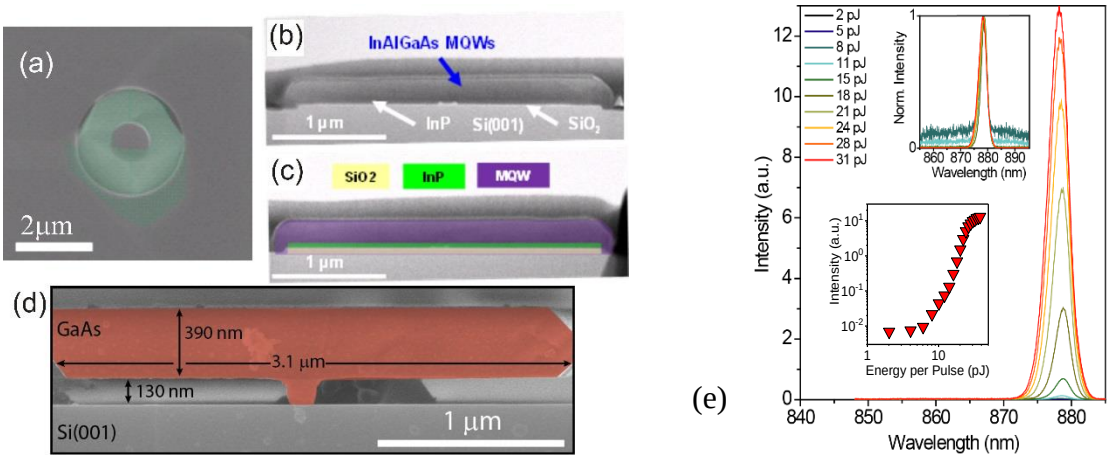

Figure 4 Different approaches for monolithic integration of III-V lasers on Si, from [7-9]. (a) Top-view SEM image of GaAs ring structure grown o Si using the virtual substrate approach. (b) Cross sectional TEM showing two III-V structures with caption, (c) (false colored) with overgrown InAlGaAs MQW stack on InP-OI. (d) Direct growth of GaAs μ-disc laser on Si. (e) lasing characteristics of GaAs μ-disc laser shown in (d).

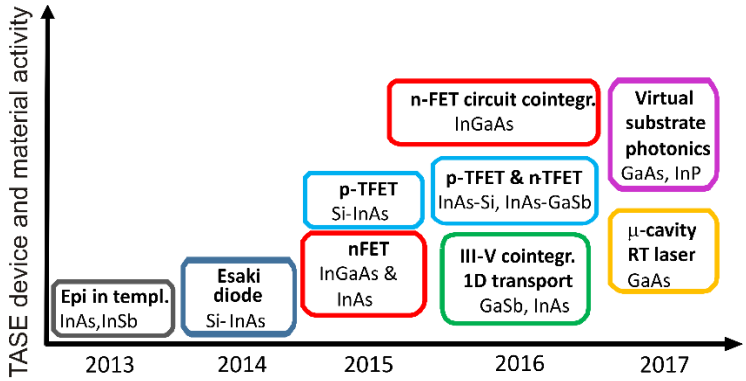

Figure 5 Evolution of TASE-based work, spanning growth, materials and device activities all with focus towards CMOS compatibility.

Conclusion

Monolithic III-V integration on Si using TASE is a very versatile integration method, suited for the seamless integration of high-quality III-V nanostructures with Si devices. Abrupt heterojunctions have been demonstrated as well as stacked III-V NWs and multiple III-V integration on a single Si substrate. As it can be seen in Fig. 5 which portrays the timeline of our device and material focus, it was originally developed for electronics but we are now also exploring active photonic devices.

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