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Research Report

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InGaAs-on-Insulator MOSFETs Featuring Scaled Logic Devices and Record RF Performance

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Abstract

We demonstrate scaled InGaAs-on-insulator FinFETs and planar MOSFETs on Si substrate for low power logic and RF applications. This Si-CMOS compatible technology implements SiN_x source-drain spacers and doped extensions for reduced overlap capacitances. FinFETs with performance for logic applications matching state-of-the-art are demonstrated. Simultaneously, f_t and f_{max} of 400 and 100 GHz are achieved respectively, the highest reported f_t for a III-V MOSFET on Si. Finally, we explore the use of an extended gate line to reduce gate resistance, offering balanced f_t/f_{max} of 215/300 GHz, the first report of III-V RF devices on Si matching state of the art Si-CMOS.

Introduction

High electron mobility III-V materials such as $In_xGa_{1-x}As$ are considered as replacements for strained Si in nFETs for low power logic applications [1]-[3]. Their superior electron transport properties also make them suitable for RF applications, enabling high-frequency and low-noise functionality [4]. However, a Si CMOS-compatible III-V-on-Si RF-MOSFET technology matching the RF performance of Si-CMOS has not yet been shown. In this work, we demonstrate an InGaAs FET technology enabling scaled FinFETs for low power logic, and RF-MOSFETs for high-frequency applications integrated on the same Si wafer, with performance in both cases matching state-of-the-art.

Device Fabrication

Fig. 1 shows a schematic cross-section of a fabricated InGaAs-on-Insulator RF-MOSFET, and **Fig. 2** shows the layout schematic of RF devices. **Fig. 3** shows STEM images of a fabricated device. The corresponding CMOS-compatible fabrication flow is shown in **Fig. 4** and follows previous work [5] with the addition of three new modules: (1) SiN_x sidewall spacers for reduced parasitic capacitances, (2) doped RSD extensions under the spacers for reduced access resistance, and (3) a gate extension option for balanced RF performance. First, a 20-nm thick InGaAs layer is integrated on a Si wafer using direct wafer bonding [6]. This technique is compatible with large-scale Si substrates and 3D monolithic integration [7]. Subsequently, fins are dry-etched in logic devices, while RF devices remain planar. 3 nm SiN_x spacers (**Fig. 3c**) are formed by ALD and RIE followed by raised source and drain (RSD) epitaxy using a dummy gate. The $Al_2O_3/HfO_2/TiN$ gate stack is subsequently formed by an RMG process. Next, the W gate fill is performed, an interlayer dielectric (ILD0') is deposited, and M1 is patterned. For the RF-MOSFET option, the ILD0' is etched to access the W gate, and the gate extension metal is patterned. Subsequently, ILD1 is deposited, and the source sides of the gate fingers are connected by M2.

Results

Fig. 5 and **6** show output and subthreshold characteristics, respectively, of FinFETs for logic applications, with fin width of W_{fin} = 25 nm. At L_G = 30 nm, SS in saturation is 83 mV/dec., and at L_G = 120 nm devices exhibit SS_{sat} = 70 mV/dec. **Fig. 7a** shows minimum SS in the linear region and **Fig. 7b** shows I_{ON} (at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V) versus L_G for planar devices and FinFETs with different W_{fin}. $I_{ON} \approx 250$ µA/µm is demonstrated for W_{fin} = 25 nm and L_G < 30 nm, matching the state-of-the-art for scaled InGaAs FinFETs on Si [5], which does not utilize sidewall spacers. This shows that the doped RSD extensions introduced in this work effectively mitigate the expected increase of access resistance due to the SiN_x sidewall spacers. RF characteristics were obtained from S-parameter measurements up to 45 GHz, and small-signal modeling [8]. The pad parasitics were de-embedded using open-short de-embedding at the M2 level [9]. **Fig. 8a** shows a gain plot of a planar RF device with L_G = 30 nm at V_{DS} = 0.9 V, exhibiting f_t and f_{max} of 400 and 100 GHz, respectively, extrapolated at -20 dB/decade. This is the highest reported f_t for a III-V MOSFET on Si. **Fig. 8b** shows similar for a device with GE, exhibiting a more balanced f_t and f_{max} of 215 and 300 GHz, respectively, in line with Si 14 nm FinFET technology [10][11]. Here, f_{max} is obtained from a small signal model with a good fit to the measured S-parameters. Transconductance is g_m = 1.5 mS/µm at V_{DS} = 0.5 V. **Fig. 9** shows average values of f_{max} and f_t versus L_G with and without GE at V_{DS} = 0.7 V. The increased f_{max} is due to a reduction of R_G, while the decreased f_t is due to an increase of C_{GS}/C_{GD} from parasitic coupling to the GE metal. **Fig. 10** shows R_G versus L_G for devices with and without GE. The apparent increase of R_G at long channels comes from the fact that the modeled R_G contains a contribution from the channel resistance in series. The increase of R_G at very short L_G is in part due to short-channel reduction of g_m and in part by the reduced width of the gate metal. Short gate length also leads to the lower part of the gate being filled only by relatively resistive TiN, rather than both TiN and W as for longer L_G. R_G reaches a minimum of 12 Ω at $L_G \approx 50$ nm. For devices without GE, R_G is increased by ~60 Ω at short L_G. **Fig. 11** shows the gate-source capacitance C_{GS}, versus L_G with and without GE. The *y*-axis intercept represents the parasitic contribution to C_{GS}, i.e. from the RSD epi to the channel and gate metal and from the gate metal to the source/drain metal and the W plugs. Without GE, this value is $C_{GS,par}$ = 0.5 fF/µm, and with GE, it increases to $C_{GS,par}$ = 0.9 fF/µm, primarily due to increased coupling between the GE metal and the W plugs. **Fig. 12a** and **b** show f_{max} and f_t, respectively, versus V_{GS} and V_{DS} for a device with GE and L_G = 40 nm. **Table 1** shows a benchmark of state-of-the-art Si-CMOS RF as well as III-V-on-Si devices.

Conclusions

We have shown a Si-CMOS compatible InGaAs-On-Insulator MOSFET platform for RF and low power digital applications, as well as a gate extension technology to balance RF performance. Simultaneous f_t/f_{max} of 400/100 GHz as well as 215/300 GHz was demonstrated, together with strong logic performance in FinFETs, with $I_{ON} \approx 250$ µA/µm at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm.

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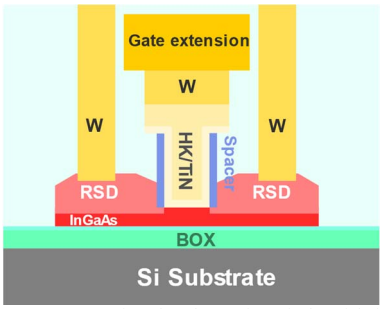

Fig. 1. Cross-sectional schematic of the fabricated InGaAs-on-insulator RF MOSFETs with gate extension. Logic devices include fins in the channel, tighter contact pitch and omission of the T-gate.

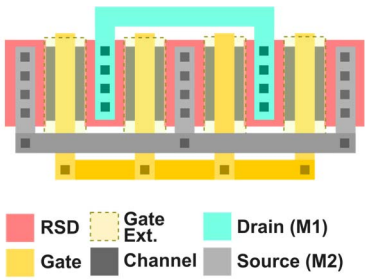

Fig. 2. Layout schematic of an RF-MOSFET with gate extension.

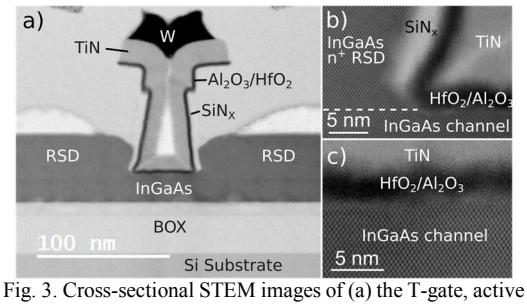

Fig. 3. Cross-sectional STEM images of (a) the T-gate, active region and BOX layer, (b) the RSD epi and the ~4 nm SiN_x spacers and (c) the channel and gate oxide.

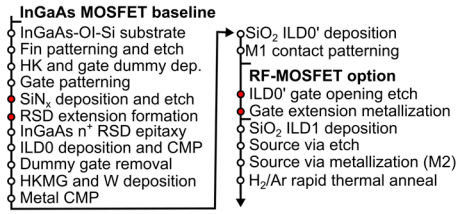

Fig. 4. Process flow overview for the fabricated devices up to M2, including an RF-MOSFET option. Newly introduced modules are highlighted in red.

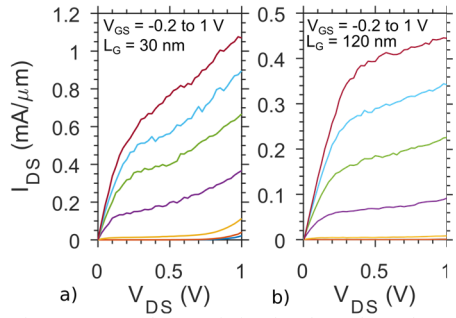

Fig. 5. Output characteristics for short channel and long channel logic devices (FinFETs) with W_{fin} = 25 nm and (a) L_G = 30 nm and (b) L_G = 120 nm.

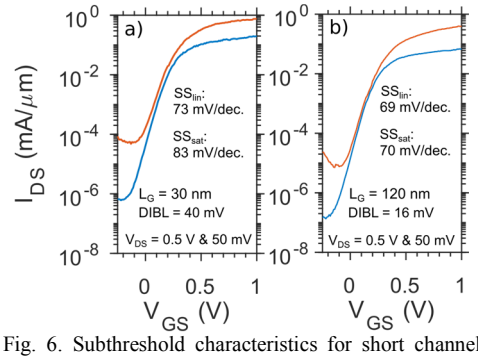

Fig. 6. Subthreshold characteristics for short channel and long channel logic devices with W_{fin} = 25 nm and (a) L_G = 30 nm and (b) L_G = 120 nm.

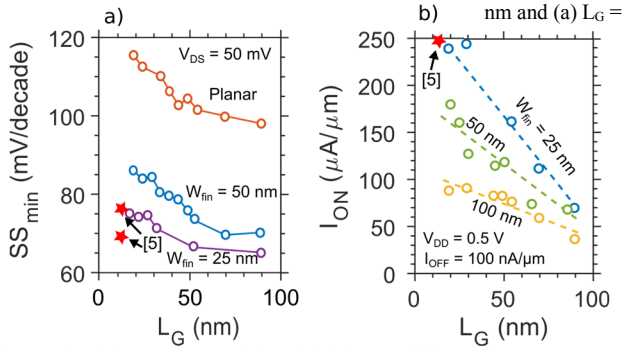

Fig. 7. (a) Minimum linear subthreshold slope and (b) on-current versus L_G for logic devices. Performance matches that of [5], which employs a similar technology but without the SiN_x sidewall spacers and doped RSD extension modules introduced in this work.

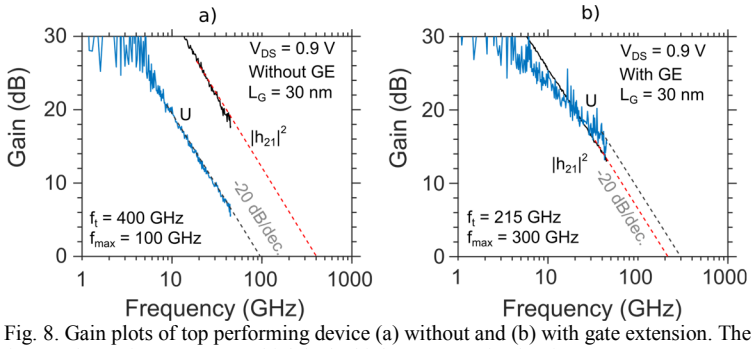

Fig. 8. Gain plots of top performing device (a) without and (b) with gate extension. The former shows f_t = 400 GHz, which is the highest reported value for a III-V MOSFET on Si, while the latter exhibits lower R_G with more balanced f_t/f_{max} matching Si CMOS.

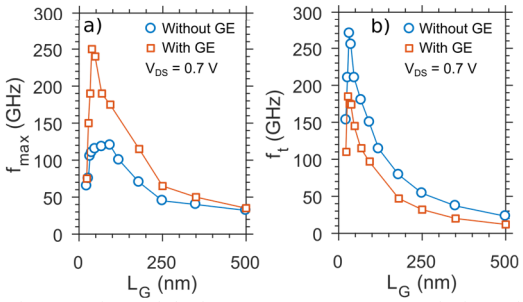

Fig. 9. (a) f_{max} and (b) f_t versus L_G at V_{DS} = 0.7 V, devices with and without gate extensions. The reduction of f_t at short L_G is due to short-channel effects reducing g_m.

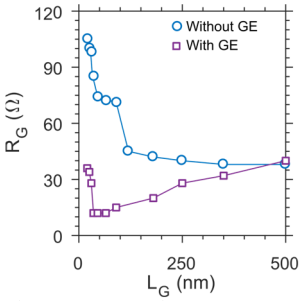

Fig. 10. Gate resistance versus L_G with and without GE.

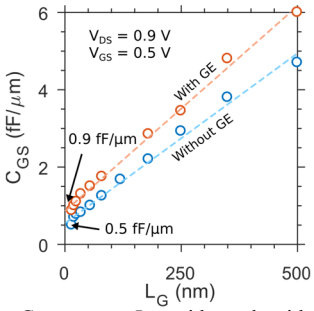

Fig. 11. C_{GS} versus L_G with and without gate extension. The increased C_{gs} leads to a reduction of f_t.

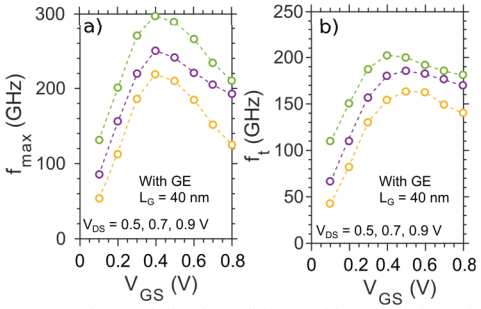

Fig. 12. (a) f_{max} and (b) f_t at different bias conditions for a device with gate extension.

Table 1. Benchmark of state-of-the-art Si and III-V technologies for logic and RF applications.

Technology	Platform	I_{ON} @ V_{DD} = 0.5 V & I_{OFF} = 100 nA/μm	f_t (GHz)	f_{max} (GHz)
This work	InGaAs on Si	250 μA/μm (L_G = 30 nm)	215	300
TSMC FinFET [2]	InGaAs on Si	300 μA/μm (L_G = 120 nm)	-	-
imec GAA [12]	InGaAs on Si	210 μA/μm (L_G = 46 nm)	-	-
Intel 22FFL [11]	Si	-	230	284
GF 14nm FinFET [10]	Si	-	314	180

[1] X. Sun et al., VLSI Tech. Dig., p. T3, 2017; [2] M. L. Huang et al., VLSI Tech. Dig., 2016; [3] C. Zota et al., IEDM Tech Dig. p. 3.2.1, 2016; [4] D. Kim et al., Applied Physics Lett., 101, 2012; [5] H. Hahn et al., IEDM Tech. Dig., 2017; [6] L. Czornomaz et al., IEDM Tech. Dig., p. 23.4.1, 2012; [7] V. Deshpande, IEDM Tech. Dig., p. 8.8.1, 2015; [8] I. Kwon et al., IEEE Trans. Microw. Theory Techn., 50, 2002; [9] M. C. Koolen et al., IEEE BCTM, p. 188, 1991; [10] J. Singh et al., VLSI Tech. Dig., p. T140, 2017; [11] B. Sell et al., IEDM Tech. Dig., p. 685, 2017. [12] X. Zhou et al., VLSI Tech. Dig., 2016.