RZ 3950 (#ZUR1804-013) 04/10/2018
Electrical Engineering 4 pages

Research Report

InGaAs FinFETs 3D Sequentially Integrated on FDSOI Si CMOS with Record Perfomance

C. Convertino, C. B. Zota, D. Caimi, M. Sousa and L. Czornomaz

IBM Research – Zurich
8803 Rüschlikon
Switzerland

This is the accepted version of the article published by IEEE: C. Convertino, C. B. Zota, D. Caimi, M. Sousa and L. Czornomaz, "InGaAs FinFETs 3D Sequentially Integrated on FDSOI Si CMOS with Record Perfomance," Proc. 2018 48th European Solid-State Device Research Conference (ESSDERC). 10.1109/ESSDERC.2018.8486862

InGaAs FinFETs 3D Sequentially Integrated on FDSOI Si CMOS with Record Perfomance

C. Convertino, C. B. Zota, D. Caimi, M. Sousa and L. Czornomaz
IBM Research Zurich, Rüschlikon, Switzerland
e-mail: ino@zurich.ibm.com

***Abstract*— In this paper, we demonstrate InGaAs FinFETs 3D sequentially (3DS) integrated on top of a fully-depleted silicon-on-insulator CMOS. Top layer III-V FETs are fabricated using a Si CMOS compatible HKMG replacement gate flow and self-aligned raised source-drain regrowth. The low thermal budget of the top layer process caused no performance degradation of the lower level FETs. Record I_{ON} of 200 µA/µm (at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V) for 3DS integrated III-V FETs on silicon is demonstrated, with a 50% reduction of R_{ON} compared to previous work. The achieved improved performance can be attributed to the introduction of doped extensions underneath the gate region as well as improvements in the direct wafer bonding technique.**

Keywords—3DS, III-V, FinFETs, sequential integration, wafer bonding, monolithic integration

I. Introduction

3D sequential (3DS) integration – the sequential fabrication of multiple transistor levels – is considered a key technology in the CMOS roadmap [1]. Compared to 3D packaging using through-silicon vias, where levels are fabricated in parallel, then bonded together with low-resolution alignment, 3DS integration allows for alignment of subsequent levels as well as inter-level interconnects limited only by the resolution of the stepper. Key challenges of this technology include thermal budget management [2] and integration of channel layers with low defect density.

3DS integration facilitates not only traditional scaling motivators [3]–[5], such as power density and delay reduction through shorter interconnects, but also "More than Moore" approaches, such as monolithic integration of functionally different layers, e.g. for photonics, RF and sensing. III-V materials [6] are attractive in such systems, both as CMOS and RF performance boosters through high electron mobility, as well as enablers of new functionalities e.g. as direct band gap materials. Hybrid solutions, combining Si CMOS and III-V channels [7], [8], furthermore, can leverage the low thermal budget process of III-V FETs [9], typically sub-600 °C, to avoid degradation of reliability and performance of the bottom level Si CMOS.

In this work we demonstrate InGaAs FinFETs using a Si CMOS-compatible low-thermal budget process flow 3D sequentially integrated on Si CMOS. Through improved III-V wafer bonding and doped spacer extensions, devices with record I_{ON} for a 3DS III-V FET are demonstrated.

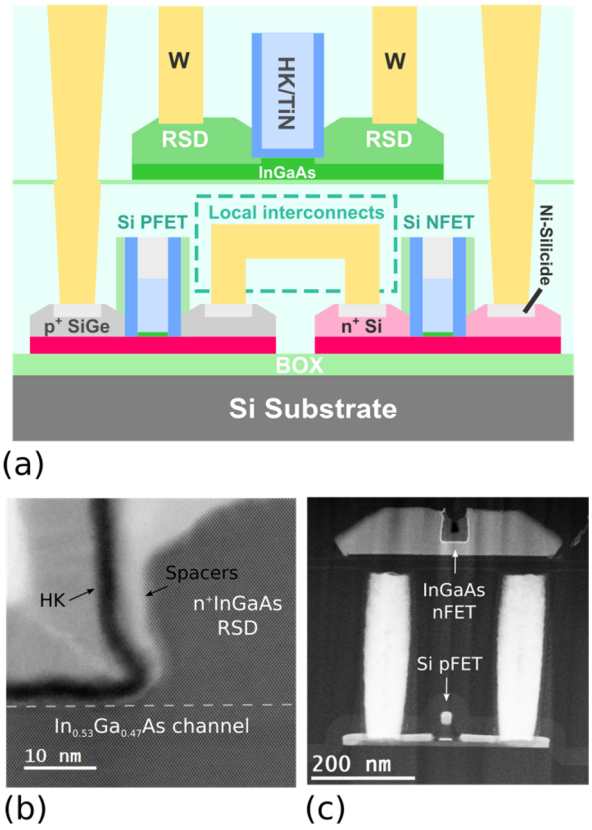

Figure 1 a) Schematic of the 3DS integrated stack, InGaAs nFETs on top of fully-depleted silicon-on-insulator Si pFETs and nFETs. A gate-first process is used for the Si CMOS and a RMG process for the InGaAs nFETs. b) Detailed TEM image of the InGaAs FET gate region. High crystalline quality for the InGaAs channel is shown. The Al_2O_3/HfO_2 gate oxide and the approximately 4 nm thick SiN_x spacers are highlighted. c) TEM cross-section of the 3DS integrated stack both transistor levels. Cross-section along the gate showing an InGaAs nFET with L_G = 60 nm on top of a Si pFET. W inter-layer contacts are also shown.

II. Device Fabrication

The 3DS integrated stack is composed of InGaAs FETs and FinFETs fabricated on top of a fully-depleted silicon-on-insulator (FDSOI) Si CMOS layer, as schematized in Fig. 1a. TiN/W contacts are used to connect the two tiers as well as for local interconnects. A standard gate-first FDSOI fabrication

flow is carried out for the bottom Si CMOS layer [10]. The active device layer is patterned on a silicon-on-insulator (SOI) substrate and optimized gate high-k (HK) dielectric, gate metal and poly-Si gate are deposited on the mesas. Subsequently, gate patterning is followed by spacer formation. N^+-Si raised source/drain (RSD) is carried out for the nFET and p^+-SiGe for the pFET. Extension implants, both for n/pFET, and annealing is then performed, followed by spacer deposition and patterning. Highly doped source/drain contacts are obtaining by doping implantation and salicidation with Ni/Pt silicide.

A first inter-layer dielectric (IL0) is deposited and planarized by chemical-mechanical polishing (CMP). After that, vias are etched to the RSD contacts, filled out with TiN/W and subsequently planarized to form the interlayer contacts for the 3DS stack. Afterwards, a second thin inter-layer dielectric (IL0') is deposited on the Si CMOS devices and CMP is performed to planarize the layer. This represents a crucial step in achieving low-defect density and high mobility in the 20 nm $In_{0.53}Ga_{0.47}As$ layer sequentially integrated on the Si CMOS wafer by direct wafer bonding [11]. The bonding was performed with a 2-inch donor InP wafer.

Compared to our previous 3DS integration work [12], we introduced three new modules in the III-V FET process flow, consisting in SiN_x spacers, doped extensions underneath the spacers and improvements in the wafer bonding technique.

A replacement metal gate (RMG) process is carried out on the top bonded layer for the nFET fabrication. Planar and fins structures are patterned by electron beam lithography and dry etching. The interlayer alignment accuracy is the same as in the Si CMOS layer. After active area patterning, the RMG process starts by deposition of a dummy metal gate. Then the gate pattern is defined by e-beam lithography and dry etching and subsequently SiN_x spacers are deposited and formed by RIE. Doped extensions are obtained by under-etching the III-V below the spacers followed by self-aligned *in-situ* doped contacts formation. N^+InGaAs RSD epitaxy is done by metal-organic chemical vapor deposition (MOCVD). After depositing an etch-stop layer and an encapsulation oxide layer (ILD1), planarization by CMP and dummy gate removal is carried out. An optimized HK and metal gate featuring a scaled bilayer Al_2O_3/HfO_2 (approximately 0.5 nm/3 nm thick) dielectric and TiN metal are deposited on the exposed InGaAs channel. Afterwards, a new encapsulating ILD2 layer is deposited and again planarized. Finally, contact vias are opened and filled with W.

Fig. 1b shows a TEM image of the high-quality InGaAs channel, highlighting spacers as well as the HK layer. A TEM cross-section of the fabricated InGaAs FET on top of Si pFET is shown in Fig. 1c.

III. Results

Output and subthreshold characteristic, after 3DS integration, are shown in Fig. 2, for bottom level Si n-FinFET and p-FinFET devices with L_G = 60 nm showing well-behaved transistor characteristics. We have previously demonstrated interlayer functionality in III-V/Si 3D SRAM cells [12]. Fig. 3

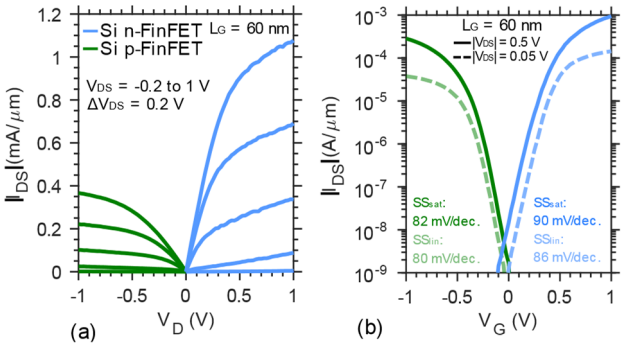

Figure 2 a) Output characteristic and b) subthreshold characteristic of Si n-FinFET (blue) and p-FinFET (green) with L_G = 60 nm after top-layer 3DS integration.

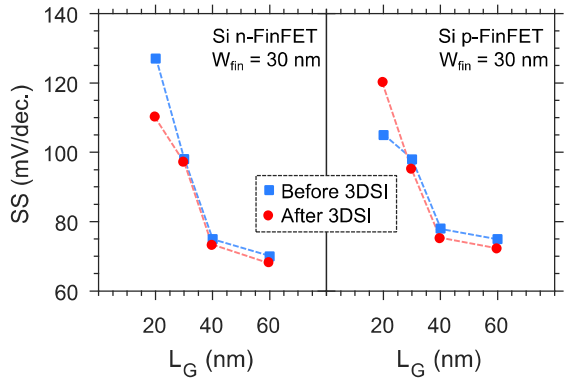

Figure 3 Subthreshold slope of Si CMOS n- and p-FinFETs in saturation, for devices with fin width of 30 nm before and after 3D sequential integration of the top III-V transistor level. Negligible change of SS is observed as a result of the 3DS integration.

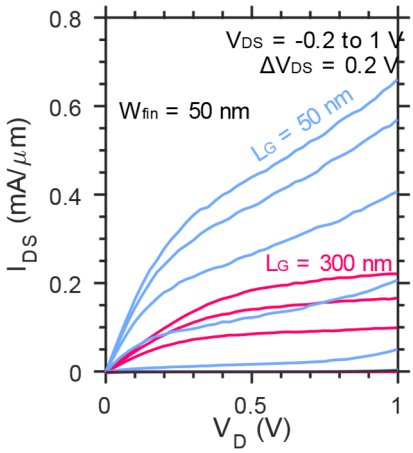

Figure 4 Output characteristic of InGaAs FinFETs for L_G = 50 nm and L_G = 300 nm, with W_{fin} = 50 nm showing well-behaved characteristics.

shows subthreshold slope in saturation for Si p- and n-FinFETs with fin width of W_{fin} = 30 nm before and after 3DS integration of the top III-V transistor layer. No significant impact on the bottom layer is observed post-integration. In Fig. 4 and 5, respectively, III-V FinFETs output and subthreshold characteristics for short (L_G = 50 nm) and long

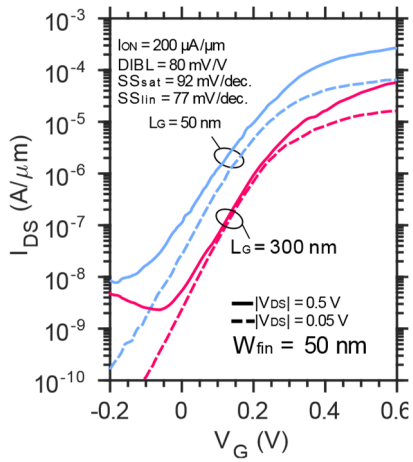

Figure 5 Transfer characteristic of InGaAs FinFET for L_G = 50 nm and L_G = 300 nm, with W_{fin} = 50 nm. Devices with at L_G = 50 nm show I_{ON} of 200 µA/µm (at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V), a record value for 3DS integrated InGaAs FET, enabled by SS in saturation of 92 mV/decade and transconductance of 1.1 mS/µm.

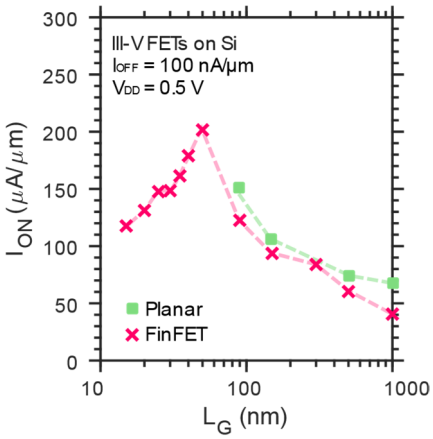

Figure 6 I_{ON} versus L_G for III-V Planar and FinFET structures. I_{ON} peaks at L_G = 50 nm. Below L_G = 50 nm, short-channel effects degrade performance for FinFETs while planar scalability is limited to L_G = 100 nm by the off current.

(L_G = 300 nm) gate lengths are reported for fin width of 50 nm. An excellent I_{ON} of 200 µA/µm is achieved for the short channel device at I_{OFF} = 100 nA/ µm and V_{DD} = 0.5 V. For the same device drain-induced barrier lowering (DIBL) of 80 mV/V and SS_{LIN} = 77 mV/dec is reported. The transconductance is g_m = 1.1 mS/µm for this device. Fig. 6 shows I_{ON} versus L_G for III-V FinFETs and planar FETs. For FinFETs, I_{ON} peaks at L_G = 50 nm, after which short-channel effects (SCE) impact SS. For planar devices, the I_{OFF} increases more strongly, limiting scalability, and at L_G = 100 nm, the I_{OFF} = 100 nA/µm target is no longer met.

Fig. 8 shows the on-resistance R_{ON} versus L_G. Compared to previously reported 3DS integrated III-V on Si CMOS [13], we achieve a reduction of R_{ON} by approximatively 50%. The reduction of R_{ON} can be explained by a lower defect density at the bonded InGaAs layer interface, yielding a higher electron mobility, obtained via improvements to the wafer bonding technique. The saturation of R_{ON} at short L_G may be caused by

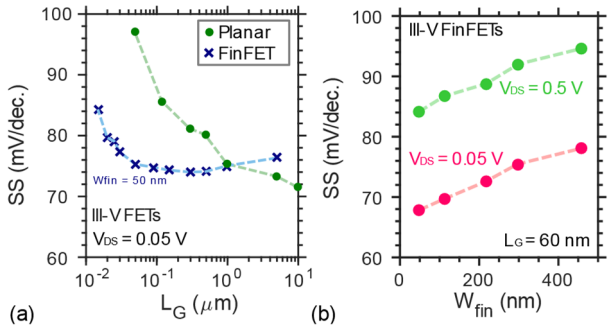

Figure 7 a) SS_{LIN} versus L_G for planar (green) and FinFETs (blue) structures. b) SS in linear and saturation region versus fin width.

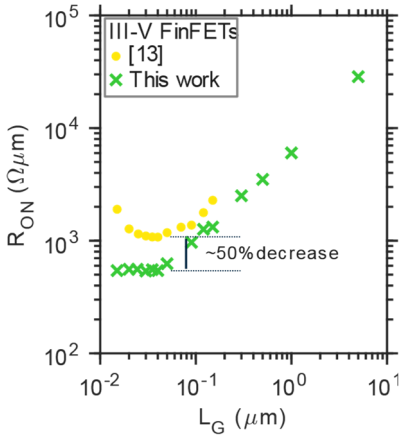

Figure 8 R_{ON} versus L_G for III-V FinFETs structures from this work compared to other 3DS integrated on Si CMOS work. A two-fold reduction for R_{ON} is demonstrated, as result of the improvements introduced in the III-V nFET processing. An access resistance of approximatively 100 Ωµm is extracted through linear extrapolation at L_G = 0 nm.

e.g. SCE reducing g_m due to high output conductance. Another explanation is an inhomogeneous distribution of defects in the channel, particularly a higher density near the n^+ contact regions, causing a reduction of the effective mobility in scaled devices. From long-channel devices, an access resistance of 100 Ωµm is obtained by linear extrapolation.

Subthreshold slopes versus gate length and fin width are

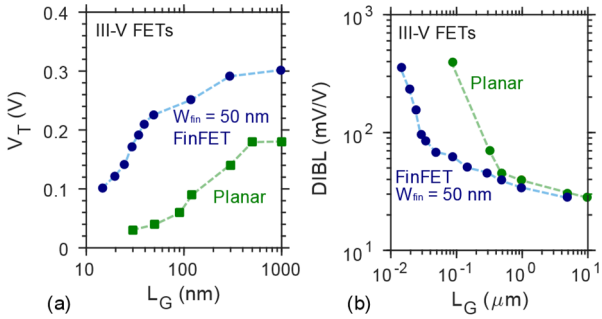

Figure 9 a) V_T versus L_G for planar (green) and FinFET (blue) devices with W_{fin} = 50 nm showing V_T roll-of onset at L_G = 50 nm. b) Drain-induce barrier lowering versus L_G for planar and FinFETs.

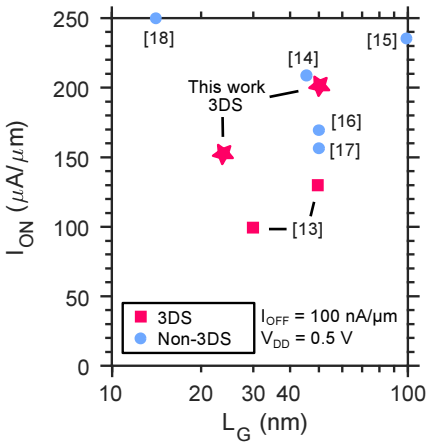

Figure 10 Benchmarking of I_{ON} versus L_G for 3DS integrated III-V FETs on Si (red symbols) as well as non-3DS III-V on silicon (blue dots)

shown in Fig. 7a and 7b, respectively. As also observed for I_{ON}, scaling L_G beyond 50 nm in FinFETs with W_{fin} = 50 nm causes SCE, increasing SS due to a lack of electrostatic control. Further scaling of W_{fin} will enhance off-state performance and scalability. For very long gate lengths (L_G > 5 µm) planar devices outperform FinFETs due to process-induced long-scale fin roughness.

Finally, threshold voltage and DIBL behavior with L_G scaling is shown (Fig. 9a,b). V_T roll-off onset is observed at L_G = 50 nm for FinFETs and 500 nm for planar FETs. Similarly, a strong increase of DIBL is observed at 30 nm for FinFETs and 500 nm for planar FETs. Both cases indicate a strong increase of electrostatic control in FinFET devices.

Fig. 10 shows a benchmark of I_{ON} (I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V) for state-of-the-art III-V-on-Si FETs, both with and without 3DS integration on Si CMOS [13]–[18]. Peak I_{ON} at L_G = 50 nm represents the highest value reported for III-V FETs 3DS integrated on Si CMOS and approaching the record value for all III-V-on-Si devices, showing that III-V FETs can be 3DS integrated with minimal loss of performance.

IV. Conclusions

In this work we have demonstrated InGaAs FinFETs 3DS integrated on FDSOI Si CMOS. The low thermal budget of the III-V top layer process flow enabled maintained Si CMOS performance post-3DS integration. By improvements to the wafer bonding technique and with the introduction of doped extensions, we achieved a record I_{ON} of 200 µA/µm for 3DS integrated III-V FETs on Si and approaching the record for all III-V-on-silicon FETs. These results show that 3DS integration of III-V FETs on Si CMOS can be performed with minimal performance degradation in both transistor levels.

Acknowledgment

The authors want to acknowledge CEA-Leti Institute for providing the silicon CMOS wafers (H. Boutry, J. Widiez, L. Brévard, C. Le Royer and M. Vinet) and the BRNC staff for technical. This work was funded by Horizon 2020 grant agreement no. 688784 (INSIGHT) and grant agreement no. 687931 (REMINDER).

Reference

[1] A. Mallik *et al.*, "The impact of Sequential-3D integration on semiconductor scaling roadmap," *Int. Electron Devices Meet. IEDM*, p. 32.1.1-32.1.4, 2017.

[2] G. R. K. Triantopoulos, M. Casse, L. Brunet, P. Batude, C. Fenouillet-Beranger, B. Mathieu, M. Vinet, G. Ghibaudo, "Thermal effects in 3D sequential technology," *Int. Electron Devices Meet. IEDM*, p. 7.6.1, 2017.

[3] P. Batude *et al.*, "3D Sequential Integration: Application-driven technological achievements and guidelines," *Int. Electron Devices Meet. IEDM*, p. 3.1.1-3.1.4, 2017.

[4] M. Vinet *et al.*, "Monolithic 3D integration: A powerful alternative to classical 2D scaling," *2014 SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. S3S 2014*, pp. 17–19, 2014.

[5] P. Batude *et al.*, "3DVLSI with CoolCube process: An alternative path to scaling," *Symp. VLSI Technol.*, vol. 2015–Augus, pp. T48–T49, 2015.

[6] H. Riel, L. E. Wernersson, M. Hong, and J. A. Del Alamo, "III-V compound semiconductor transistors - From planar to nanowire structures," *MRS Bull.*, vol. 39, no. 8, pp. 668–677, 2014.

[7] C. B. Zota, F. Lindelow, L. Wernersson, and E. Lind, "InGaAs Tri-gate MOSFETs with Record On-Current," *Int. Electron Devices Meet. IEDM*, p. 3.2.1-3.2.4, 2016.

[8] X. Sun *et al.*, "High Performance and Low Leakage Current InGaAs-on-Silicon FinFETs with 20 nm Gate Length," *Symp. VLSI Technol.*, pp. 40–41, 2017.

[9] J. Micout *et al.*, "High performance low temperature FinFET with DSPER , gate last and Self Aligned Contact for 3D sequential integration," *Int. Electron Devices Meet. IEDM*, p. 32.2.1-32.2.4, 2017.

[10] S. Barraud *et al.*, "Scaling of Ω-Gate SOI Nanowire N- and P-FET down to 10nm Gate Length: Size- and Orientation-Dependent Strain Effects," *Symp. VLSI Circuits*, pp. 230–231, 2013.

[11] L. Czornomaz *et al.*, "An integration path for gate-first UTB III-V-on-insulator MOSFETs with silicon, using direct wafer bonding and donor wafer recycling," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 517–520, 2012.

[12] V. Deshpande *et al.*, "Demonstration of 3-D SRAM Cell by 3-D Monolithic Integration of InGaAs n-FinFETs on FDSOI CMOS with Interlayer Contacts," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4503–4509, 2017.

[13] V. Deshpande *et al.*, "First Demonstration of 3D SRAM Through 3D Monolithic Integration of InGaAs n-FinFETs on FDSOI Si CMOS with Inter-layer Contacts," *Symp. VLSI Technol.*, 2017.

[14] X. Zhou *et al.*, "Scalability of InGaAs gate-All-Around FET integrated on 300mm Si platform: Demonstration of channel width down to 7nm and Lgdown to 36nm," *Symp. VLSI Technol.*, 2016.

[15] M. L. Huang *et al.*, "In0.53Ga0.47As MOSFETs with high channel mobility and gate stack quality fabricated on 300 mm Si substrate," *Symp. VLSI Technol.*, 2015.

[16] N. Waldron *et al.*, "Gate-all-around InGaAs nanowire FETS with peak transconductance of 2200µS/µm at 50nm Lg using a replacement Fin RMG flow," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, p. 31.1.1-31.1.4, 2015.

[17] V. Djara, V. Deshpande, M. Sousa, D. Caimi, L. Czornomaz, and J. Fompeyrine, "CMOS-compatible Replacement Metal Gate InGaAs-OI FinFET With ION = 156 µA/µm at VDD = 0.5 V and IOFF = 100 nA/µm," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 169–172, 2016.

[18] H. Hahn *et al.*, "A scaled replacement metal gate InGaAs-on-Insulator n-FinFET on Si with record performance," *Int. Electron Devices Meet. IEDM*, p. 17.5.1-17.5.4, 2017.