RZ 3954 (#ZUR1610-034) 10/13/2016
Electrical Engineering 17 pages

Research Report

3D Monolithic Integration of III-V and Si(Ge) FETs for hybrid CMOS and Beyond

V. Deshpande[1], V. Djara[1], E. O'Connor[1], P. Hashemi[2], T. Morf[1], K. Balakrishnan[2], D.Caimi[1], M. Sousa[1], J. Fompeyrine[1] and L. Czornomaz[1]

[1] IBM Zurich Research Laboratory, Saumerstrasse 4, CH-8803 Rueschlikon, Switzerland

[2] IBM T.J.Watson Research Center, 1101 Kitchawan Rd., Route 134 Yorktown Heights, NY, USA

© 2017 The Japan Society of Applied Physics.
This is a peer-reviewed, un-copyedited version of an article published by IOP: V. Deshpande, V. Djara, E. O'Connor, P. Hashemi, T. Morf, K. Balakrishnan, D.Caimi, M. Sousa, J. Fompeyrine and L. Czornomaz, "3D Monolithic Integration of III-V and Si(Ge) FETs for hybrid CMOS and Beyond," Japanese Journal of Applied Physics 56, 04CA05 (2017).
IOP Publishing Ltd is not responsible for any errors or omissions in this version of the manuscript or any version derived from it. The Version of Record is available online at 10.7567/JJAP.56.04CA05.

LIMITED DISTRIBUTION NOTICE

This report has been submitted for publication outside of IBM and will probably be copyrighted if accepted for publication. It has been issued as a Research Report for early dissemination of its contents. In view of the transfer of copyright to the outside publisher, its distribution outside of IBM prior to publication should be limited to peer communications and specific requests. After outside publication, requests should be filled only by reprints or legally obtained copies (e.g., payment of royalties). Some reports are available at http://domino.watson.ibm.com/library/Cyberdig.nsf/home.

IBM Research
Africa • Almaden • Austin • Australia • Brazil • China • Haifa • India • Ireland • Tokyo • Watson • Zurich

3D Monolithic Integration of III-V and Si(Ge) FETs for hybrid CMOS and Beyond

V. Deshpande[1 *], V. Djara[1], E. O'Connor[1], P. Hashemi[2], T. Morf[1], K. Balakrishnan[2], D. Caimi[1], M. Sousa[1], J. Fompeyrine[1] and L. Czornomaz[1]

[1] *IBM Zurich Research Laboratory, Saumerstrasse 4, CH-8803 Rueschlikon, Switzerland*
[2] *IBM T.J.Watson Research Center, 1101 Kitchawan Rd., Route 134 Yorktown Heights, NY, USA*

3D Monolithic integration can enable higher density and has the potential to stack independently optimized layers at transistor level. Owing to high mobility and lower processing temperatures, InGaAs is well-suited to be used as the top layer channel material in 3D monolithic integation along with Si/Si(Ge) FETs. A review of recent progress to develop InGaAs-on-Si(Ge) 3D Monolithic technology is presented here.

1. Introduction

The conventional CMOS technology or 2D CMOS technology is facing significant challenges for downscaling the area of circuits in advanced nodes owing to high densities required. Exploiting the third dimension through vertical stacking of device layers presents an interesting opportunity to achieve higher device density without scaling down the dimensions. In this context monolithic 3D (3DM) integration has the potential to achieve very high interconnect densities,[1)2)] due to very high granularity provided by transistor level stacking. Besides conventional digital circuits,[3)] it offers the opportunity to stack independently optimized multi-functional layers at transistor level for *More-than-Moore* technologies.[4)] Recently, there has been significant effort in developing scalable monolithic 3D integration with group IV semiconductor channels involving Si or Ge FET layer on top of Si/SiGe FET layer.[5)] However, due to the inherently high thermal budget of Si MOSFET process, monolithic 3D integration of Si(Ge)-on-Si faces a major challenge in terms of degradation of bottom layer FET performance due to the top layer FET thermal budget. This mandates the development of low temperature process for top layer Si or Si(Ge) FETs while maintaining the device performance. Recent efforts in this direction[3)6)] demonstrate the significance of this technological challenge.

*E-mail:vee@zurich.ibm.com

In this purview, III-V channel FETs (specifically InGaAs based) present an exciting opportunity. As InGaAs based FET process is inherently a lower thermal budget process (typically <650 °C), it brings a native advantage for utilization as top layer FET. Moreover, InGaAs material system is well-known to higher electron mobility compared to Silicon[7] and is being considered as potential n-channel material for scaled CMOS nodes to replace Silicon. Considerable progress has also been made recently in InGaAs based MOSFETs demonstrating high performance at low supply voltages, both on InP substrate,[8][9] and on silicon platform[10][11].[12] Besides the recent consideration as n-channel material for CMOS technology, InGaAs based material system has traditionally been utilized as channel in high-electron mobility transistors (HEMTs) for high-frequency applications. Benefiting from the developments made in InGaAs based FETs, impressive cut-off frequencies have been demonstrated in MOS-HEMT and MOSFET architectures,[13][14] Thus, a III-V channel material such as InGaAs, has potential to enable both high-performance digital logic as well as high-frequency circuits tightly cointegrated, down to transistor level, in 3D monolithic integration. Therefore one can envisage a truly multi-functional 3D monolithic integration scheme where InGaAs nFETs on top of Si/SiGe FETs can allow higher performance hybrid CMOS[15] and high frequency InGaAs RF-FETs can benefit from closely integrated CMOS circuits.[16]

The recent developments towards such a multi-functional hybrid 3D monolithic integration involving III-V (mainly InGaAs bsed materials)and group IV materials (mainly Si/SiGe) are reviewed here. First of all, efforts involving III-V material integration on Silicon substrate, specifically those that can enable a scalable 3D monolithic platform are also reviewed. Then the-state-of-the-art of device integration in such a hybrid 3D monolithic integration is reviewed. Then various works demonstrating both DC and RF performance in a III-V and Si 3D monolithic integration scheme are detailed. Finally, conclusions and future perspectives are discussed.

2. III-V material Integration Through Direct Wafer Bonding

One of the very important modules in 3D monolithic integration of III-V materials with Si/Si(Ge) is the process of forming III-V channel layer on top of Si/Si(Ge) device layer. For a robust and scalable 3D monolithic integration scheme, it would be advantageous to have continuous high-quality film of the channel material. As in the case of Si(Ge)-on-Si 3D monolithic integration, direct wafer bonding (DWB) (of III-V materials in this case) through oxide-oxide molecular bond provides a scalable and manufacturable approach.

In order to obtain low defectivity channel material, it is essential to grow it on a lattice

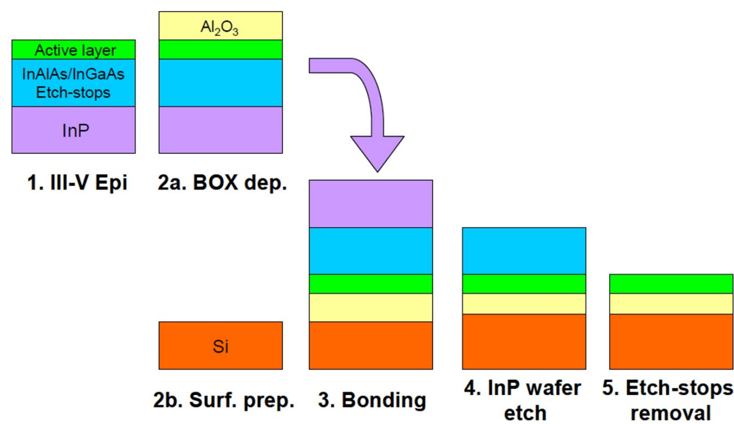

Fig. 1. Schematic showing process steps for direct wafer bonding of III-V layers on Si substrate starting from InP donor wafer.

matched donor substrate. InP is lattice matched InGaAs with 53% In content. Therefore, InP substrates are ideal to be used as donor substrates to transfer InGaAs layer on to Si/Si(Ge) device layer. It is essential choose a bonding oxide that can enable relatively low temperature bonding with high bonding strength. Early work from various groups[17)18)] has shown Al_2O_3 to be excellent material for this purpose. Figure 1. shows the schematic of bonding process with InP donor wafer.

The process starts with growing etch stop layers and final InGaAs channel layer on an InP wafer. Typically this is done on 2 inch InP wafers due to their relative ease of availability and reasonable cost (wafers of higher diameter can be extremely expensive). After growing the channel layer with all the etch stops, a bonding oxide is deposited on top. Next a silicon receiver wafer is deposited with bonding oxide. Thereafter the two wafers are bonded together by bringing oxide surfaces to contact and forming oxide-oxide molecular bond. Afterwards, the InP wafer can either be etched away or cleaved out and recycled if pre-implanted with hydrogen ions as described in reference[18)] . In the case of 3D monolithic integration of III-V and Si/Si(Ge) layers, the receiver wafer has Si/Si(Ge) FET layer processed and a interlayer dielectric deposited, planarized and bonding oxide deposited on top (if different from interlayer dielectric).

As mentioned before, due to lack of availability of large diameter InP wafers, the method of transferring top layer from InP donor wafer gets limited to 2 inch diameters. This makes it non-viable for manufacturing. Therefore, it is essential to have method that provides scalability to large area substrates. Recently significant progress has been made in this direc-

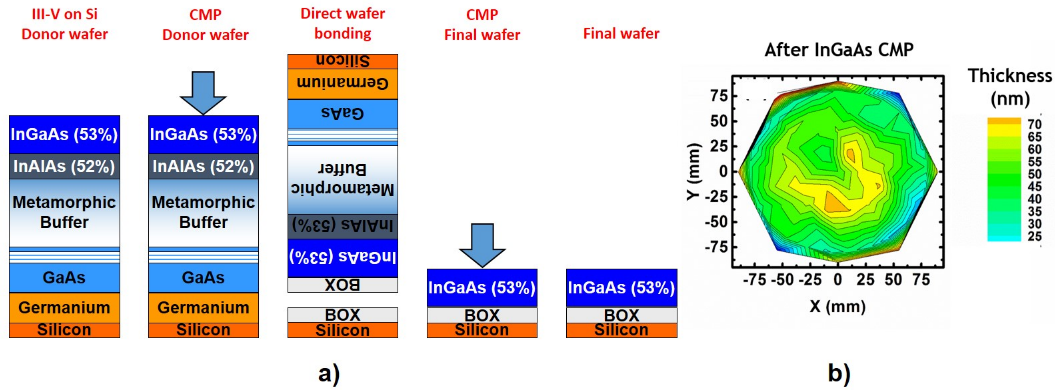

Fig. 2. a) Schematic showing process steps for direct wafer bonding of III-V layers on Si substrate starting from Si donor wafer. b) Spectroscopic ellipsometry map of the 200 mm InGaAs-OI wafer showing InGaAs layer thicknes of 50 nm. Adapted from[20] .

tion[19)20)21] and InGaAs-on-insulator wafer up to 300 mm diameter have been demonstrated[21] . The method consists of first growing strain relaxing metamorphic buffer layers on large area silicon substrates and finally growing the channel material. This process allows to obtain low-defectivity top channel material. The fabrication process of the InGaAs-OI substrate starting from Silicon donor substrate as described in reference[20] is shown in figure 2.

The donor is InGaAs (53% In content) grown by MBE on 200 mm Si (100) substrate. Starting from Si substrate, first a 2.5 m Ge buffer was directly grown on Si followed by 0.5 m Ga(Al)As and 1.5-2 μm $In_xAl_{1-x}As$ metamorphic buffer (MB) and finally 500 nm InGaAs channel (53% In content) material. The wafer was planarized using CMP and a post CMP roughness below 0.4 nm was obtained. After CMP, Al_2O_3 bonding oxide (BOX) layer was deposited. The donor wafer was subsequently removed by wet-etching and a 200 mm InGaAs-OI substrate was obtained. At this step InGaAs thickness of about 250 nm was obtained. A second CMP step on the InGaAs-OI wafer was used to reduce the active layer thickness to about 50 nm. The reported spectroscopic ellipsometry map of the 200 mm wafer after second CMP step is shown in figure 2.

A similar process but improved to allow donor wafer recycling through SmartCut™was developed in reference[22] . InGaAs-on-insulator wafers of 300 mm diameter were demonstrated in this work. The process flow described in the reference[22] is shown in figure 3. Here, the buffer layer consist of GaAs and InP. Prior to oxide-oxide bonding with receiver wafer, H^+ implantation is carried out to create defects in InP layer that enable splitting of wafer after bonding. Post-splitting, the donor wafer can be recycled to perform bonding again. 300 mm InGaAs-on-insulator wafer so obtained is shown in figure 3.

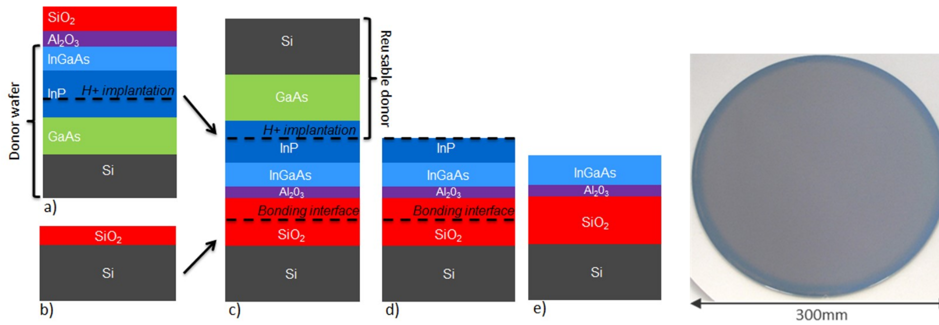

Fig. 3. Schematic showing process steps for direct wafer bonding of III-V layers on Si substrate with SmartCut™ process. Also shown is photograph of 300 mm InGaAs-on-insulator wafer obtained. Adapted from ref.[22]

Reference	[23]		[24]		[15]	
Device	Bottom pFET	Top nFET	Bottom pFET	Top nFET	Bottom pFET	Top nFET
Material	Ge-bulk	InGaAs-OI	SiGe-OI	InGaAs-OI	SiGe-OI	InGaAs-OI
Device Architecture	Planar GF	Planar GF	Fin (30 nm) GF	Fin (30 nm) GF	Fin (~8-20 nm) GF	Planar & Fin (35-80 nm) RMG
Source/Drain	NiGe	Ni-InGaAs	Ni-SiGe	Ni-InGaAs	SiGe-RSD/NiPt	InGaAs-RSD
CET	1.5 nm	4.2 nm	1.5 nm	4.2 nm	1.4-1.5 nm	1.6 nm
Min Gate Length	200 µm	200 µm	300 nm	300 nm	Sub-20 nm	~30 nm

Fig. 4. Table showing various reports on InGaAs-on-Si(Ge) 3D monolithic integration. Adapted from ref.[15]

These methods can be utilized to develop 3D monolithic integration of InGaAs on large area Si/Si(Ge) FET processed wafers. In that case, the Si/Si(Ge) FET layer with interlayer dielectric deposited and planarized will become the receiver wafer.

3. InGaAs-on-Si(Ge) 3D Monolithic Integration

All the works demonstrating InGaAs-on-Si(Ge) 3D monolithic integration have been summarized in a table in Figure 4.

The first demonstration of InGaAs-on-Ge 3D monolithic integration was carried out by Irisawa et al as reported in.[23] The work demonstrated, for the first time, 3D monolithic integration of InGaAs nFETs on Ge pFETs. Ge pFETs were fabricated on bulk Ge substrate with a gate-first flow. Ge pFET source/drain regions were formed by NiGe alloy formation. No implantation or epitaxially grown doped source/drain was used. InGaAs layer (53% In content) was transferred on top of the pFET layer through DWB from 2 inch InP wafer similar to process described in previous section. InGaAs nFETs were also fabricated with gate-first flow and low temperature (<350°C) Ni-InGaAs alloy formed the source/drain. No impact on Ge

pFET performance was observed after nFET fabrication. 3D inverters with top InGaAs nFET and bottom Ge pFET were reported with VTC measured down to Vdd = 0.2 V. Both pFET and nFET had limited drive currents. Although relatively simpler integration scheme was used for pFET and nFETs, it was the first demonstration of 3D monolithic circuits involving InGaAs and Ge devices.

Another important 3D monolithic integration of InGaAs-on-SiGe was demonstrated by the same group (Irisawa et. al[24]). The 3D monolithic integration reported was relatively more complex featuring independent back-gates for both top InGaAs nFETs and bottom SiGe-OI pFETs. The integration scheme involved fabrication of bottom SiGe-OI p-finFETs through Ge condensation, followed by gate-first flow with Ni-SiGe source/drain. No implantation or RSD was used to form source/drain regions. After bottom SiGe-OI pFET fabrication, back gate for top layer was formed through TaN deposition. Oxide was then deposited on top and InGaAs layer was transferred through DWB. InGaAs nFETs featured fins down to 30 nm. Source/drain regions were formed through Ni-InGaAs alloy. 3D CMOS inverters with symmetric characteristics (down to Vdd =0.2 V) and 21 stage ring-oscillators were reported with individual back gate tunability. Thus the work demonstrated relatively large circuits with complex 3D monolithic integration. Although, individual FET performances were limited by access resistance, the work demonstrated potential of InGaAs-on-SiGe 3D monolithic integration and advantages of independent back-gate.

Recently, advanced 3D monolithic integration of InGaAs-on-SiGe was demonstrated by Deshpande et. al.[15] The work featured InGaAs planar and wide-fin nFETs on top of SiGe-on-insulator (SiGe-OI) pFETs. Both layers featured state-of-the-art device integration with top InGaAs nFETs processed with Replacement-Metal-Gate (RMG) flow and bottom SiGe-OI pFETs were processed with Gate-First (GF) process. The bottom pFETs featured self-aligned raised source/drain (RSD) and salicide process and the top InGaAs nFETs also featured self-aligned RSD. Since salicide on the bottom pFET sets the thermal budget limitation for the top nFET process, having an epitaxially grown RSD process for top nFETs (highest thermal budget of all process steps for top nFET) demonstrated the complete hybrid CMOS process without compromises on either layers. An optimized RSD process for top nFET layer enabled negligible impact on the performance of bottom pFET layer. Figure 5 shows the process flow for the 3D monolithic integration scheme as described in reference.[15]

Firstly, bottom layer SiGe-OI fin pFETs were fabricated with GF process similar to the one described in[25].[26] The process involved thinning of silicon layer of an 8 inch SOI wafer followed by Ge condensation to obtain SiGe-OI layer (with 25% Ge content). Then active

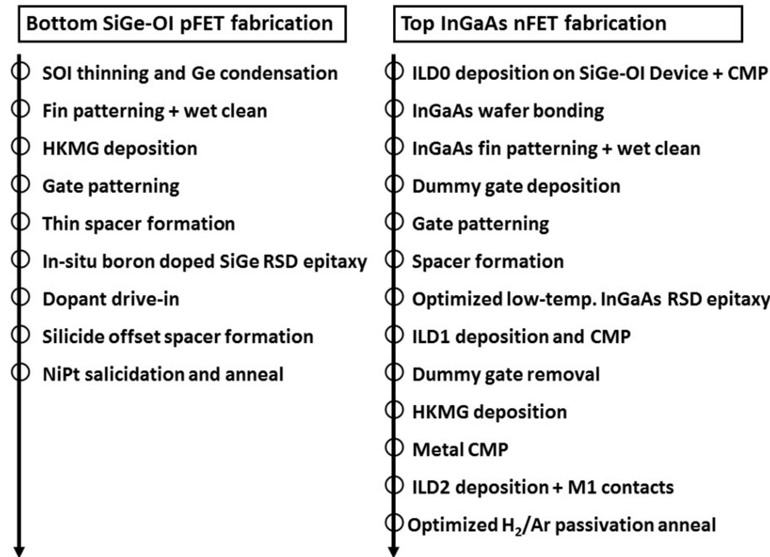

Fig. 5. Process flow for 3D monolithic integration of InGaAs-on-SiGe. Adapted from ref.[15]

pFET areas were formed and gate-stack featuring high-k dielectric and metal gate was deposited. After gate pattering and spacer formation, in-situ doped SiGe epitaxy was carried out to form self-aligned raised source drain (RSD) regions. Then NiPt salicidation (self-aligned silicidation) was performed for low contact resistivity on the pFETs. The thermal budget limit for the top nFET processing is set by the stability of this silicide. The top layer nFET fabrication was carried out after the silicidation step of SiGe-OI finFET process. Firstly, an interlayer oxide was deposited and chemical-mechanical-polish (CMP) planarization was carried out. The InGaAs layer was transferred on to this oxide with direct wafer bonding from 2 inch InP donor wafers with the process described in previous section. InGaAs nFET fabrication was then performed with a RMG process described in reference.[20] This involved patterning the active transistor regions followed by a dummy gate stack deposition. Then the dummy gate was patterned and spacers were formed. Thereafter an optimized self-aligned RSD process was carried out. As this step has the highest thermal budget of all the processes involved in top nFET fabrication, it determines the impact on the performance of the bottom pFET. However, this is also a crucial step to obtain high-performance InGaAs nFET as it provides low contact resistivity. Gate replacement process steps were carried out thereafter. An oxide layer was deposited and planarized to expose the top of dummy gate. Then the dummy gate stack was selectively etched out. An optimized high-k/metal gate stack[27] was deposited and metal CMP was carried out. Finally, oxide encapsulation was performed and contact holes were opened to both top and bottom layers. Metallization was completed to create contact

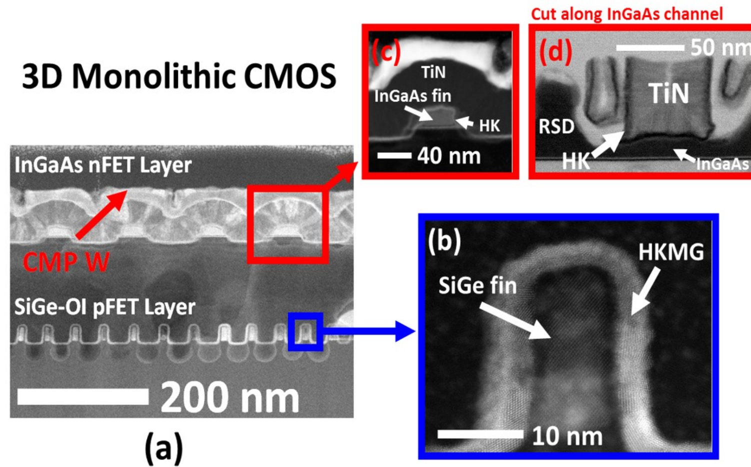

Fig. 6. Cross-section TEM images of InGaAs-on-SiGe 3D monolithic stack. (a) InGaAs nFET layer on SiGe-OI pFET layer along gate, (b) zoom-in on an 8 nm wide SiGe pFET fin (c) a 35 nm wide InGaAs nFET fin, and (d) cross section along nFET InGaAs channel showing RMG. Adapted from ref.[15)]

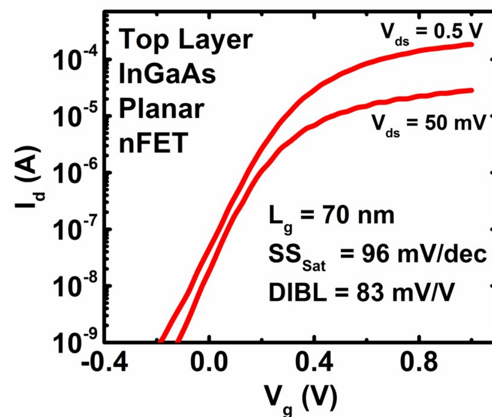

Fig. 7. Top layer InGaAs nFET $I_d - V_g$ characteristics. Adapted from ref[15)]

pads for both layers.

Cross section TEM images of the so completed 3D monolithic integration is shown in figure 6.

The reported DC transfer characteristics of the top layer InGaAs nFET featuring a gate length of 70 nm and a bottom layer SiGe-OI pFET featuring a gate length of 25 nm are shown in figures 7 and 8 respectively. SiGe-OI pFET shows excellent electrostatic integrity (SS_{sat} = 81 mV/dec, DIBL = 48 mV/V) at L_g = 25 nm owing to the optimized process(pouya13, pouya14). InGaAs nFET reported is a planar FET and demonstrates competitive electrostatic integrity (SS_{sat} =96 mV/dec, DIBL = 83 mV/V) at L_g = 70 nm.

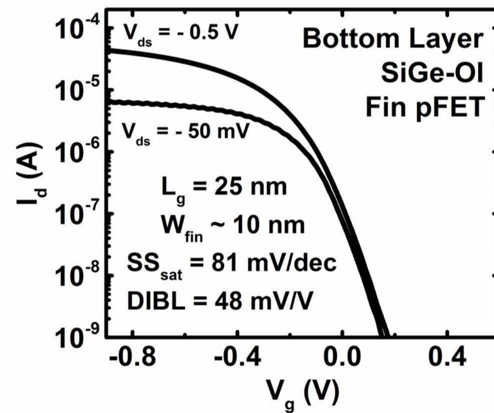

Fig. 8. Bottom layer SiGe-OI pFET $I_d - V_g$ characteristics Adapted from ref.[15)]

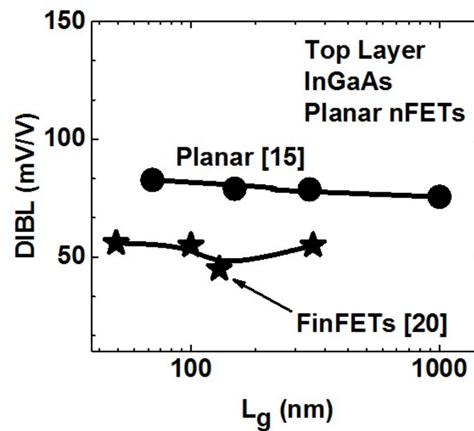

Fig. 9. DIBL vs.L_g characteristics for top layer InGaAs nFETs. Adapted from ref.[15)]

The DIBL and SS_{sat} roll-off characteristics of the nFET were also reported and are shown in figures 9 and 10. Well-controlled nFET scaling behavior was demonstrated and the performance was close to previously reported InGaAs-OI RMG FinFETs by the same group.[27)] Thus, independent optimized process for both layers developed separately, were brought together in one 3D monolithic integration scheme without adverse performance impact.

The impact on pFET characteristics post top nFET fabrication is the ultimate test for the feasibility of 3D monolithic integration scheme. The reported comparison of bottom pFET $I_d - V_g$ before and after top nFET fabrication is shown in figure11. Almost comparable Idsat was obtained postnFET indicating very minimal impact on pFET silicide. DIBL and SS_{sat} roll-offs for pFETs were also compared pre and post nFET fabrication. Very minimal change was observed post nFET process as shown in figure12.

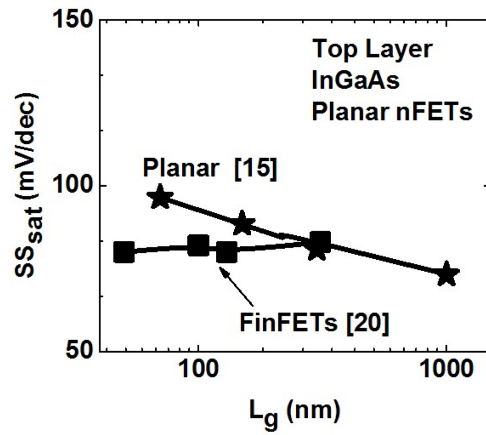

Fig. 10. SS_{sat} vs.L_g characteristics for top layer InGaAs nFETs. Adapted from ref.[15]

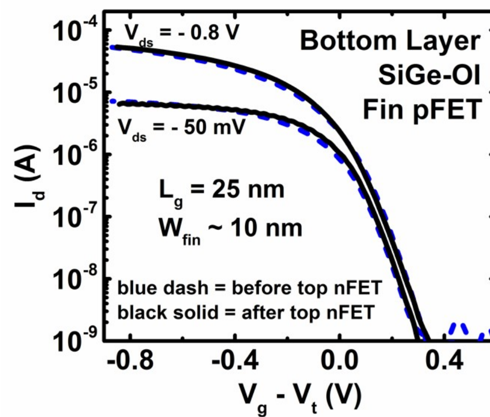

Fig. 11. Comparison of bottom layer SiGe-OI pFET $I_d - V_g$ characteristics before and after top layer nFET fabrication as reported in ref.[15]

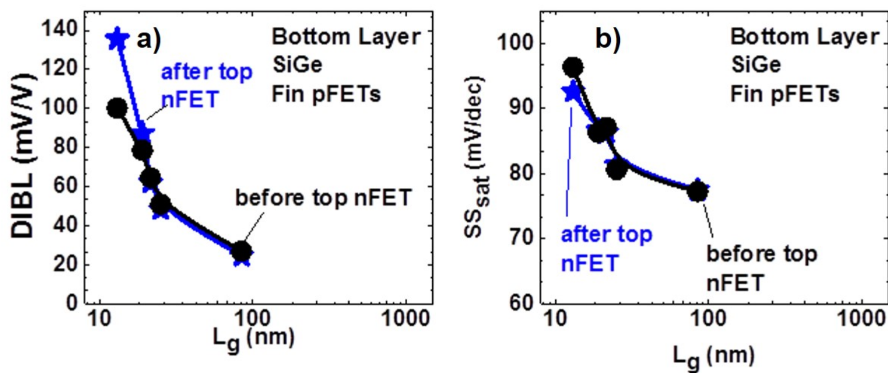

Fig. 12. Comparison of bottom layer SiGe-OI pFET DIBL and SS_{sat} vs. L_g characteristics before and after top layer nFET fabrication as reported in ref.[15]

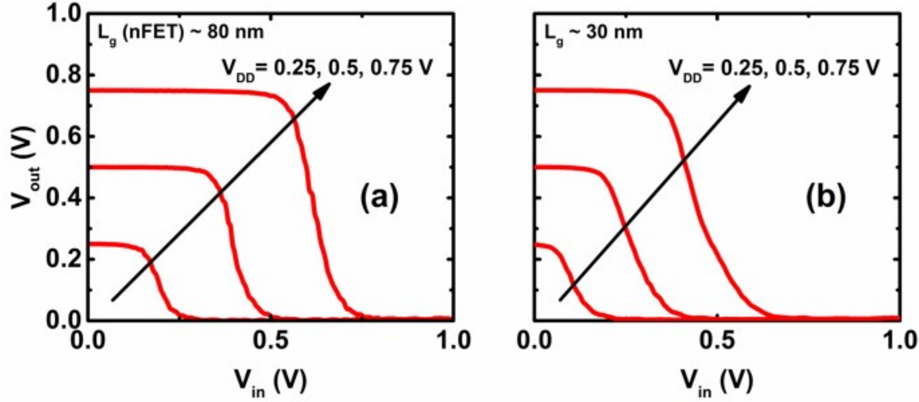

Fig. 13. Reported voltage transfer characteristics of 3D inverters. Adapted from ref.[15)]

Thus the feasibility of InGaAs-on-SiGe 3D monolithic integration was demonstrated. Voltage transfer characteristics (VTC) of scaled 3D inverters with nFET L_g = 80 nm and L_g 30 nm (for both nFET and pFET) were also reported shown in Fig 13(a) and (b) respectively. Well-behaved transitions were obtained down to Vdd = 0.25 V. The VTC were not symmetric owing to mis-match in pFET and nFET device performances.

3.1 Top layer InGaAs RFFETs

As mentioned earlier, III-V channel materials are well-suited for high-frequency devices. Integrating them in a 3D monolithic scheme on top of Si/Si(Ge) provides opportunity to realize mixed signal circuits. Recent simulation work has shown benefits of III-V high frequency devices co-integrated with Si CMOS.[16)] First efforts to characterize the RF performance of InGaAs FETs integrated on top of SiGe pFETs have recently been reported.[28)] The InGaAs RFFETs were fabricated along with the DC FETs detailed in the previous section. In order to enable RF characterization of top layer InGaAs nFETs, their layout consisted of multi-finger gates with a ground-signal-ground (GSG) pad configuration. A device reported in reference[28)] featured 10 parallel finger gates, each with a width of 2 μm (= total device width of 20 μm). DC $I_d - V_g$characteristics reported are shown in figure 14.

The current gain $|h21|$ (dB) vs. frequency reported is shown in Fig. 15, for a device with L_g = 120 nm. A cut-off frequency (F_t) of 16.4 GHz was obtained for V_{ds} = 1 V. Although this relative lower value than typical InGaAs HEMTs or MOS-HEMTs, it should be noted that the device structure was not optimized for RF performance and hence further optimization could enable higher cut-off frequencies. This is very encouraging result towards diversification of InGaAs-on-Si(Ge) 3D monolithic integration platform towards ‘More-than-Moore’ applications.

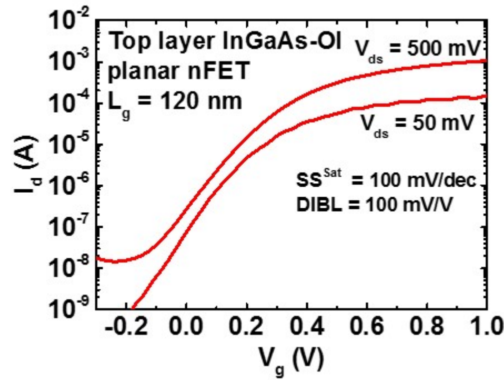

Fig. 14. Reported DC $I_d - V_g$ characteristics top layer InGaAs RFFET. Adapted from ref.[28)]

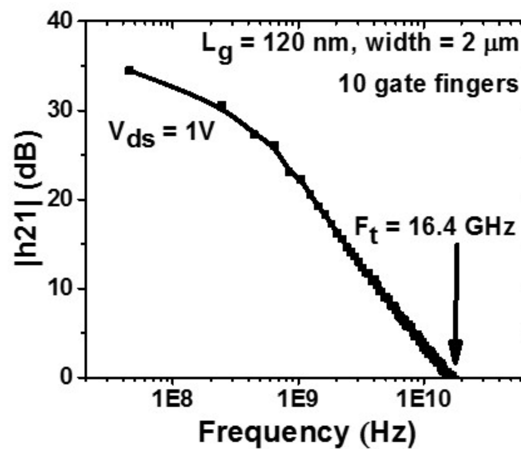

Fig. 15. Reported current gain ($|h21|$) and cut-off frequency of top layer InGaAs RFFET with L_g = 120 nm. Adapted from ref.[28)]

4. Conclusions

3D monolithic integration of III-V MOSFETs on top of Si/Si(Ge) provides opportunity achieving both high performance, dense CMOS as well as mixed-signal applications. It can become a truly multi-functional platform bringing best of III-V world and conventional Si/Si(Ge) CMOS world. Recently progress in this context were reviewed, starting from III-V material integration to 3D monolithic integration with state-of-the-art process flows and 3D circuits. Significant progress has been made in upscaling the III-V wafer bonding to 300 mm wafer sizes. This will become key enabler for a feasible InGaAs-on-Si(Ge) 3D monolithic technology. Progress made in advanced device integration in 3D monolithic scheme demonstrates that no major hurdles are present to realize a high-performance 3D hybrid CMOS. As a step further, improving performance of III-V devices (in 3D monolithic scheme) to the level

shown on InP substrates needs to be achieved. Also, demonstration of 3D monolithic integration of InGaAs-on-Si/Si(Ge) through layer transfer on 300 mm wafer size will be significant step forward towards a manufacturable platform. Thus, exciting prospects exist for realizing a hetero-integrated 3D monolithic platform with high-mobility III-V materials.

Acknowledgment

Funding from the EU is acknowledged (ICT-2013-11 COMPOSE3, ICT-2013-11 IIIVMOS, H2020-ICT-2015-688784-INSIGHT and PEOPLE-2013-IEF FACIT). Authors acknowledge the IBM MRL and BRNC staff as well as management support at both sites.

References

1) P. Batude, M. Vinet , A. Pouydebasque , C. Le Royer , B. Previtali , C. Tabone , L. Clavelier , S. Michaud , A. Valentian , O. Thomas , O. Rozeau , P. Coudrain , C. Leyris , K. Romanjek , X. Garros , L. Sanchez , L. Baud , A. Roman , V. Carron , H. Grampeix , E. Augendre , A. Toffoli , F. Allain , P. Grosgeorges , V. Mazzochi , L. Tosti , F. Andrieu , J. M. Hartmann , D. Lafond , S. Deleonibus , O. Faynot, *GeOI and SOI 3D monolithic cell integrations for high density applications* Symposium on VLSI Technology, pp. 166-167 (2009).
2) Billoint, Olivier and Sarhan, Hossam and Rayane, Iyad and Vinet, Maud and Batude, Perrine and Fenouillet-Beranger, Claire and Rozeau, Olivier and Cibrario, Gerald and Deprat, Fabien and Turkyilmaz, Ogun and Thuries, Sebastien and Clermidy, Fabien, *From 2D to Monolithic 3D: Design Possibilities, Expectations and Challenges*, Proceedings of the 2015 Symposium on International Symposium on Physical Design, pp. 127–127 (2015).
3) P. Batude et al., *3DVLSI with CoolCube process: An alternative path to scaling*, 2015 Symposium on VLSI Technology (VLSI Technology), Kyoto, pp. T48-T49 (2015).
4) T. T. Wu et al., *Low-cost and TSV-free monolithic 3D-IC with heterogeneous integration of logic, memory and sensor analogy circuitry for Internet of Things*, 2015 IEEE International Electron Devices Meeting (IEDM), pp. 25.4.1-25.4.4 (2015).
5) P. Batude et al., *3D monolithic integration*, 2011 IEEE International Symposium of Circuits and Systems (ISCAS), pp. 2233-2236 (2011).
6) C. Fenouillet-Beranger, B. Previtali, P. Batude, F. Nemouchi, M. Cass, X. Garros, L. Tosti, N. Rambal, D. Lafond, H. Dansas, L. Pasini, L. Brunet, F. Deprat, M. Grgoire, M. Mellier, M. Vinet, *FDSOI bottom MOSFETs stability versus top transistor thermal budget featuring 3D monolithic integration*, Solid-State Electronics, Volume 113, Pages 2-8 (2015)
7) J. A. del *INanometre-scale electronics with III-V compound semiconductors*, Nature, 479, pp. 317323 (2011).
8) S. Lee, V. Chobpattana , C. Y. Huang , B. J. Thibeault , W. Mitchell , S. Stemmer , A. C. Gossard , M. J. W. Rodwell, ”Record Ion (0.50 mA/m at VDD = 0.5 V and Ioff = 100 nA/m) 25 nm-gate-length ZrO2/InAs/InAlAs MOSFETs, *Record Ion (0.50 mA/m at VDD = 0.5 V and Ioff = 100 nA/m) 25 nm-gate-length ZrO2/InAs/InAlAs MOSFETs*, 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers,

pp. 1-2 (2014).

9) Y. Sun A. Majumdar , C. W. Cheng , Y. H. Kim , U. Rana , R. M. Martin , R. L. Bruce , K. T. Shiu , Y. Zhu , D. Farmer , M. Hopstaken , E. A. Joseph , J. P. de Souza , M. M. Frank , S. L. Cheng , M. Kobayashi , E. A. Duch , D. K. Sadana , D. G. Park , E. Leobandung, *Self-aligned III-V MOSFETs: Towards a CMOS compatible and manufacturable technology solution*, 2013 IEEE International Electron Devices Meeting, pp. 2.7.1-2.7.4 (2013).

10) V. Djara, V. Deshpande, M. Sousa, D. Caimi, L. Czornomaz and J. Fompeyrine, *CMOS-Compatible Replacement Metal Gate InGaAs-OI FinFET With I_{ON} =156μ textAμ textm at V_{DD}= 0.5 V and I_{OFF}=100 nA/ μ textm*, IEEE Electron Device Letters, vol. 37, no. 2, pp. 169-172 (2016).

11) X. Zhou et al., *Scalability of InGaAs gate-all-around FET integrated on 300mm Si platform: Demonstration of channel width down to 7nm and Lg down to 36nm,*, 2016 IEEE Symposium on VLSI Technology, pp. 1-2 (2016).

12) M. L. Huang et al., *High performance In0.53Ga0.47As FinFETs fabricated on 300 mm Si substrate*, 2016 IEEE Symposium on VLSI Technology, pp. 1-2 (2016).

13) J. A. del Alamo, D. Antoniadis , A. Guo , D. H. Kim , T. W. Kim , J. Lin , W. Lu , A. Vardi , X. Zhao, *InGaAs MOSFETs for CMOS: Recent advances in process technology*, 2013 IEEE International Electron Devices Meeting, pp. 2.1.1-2.1.4 (2013).

14) C. B. Zota, G. Roll, L. E. Wernersson and E. Lind, *Radio-Frequency Characterization of Selectively Regrown InGaAs Lateral Nanowire MOSFETs* IEEE Transactions on Electron Devices, vol. 61, no. 12, pp. 4078-4083 (2014).

15) V. Deshpande, V. Djara , E. O'Connor , P. Hashemi , K. Balakrishnan , M. Sousa , D. Caimi , A. Olziersky , L. Czornomaz , J. Fompeyrine, *Advanced 3D Monolithic hybrid CMOS with Sub-50 nm gate inverters featuring replacement metal gate (RMG)-InGaAs nFETs on SiGe-OI Fin pFETs* IEEE International Electron Devices Meeting (IEDM), pp. 8.8.1-8.8.4 (2015).

16) Tong Ge, Linfei Guo, Huiqiao He, Kang Yang, Yu Jia, Joseph Chang, *Envelope Tracking RF Power Amplifiers: Fundamentals, Design Challenges, and Unique Opportunities Offered by LEES-SMART InGaAs-on-CMOS Process* Procedia Engineering, Volume 141, pp. 94-97 (2016).

17) M. Yokoyama et al., *High mobility IIIV-on-insulator MOSFETs on Si with ALD-Al2O3 BOX layers*, Symposium on VLSI Technology, pp. 235-236 (2010)

18) L. Czornomaz et al., *An integration path for gate-first UTB III-V-on-insulator*

MOSFETs with silicon, using direct wafer bonding and donor wafer recycling, 2012 IEEE International Electron Devices Meeting (IEDM), pp. 23.4.1-23.4.4 (2012).

19) Daix, N. and Uccelli, E. and Czornomaz, L. and Caimi, D. and Rossel, C. and Sousa, M. and Siegwart, H. and Marchiori, C. and Hartmann, J. M. and Shiu, K.-T. and Cheng, C.-W. and Krishnan, M. and Lofaro, M. and Kobayashi, M. and Sadana, D. and Fompeyrine, *Towards large size substrates for III-V co-integration made by direct wafer bonding on Si* APL Mater., 2, 086104 (2014)

20) V. Djara, V. Deshpande, E. Uccelli, N. Daix, D. Caimi, C. Rossel, M. Sousa, H. Siegwart, C. Marchiori, J. Hartmann, K.-T. Shiu, C.-W. Weng, M. Krishnan, M.Lofaro, R. Steiner, D. Sadana, D. Lubyshev, A. Liu, L. Czornomaz, and J. Fompeyrine, *An InGaAs on Si-platform for CMOS with 200 mm InGaAs-OI substrate, gate-first, replacement gate planar and FinFETs down to 120 nm contact pitch* 2015 Symposium on VLSI Technology (VLSI Technology), T176T177 (2015).

21) J. Widiez, S. Sollier, T. Baron, M. Martin, G. Gaudin, Frdric Mazen, F. Madeira, S. Favier, A. Salaun, R. Alcotte, E. Beche, H. Grampeix, C. Veytizou, J-S. Moulet, *300 mm InGaAs-on-insulator substrates fabricated using direct wafer bonding and the Smart Cut¢ technology*, Japanese Journal of Applied Physics, 55, 4S, pp. 04EB10 (2016)

22) J. Widiez, S. Sollier, T. Baron, M. Martin, G. Gaudin, Frdric Mazen, F. Madeira, S. Favier, A. Salaun, R. Alcotte, E. Beche, H. Grampeix, C. Veytizou, J-S. Moulet, *300 mm InGaAs-on-insulator substrates fabricated using direct wafer bonding and the Smart Cut¢ technology*, SSDM (2016)

23) T. Irisawa et al., *3D Integration of High Mobility InGaAs nFETs and Ge pFETs for Ultra Low Power and High Performance CMOS*, 2013 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, pp. 1-2 (2013).

24) T. Irisawa et al., *Demonstration of ultimate CMOS based on 3D stacked InGaAs-OI/SGOI wire channel MOSFETs with independent back gate*, 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, pp. 1-2 (2014).

25) P. Hashemi,M. Kobayashi , A. Majumdar , L. A. Yang , A. Baraskar , K. Balakrishnan , W. Kim , K. Chan , S. U. Engelmann , J. A. Ott , S. W. Bedell , C. E. Murray , S. Liang , R. H. Dennard , J. W. Sleight , E. Leobandung , D. G. Park, *High-performance Si1-xGex channel on insulator trigate PFETs featuring an implant-free process and aggressively-scaled fin and gate dimensions* Symposium on VLSI Technology (VLSIT), pp. T18-T19 (2013).

26) P. Hashemi,K. Balakrishnan , A. Majumdar , A. Khakifirooz , W. Kim , A. Baraskar , L.

A. Yang , K. Chan , S. U. Engelmann , J. A. Ott , D. A. Antoniadis , E. Leobandung , D. G. Park, *Strained Si1-xGex-on-insulator PMOS FinFETs with excellent sub-threshold leakage, extremely-high short-channel performance and source injection velocity for 10nm node and beyond* VLSI Technology (VLSI-Technology): Digest of Technical Papers, pp. 1-2 (2014).

27) Vladimir Djara, Marilyne Sousa, Nikola Dordevic, Lukas Czornomaz, Veeresh Deshpande, Chiara Marchiori, Emanuele Uccelli, Daniele Caimi, Christophe Rossel, Jean Fompeyrine, *Low Dit HfO2/Al2O3/In0.53Ga0.47As gate stack achieved with plasma-enhanced atomic layer deposition* Microelectronic Engineering, Volume 147, pp. 231-234 (2015).

28) V. Deshpande, V. Djara, E. OConnor, P. Hashemi, K. Balakrishnan, D. Caimi, M. Sousa, L. Czornomaz and J. Fompeyrine, *First RF Characterization of InGaAs Replacement Metal Gate (RMG) nFETs on SiGe-OI FinFETs Fabricated by 3D Monolithic Integration*, 2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), pp. 127-130 (2016).