RZ 3955 (#ZUR1709-024) 12/09/2017
Electrical Engineering 3 pages

Research Report

Monolithic integration of multiple III-V semiconductors on Si

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This is the accepted version of the article published by IEEE: H. Schmid, B. Mayer, J. Gooth, S. Wirths, L. Czornomaz, H. Riel, S. Mauthe, C. Convertino, and K. E. Moselund, "Monolithic integration of multiple III-V semiconductors on Si," Proc. SOI-3D-Subthreshold Microelectronics Technology Unified Conference (IEEE S3S, 2017).
10.1109/S3S.2017.8309200

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ABSTRACT

We review our work on the direct epitaxy of III-V compounds on Si using template-assisted selective epitaxy (TASE) and demonstrate its use for the integration of electronic and optical devices. The III-V material is grow within the confined space given by an oxide template structure and lead to a III-V on insulator structure which can be further processes into devices. Monolithic integration of a broad range of III-V compounds enabled the fabrication of III-V FETs, TFETs, ballistic devices as well as optically pumped microdisk lasers on Si.

I. INTRODUCTION

A system's computing performance is closely linked to the integration density of its components. By focusing primarily on device (transistor) down-scaling, computing power has been successfully improved over the past decades. However, nowadays integration must apply to all components to achieve a relevant system performance gain and therefore greatly benefits from emerging multi-chip packaging solutions enabling high bandwidth, for example. Obviously, the integration density is maximized going from 2D towards 3D either by stacking processed dies on top of each other or adding an additional layer on the device level. These aggressively pursued packaging solutions can bring another important benefit nearly for fee, namely the combination of functionalities requiring different semiconductor or substrate materials. Illustrative examples are: CCD chips, were the computing-, memory- and photodiode layer are bonded together [1], RF and logic applications with III-V device layer bonded onto a Si circuit [2, 3], and integrated optics with bonded lasers [4]. In contrast to above packaging / bonding approaches, epitaxial approaches towards dense integration of multiple semiconductors are less established [5]. Figure 1 illustrates the envisioned space for dense, epitaxial device level integration compared to established chip level packaging. Here we address some of the key obstacles for epitaxial integration, show an approach that circumvent previous shortcomings, and which might inspire novel device architectures. The difficulty in hetero epitaxy stems from thermal and lattice mismatch, and existence of polar / non-polar material interfaces, resulting in propagating defects and therefore defective layers. The art of hetero epitaxy engineering is to suppress and/or confine the defective interface layer close to the substrate, such as to keep defects away from the device layer. This can be done by careful surface preparation, introduction of nucleation and buffer layers, annealing strategies, and/or the use of structured or masked substrates [6]. Here, we will first introduce an epitaxial growth technique, TASE [7,8,9] which is based on the local confinement of III-V growth, then detail on material characterization and show fabricated devices.

II. SELECTIVE EPITAXY IN TEMPLATES

Material interfaces in hetero-epitaxy are often difficult to control. However, reducing the interfacial area can significantly relax some of the previously mentioned constraints compared to a bulk situation. Therefore, ideally only the orientation of the crystal lattice needs to be transferred from the substrate to the epi layer which can serve as seed for an epitaxial crystal. This is conceptually illustrated in Fig. 2a and is implemented by fabricating a mold or template that serves as solid state confinement during vapor phase epitaxy. Each template, whether on bulk Si or SOI, contains a (Si) seed area for nucleation. Metal-organic chemical vapor deposition (MOCVD) is well suited for selective area growth due to the long diffusion length of the precursor molecules which allows migration through the entire cavity to the seed area. Compared to blanket epitaxy, the optimal growth parameters in selective area epitaxy must be adapted to account for the modified mass transport which needs to be established for each material and composition. So far, arsenides, phosphides and antimonides have been deposited in the templates and processed to devices as detailed below. In all cases investigated, the Si-III-V hetero-junction is decorated with misfit dislocations which relax the significant lattice strain between the materials. Beyond the junction area, the deposited material is free from propagating dislocations and anti-phase or grain boundaries. However, in most compounds a high density of planar defects (stacking faults and twins) are observed that run through the entire crystal.

III. INTEGRATION ON SI

The selective and epitaxial filling of semiconductors in a wide range of geometries using template structures is interesting for the implementation of vertical, lateral and 3D stacked device layouts. Selected examples of fabricated structures are presented in Figure 3. Fig. 3(a) shows vertically InAs nanowires, also including a vertical heterostructure. Notable here is the fact that the wires were grown on different oriented Si substrates, including Si(001), useful for implementing interconnects or devices. The typical lateral geometry is shown in Fig. 3(c). Here, a nanowire or fin structure

including a constriction was directly grown without the need for post patterning. Alternatively lithographically defined fins can be obtained using sheet-like structures as starting material as shown in the adjacent image. Such sheets structures are also well suited to carry out Hall bar measurements, from which we have extracted a Hall mobility for InAs of 5400 cm^2/Vs [8], and for GaSb 760 cm^2/Vs [10]. The electron and hole mobility is similar to the mobility of thin films obtained from bulk InAs or GaSb wafers. Finally, Fig. 3 demonstrates a stacked configuration of fins or sheets. Here, a template structure according to Fig. 3(d) was fabricated first and after partial removal of the Si, the hollow channels were epitaxially filled with GaAs Fig. 3(d). Templates can also be filled in a sequential manner with different compounds [10] resulting in the formation of co-planar or stacked multi-material substrates. These examples illustrated some appealing features of template-assisted selective epitaxy.

IV. III-V FET AND TFETS

We have focused on InAs and GaSb because of their advantageous material properties, foremost carrier mobility, for FETs. Alternatively, combined in a heterostructure design, it hold also promise for TFETs. Fig. 4 shows a selected overview of devices which were all fabricated on Si (001). Cross-section TEM and SEM images of the channel areas are displayed on top with corresponding device characteristics below. An InAs n-FET and the output curve of a 55nm wide device is shown in Fig. 4(a). Here, the InAs was first grown in the 25-nm thick channels [8]. After template removal and gate stack deposition (Al2O3/HfO2/TiN, EOT 1.2 nm). At V_{DS} = 0.5 V we measure Ion of 330 µA/µm and Ion/Ioff of 28 due to a poor SS of 250 mV/dec. The maximum transconductance (gm) at 0.5 V is 1.0 mS/µm. Much improved devices fabricated using a self-aligned process including raised S/D contacts were recently shown [9]. The fabricated started from 1-$µm^2$ sized In0.7Ga0.3As sheets, where 35-nm-wide channels were etched out and fabricated into FETs. Using a similar process, FETs with gate length down to 35 nm were fabricated adjacent to SiGe p-FETs into inverters and SRAM cells [11] underlining the potential of an integration approach based on epitaxy.Heterostructure designs with broken or staggered band alignment are well suited for TFETs. A subthreshold swing below 50mV/dec at room temperature using an InAs-GaSb nanowire junctions has recently been reported [12]. We fabricated two heterostructure devices based on InAs-Si [13] and InAs-GaSb junctions for p- and n-TFETs, respectively [14]. Similar to the InAs FET, the TFETs are directly grown as nanowires, which enables lateral III-V junction formation. Fig. 4(b) shows the channel cross-section with the InAs source and the Si drain. The temperature-dependent transfer characteristic is shown below, normalized to the circumference (100 nm) of the device. An Ion of 4 µA/µm and on/off ratio of 10^6 with SSavg < 80 mVdec is obtained. A significant thermally (trap) assisted current is noticeable at low current levels, while the good on/off ratio reflects the benefit of the large Si bandgap. Fig. 4(c) shows the n-TFET which shows the expected higher current density (I_{on}=40 µA/µm) due to the larger tunnel probability. However, despite the lattice matched junction, a poor SS (1 V/dec) and on/off ratio (~400) results of a non-optimized gate stack and doping levels.

V. BALLISTIC TRANSPORT DEVICES

InAs is a preferred semiconductor for ballistic transport studies. Ideally, devices must be small and have minimal bulk and surface defects to avoid random carrier fluctuations. Compared to widely used simple nanowire structures, we investigated ballistic transport in a four terminal devices using directly grown InAs crosses. This allowed to measure bend resistance, as well as ballistic transport in devices with multiple InAs leads [16]. Fig 6 shows a representative measurement revealing symmetric, quantized conductance.

VI. MICRODISK LASERS

Integrated optical functions on CMOS are foreseen to play an important role in computing and sensing applications. Typically pre-fabricated lasers are mechanically transferred to the substrate. Here we integrated a 300nm thick GaAs-AlGaAs core-shell crystal on Si using a large cavity as illustrated in Fig. 7. The disk dimensions and presence of the 130nm thick underlying oxide support the formation a high quality optical mode. Fig. 8 shows the results of optically pumping at 710nm. The integrated PL intensity as function of excitation exhibits a clear kink along with a strong linewidth reduction at a lasing threshold of 18 pJ/pulse, and lasing even up to room temperature.

CONCLUSION

We have reviewed our approach on heterogeneous material integration at a microscopic level on Si. Micron sized compound semiconductor dies on Si were fabricated using template-assisted selective epitaxy and were processed into various electrical and optical devices, showing the versatility of the approach.

Acknowledgment

The authors gratefully acknowledge the contributions of M. Borg, S. Sant, and W. Riess. The work received funding in part from the European Union Seventh Framework Program (FP7/2007-2013) E2Switch (Grant no. 619509), and in part by the European Union H2020 program INSIGHT (Grant no. 688784), and ERC project PLASMIC, and Marie Curie Post-Doctoral Research Fellowship “MODES”.

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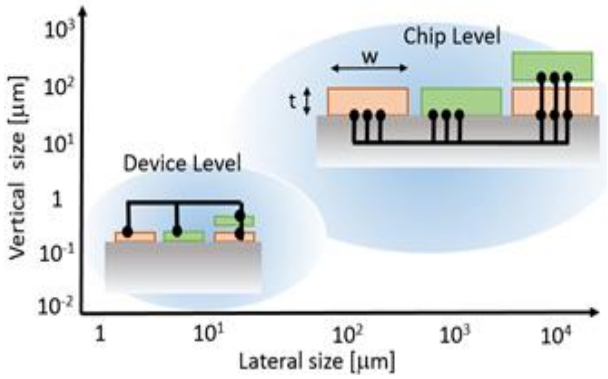

Fig. 1. Heterogeneous integration across all scales. The axes indicat thickness and width of individual macroscopic or microscopic die respectively. Here we explore the integration of microscopic dies o silicon via direct epitaxial processes.

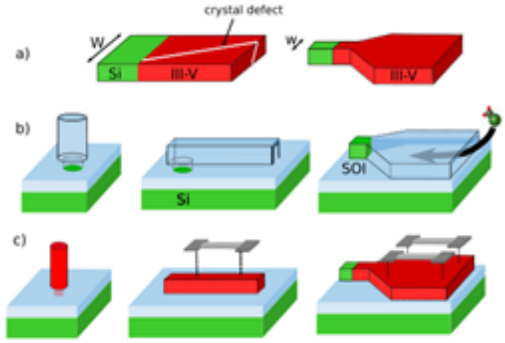

Fig. 2. Schematics illustrating the concept of TASE. (a) Growth from a small nucleation area can suppress defect formation at mismatched interfaces. (b) Implementation of SiO_2 templates: vertical, and lateral on bulk and SOI wafers. (c) Resulting epitaxial deposits after template removal, starting point for device fabrication.

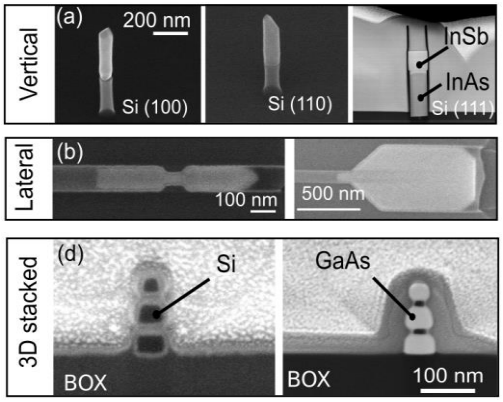

Fig. 3. Illustration of vertical, lateral and stacked epitaxial material integration. (a) Vertical InAs and InSb-InAs on Si. (b) Lateral structures with constriction and expanded platelet, both filled from left to right. (d) X-section images of stacked Si nanowires from which GaAs nanowires were grown.

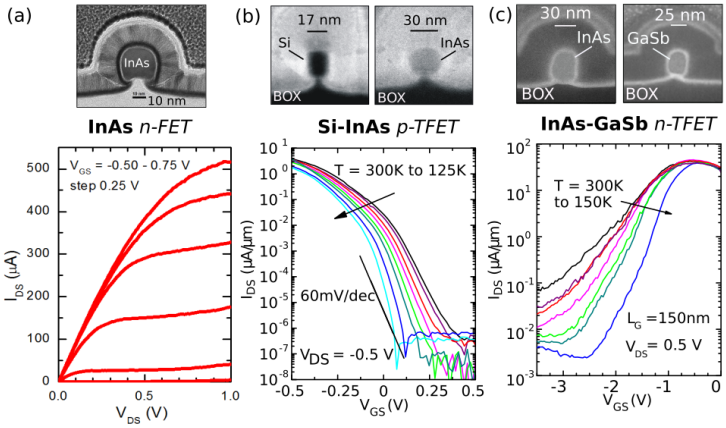

Fig. 4 Cross-section images showing the channel region of field effect devices and representative measurements. (a) Wrap gate FET with InAs channel (b) Si-InAs heterojunction tunnel-FET (c) InAs-GaSb tunnel-FET.

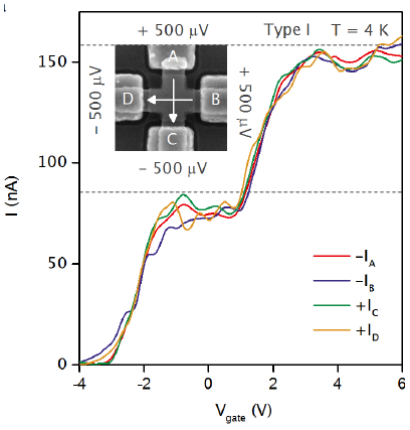

Fig. 6. Low temperature, four terminal transport measurements through an InAs cross. Similar quantized conductance is observed for all wiring schemes, as illustrated in the inset.

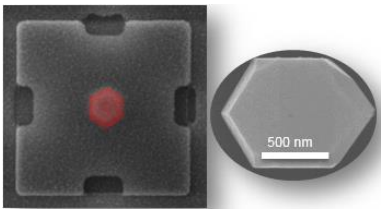

Fig. 7. Microdisk laser grown on Si. (a) SE image of a square shaped template with fo openings. A GaAs crystal (red) is located the center. (b) 300 nm thick GaAs crystal (a) after removal of SiOx template.

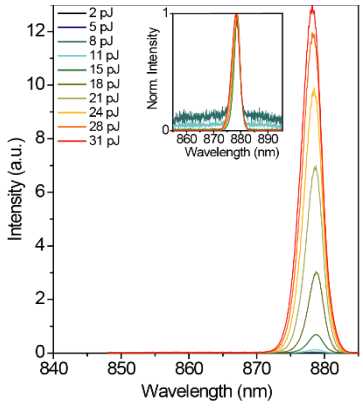

Fig. 8. Optical pumping and resulting lasing characteristics of the GaAs disk shown in fig 7.