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Research Report

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ABSTRACT

In this paper we report on our work on the monolithic integration of various III-V compounds on Si using template-assisted selective epitaxy (TASE) and its application for electronic devices. Nanowires, crossbar nanostructures, and micron-sized sheets are epitaxially grown on Si via metal-organic chemical vapor deposition and form the basis for III-V MOSFETs and Tunnel FETs. Epitaxy conditions specific to TASE are discussed and material quality assessed. Here, we focus on InAs and GaSb as a potential all-III-V alternative to complementary group IV technology. Scaled n-FETs as well as both n- and p-channel TFETs are fabricated on Si and illustrate the potential of TASE.

I. INTRODUCTION

Incorporation of additional, value added functionalities on future silicon dies most likely requires the integration of more semiconducting materials compared to what we have seen until now. A visionary goal is illustrated in Fig. 1, where various devices are integrated on Si with compounds selected based on their suitability to a specific targeted application. For this vision to materialize, dense monolithic integration onto a common Si wafer is key. However, cointegration of e.g. a wide band gap nitride with a narrow gap antimonide semiconductor is obviously not trivial from an epitaxial point of view, nor from the thermal budget available for device processing. Traditional hetero-epitaxy typically suffers from lattice mismatch, resulting in defective layers. The art of hetero epitaxy is to suppress and confine the defective interface layer close to the substrate, such as to keep defects away from the device layer. This may be achieved by nucleation and buffer layers, annealing strategies, and/or the use of masked substrates [1-4] which significantly reduces defects propagation. Here we report on an epitaxial growth technique, TASE that is based on the local confinement of III-V growth, and simplifies scaled, co-integration of multiple semiconductors on Si. Using TASE we demonstrate (1) high mobility in InAs (5400 cm^2/Vs) and GaSb (760 cm^2/Vs) films, (2) InAs FETs with on current, I_{on} of 660 µA/µm and peak transconductance (g_m) of 1.0 mS/µm at V_{DS} = 0.5 V, and (3) complementary TFET technology based on scaled InAs-Si and InAs-GaSb TFETs with I_{on} ~4 µA/µm, I_{on}/I_{off} ~10^5, and I_{on} ~40 µA/µm, I_{on}/I_{off} ~400, respectively.

II. TEMPLATE-ASSISTED SELECTIVE EPITAXY

The concept of TASE is illustrated in Fig. 2. A hollow SiO_2 template structure is pre-fabricated which contains a small Si seed area. The template is epitaxially filled starting from the seed, which assures a single nucleation point. Since the resulting large crystal is expanded from one nucleation point, typical defects found in planar epitaxy are absent. Extending growth from a small seed bears similarity to nanowire growth [5], but with the benefit of a template-defined overall geometry, and not limited to the typical [111] growth direction. This is exemplified in Fig. 3a were nanowires are grown vertically, independent of the crystalline orientations of the Si substrate [6]. Fig. 3b illustrates implementations of TASE in a planar orientation, showing flexibility of growth direction and shapes [7]. Here (001) silicon-on-insulator (SOI) substrates were used. Epitaxy in scaled, fin-shaped templates can be directly processed into devices, while sheet-like structures are suitable for further conventional patterning steps. Towards the vision shown in Fig. 1, we integrated multiple materials in a coplanar, as well as stacked implementation (Fig. 4). Metal-organic chemical vapor deposition (MOCVD) is particularly well suited for selective area growth due to the long diffusion length of the precursors (Fig. 5a). We found that the growth dynamics depend on the precursors used: InAs TASE shows a growth rate dependence on template width due to a locally reduced V/III ratio [8] while GaSb exhibits a nearly independent growth rate explained by the high Sb surface coverage. Important for epitaxy in templates is the control over growth planes, sketched in Fig. 5b, which defines growth and junction formation. Structural transmission electron microscopy (TEM) analysis of the InAs and GaAs samples (Fig. 6) show the absence of propagating dislocations and anti-phase boundaries. Misfit dislocations which relax the strain between the materials are present and confined to the Si – III-V interface. For InAs, a high density of planar defects (stacking faults and twins) is observed, while for $In_{0.7}Ga_{0.3}As$, GaAs, InP, and GaSb these defects can be suppressed.

III. HALL-BAR DEVICES

We have focused on InAs and GaSb because of their potential for n-FETs [9], p-FETs [10] as well as TFETs [11]. Electrical characterization to assess resistivity, sheet resistance and contact resistance of the materials is done by transmission line measurements on nanowires. For Van der Pauw (VDP) and Hall measurements, dedicated samples are grown. Fig. 7a shows a 23-nm-thick InAs cross-bar with 95 nm wide legs. VDP results in a sheet resistance of 1260 Ω/sq., and a resistivity of 2.95 mΩ·cm. The sheet carrier density from Hall measurements is 9.1×10^{11} cm^{-2} and results in electron charge concentration n_e = 3.9×10^{17} cm^{-3} and Hall mobility of 5400

cm^2/Vs. For the GaSb sample [9] (Fig. 7b) a 20-nm-thick and 500 nm by 1000 nm wide film is grown and contacted by Ni leads. The measurements show a sheet resistance of ~15.8 kΩ/sq, and a resistivity of 31 mΩ·cm. The sheet carrier density is $4.8x10^{11}$ cm^{-2} and results in hole charge concentration n_h = $2.4x10^{17}$ cm^{-3} and average Hall mobility of 760 cm^2/Vs [12]. The large *e* and *h* mobility obtained confirm a good quality of the as-grown crystal.

IV. Ballistic Transport

InAs and InSb are interesting materials to study ballistic and transport properties [13]. For RT operation, devices must be small and with minimal surface defects to avoid scattering. To investigate ballistic transport in our structures, we performed bend resistance measurements on InAs cross-bars contacted with Ni, but without removing the template on the channel area. Fig. 8 shows the bend-resistance $R_B = V_{12}/I_{34}$ of a 300 nm long cross-bar as a function of magnetic field and temperature applying a constant current of I_{34} = 100 nA. If the transport would be purely diffusive, the measured voltage drop would be $V_{12} > 0$. However, we observe a negative bend resistance for all temperatures investigated, revealing ballistic transport in our devices. The high quality of the measurements was made possible by the low defect density of the device interfaces of the TASE grown structures.

V. III-V MOSFETs

We have fabricated scaled III-V MOSFETs on Si by growing InAs directly in ten 25-nm-thick and 55-nm-wide channels [7]. After template removal, an Al_2O_3/HfO_2/TiN gate stack (EOT 1.2 nm) was deposited by ALD. The gate metal patterning was followed by Ni/Pd SD contacts. Fig.9 shows the device geometry and output, transfer and transconductance characteristics. The current density is normalized by taking the width of ten nanowires for normalization. Using $V_{CC} = V_{DS}$ = 0.5 V we measure I_{on} of 330 µA/µm and I_{on}/I_{off} of 28 due to a poor SS of 250 mV/dec. Using $V_{CC} = V_{DS}$ x SS/60 = 2 V instead, an I_{on}/I_{off} of 2300 is extracted, and I_{on} at V_{DS}=0.5 V is 660 µA/µm. The maximum transconductance (gm) at 0.5 V is 1.0 mS/µm. R_{on} is 1.2 kΩ and is dominated by series resistance stemming from the ungated source and drain access regions as well as contact resistance. High-density III-V CMOS integration can be also achieved starting from 1-µm² sized $In_{0.7}Ga_{0.3}As$ sheets grown in templates, where 35-nm-wide channels were etched out and fabricated into FETs using a self-aligned process with raised S/D contacts [13]. In a follow-up [14] using the same $In_{0.7}Ga_{0.3}As$ channel material, FETs with gate length down to 35 nm were fabricated adjacent to SiGe p-FETs into inverters and SRAM cells underlining the integration potential.

VI. Heterojunction TFETs

TFETs for ultra-low power electronics are preferably based on heterostructure designs that benefit from broken or staggered band alignment. We fabricated heterostructure devices based on InAs-Si [15] and InAs-GaSb junctions for p- and n-TFETs, respectively [16]. Similar to the InAs FET, the TFETs are directly grown as nanowires, which enables lateral III-V junction formation and avoids simultaneous RIE etching of the two dissimilar channel materials. Both devices used the same gate stack (Al_2O_3/HfO_2, EOT~1.75nm) with TiN or W gates, and Ni/Au S/D contacts. Fig. 10 shows p-TFET device images and temperature-dependent transfer characteristic, normalized to the circumference (100 nm) of the Ω-device. An I_{on} of 4 µA/µm at V_{GS}=V_{DS}=-0.5 V, and on/off ratio of 10^6 with SS_{avg} < 80 mVdec is obtained. The n-TFET is shown in Fig 11 it exhibits a higher I_{on} (40 µA/µm), but poor SS (1 V/dec) and on/off ratio (~400) as a result of a non-optimized gate stack and doping levels. A dip in the on-state current is observed and attributed to the on-set of depletion in the undoped GaSb channel. The output characteristics of the TFETs are displayed in Fig. 12 and Fig. 13. Negative differential resistance in forward bias is not observed for the p-FET at the gate bias conditions used and in agreement with TCAD simulations [18]. Geometric phase analysis of the Si-InAs (Fig. 14) reveals misfit dislocations which are expected to be a source of trap states limiting SS performance. In comparison these defects are absent in the InAs-GaSb device indicating that the fabricated n-TFET is limited by large oxide-semiconductor interface defect density instead, responsible for the poor SS characteristics.

Conclusion

We have reviewed our growth and device work based on TASE [Fig. 15] and demonstrated a path for local integration of III-V semiconductors and devices on Si without constraints of lattice constants. Device integration was demonstrated by fabricating scaled, functional FETs and TFETs on Si.

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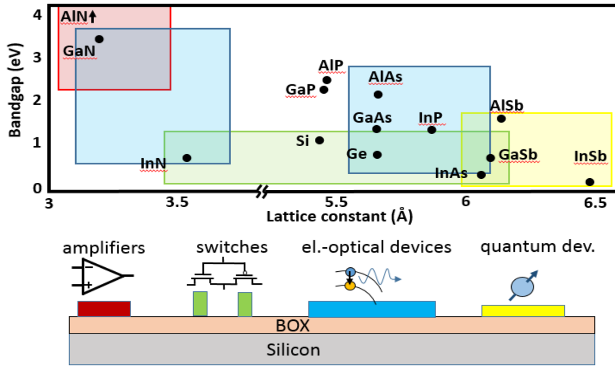

Fig. 1. Bandgap vs. lattice constant of important semiconductors and schematic of a hypothetical universal substrate. Colors reflect application areas. The Si substrate incorporates semiconductors according to their best functionality, independent of lattice parameter constraints.

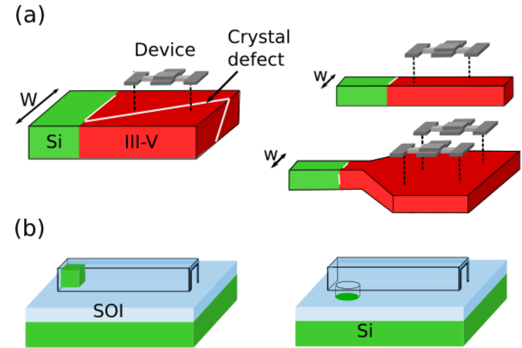

Fig. 2. Schematics illustrating the concept of TASE. (a) Growth from a small (Si) seed area, which can be followed by extended growth avoids defect formation and propagation. (b) Implementation of TASE using hollow SiO_2 templates on SOI and bulk Si wafers with Si seed area.

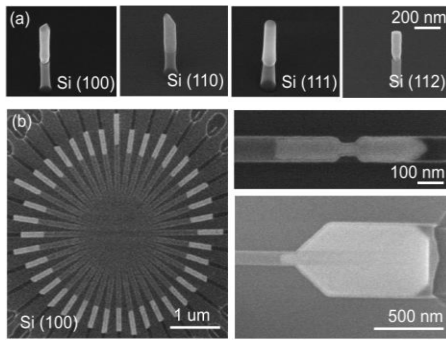

Fig. 3. Epitaxial growth of InAs on Si illustrating design flexibility. (a) Tilted SEM view of vertical nanowires grown on four different Si substrate orientations. (b) Star pattern, wire structure with a constriction and extended sheet, both filled from left to right on SOI substrate. Template has been removed in all images.

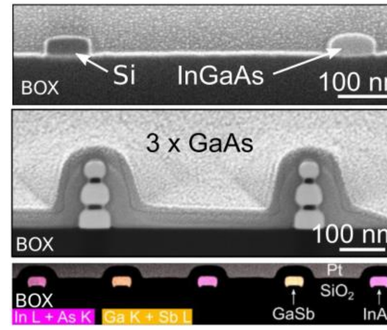

Fig. 4. Cross-section images of Si, InAs, InGaAs, GaAs and GaSb structures along [110] on Si (001). False colored image based on EDS analysis. InAs/GaSb on Si grown in two separate MOCVD steps.

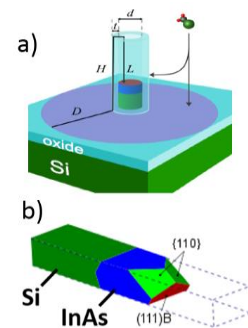

Fig. 5. (a) Precursor transport by vapor phase and surface diffusion during TASE [8]. (b) Growth front depends on epi conditions used. The illustration example shows a mixed {110} and (111) plane.

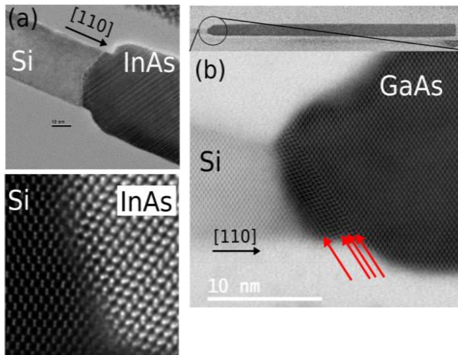

Fig. 6. TEM images of the Si-III-V junctions. (a) Si-InAs sample with high density of planar defects on (111) planes. (b) GaAs with optimized epi conditions. Four stacking faults close to the junction observed, rest of structure free of planar defects. Anti-phase boundaries or threading dislocations were not detected in all cases.

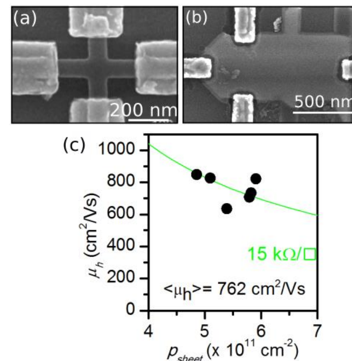

Fig. 7. Hall bar devices and analysis. (a) Grown InAs crossbar, 23-nm-thick with Ni contacts, Hall electron mobility μ_e = 5400 cm^2/Vs. (b) GaSb sheet, 20-nm- thick with Ni contacts. (c) Plot of hole mobility (μ_h) vs. carrier concentration from Hall measurements.

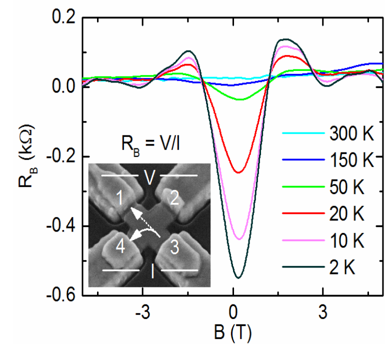

Fig. 8. Magnetic field-dependent bend resistance of a 100-nm-wide and 30-nm-thick InAs cross-junction at various temperatures. Negative bend resistance is observed, indicating ballistic transport and high-quality of TASE grown structures.

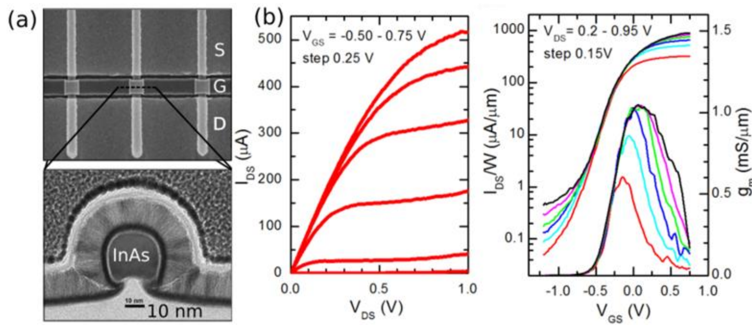

Fig. 9. (a) Top view and cross-section images of 25nm diameter InAs n-MOSFET. The BOX is under etched to form a Ω-structure. I_{on} at V_{DS} =0.5 V is 500 μA/μm. The maximum conductance (gm) at 0.5 V is 0.8 mS/μm. (b) Output curve of the 55nm wide devices and normalized transfer curve, adapted from ref [7]. I_{on} at V_{DS}=0.5 V is 660 μA/μm. The maximum conductance (g_m) at 0.5 V is 1 mS/μm. III-V channel thinning or RIE step were not used for device fabrication.

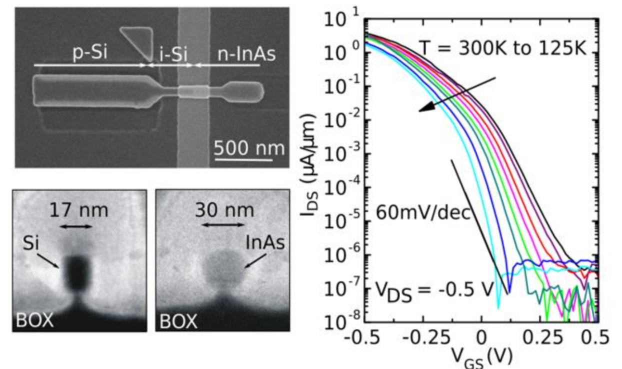

Fig. 10. Top view and cross-section images of the InAs-Si heterojunction p-TFET. Temperature-dependent transfer characteristic with I_{on} = 4μA/μm at V_{DS}=-0.5V, on/off ratio of 10^6 with SS_{avg} < 80mV/dec. Drop in I_{on} at low T due to residual barrier at metal contacts.

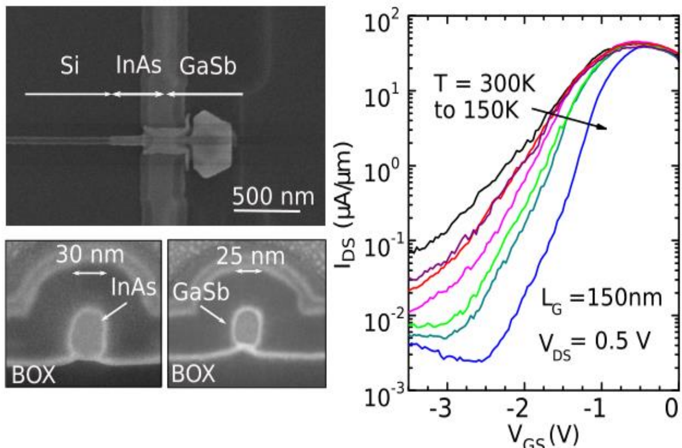

Fig11. Top view and cross-section images of the InAs-GaSb heterojunction n-TFET. Temperature-dependent transfer curve, with I_{on} = 40μA/μm at V_{DS}=-0.5V, on/off ratio of 400 with SS_{avg} ~ 1V/dec. Drop in I_{on} at low temperature due to GaSb depletion, while BTBT is temperature independent.

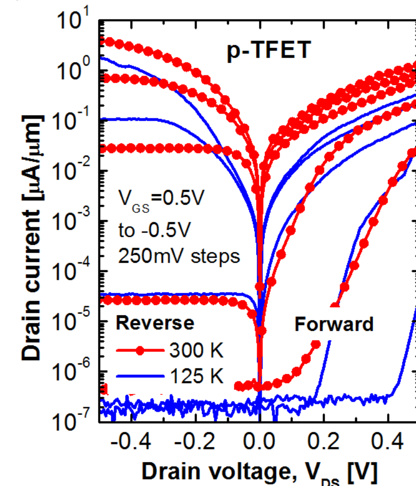

Fig. 12. Current-voltage curve of gated InAs-Si diode. The reverse bias branch corresponds to output characteristics of the p-TFET. For our measurement conditions NDR is not observed, but predicted at higher bias by TCAD simulations.

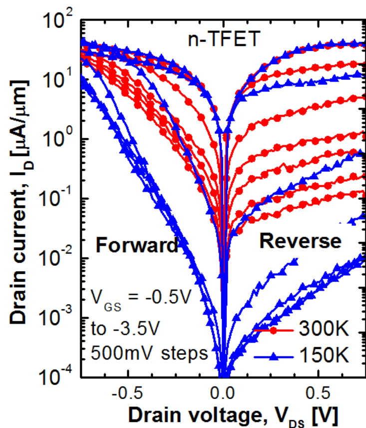

Fig. 13. Current-voltage curve of gated InAs-GaSb diode. The reverse bias branch corresponds to the output characteristics of the n-TFET. NDR is usually measured in diodes [17], but not here likely due to a high level of D_{it} at the III-V/high-k interfaces.

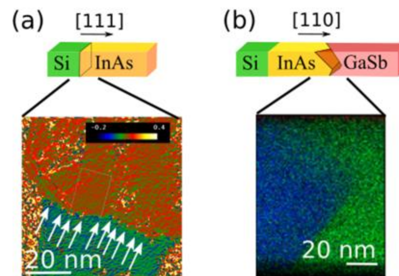

Fig. 14. Schematic and structural analysis of two heterojunctions. (a) Geometric phase analysis of a Si-InAs junction based on TEM image. Misfit dislocations are indicated, which can lead to trap states. (b) InAs-GaSb junction. EDX elemental analysis of As (blue) and Sb (green). The upper part appears blurred due to non-perpendicular viewing direction. No misfit dislocations detected by STEM.

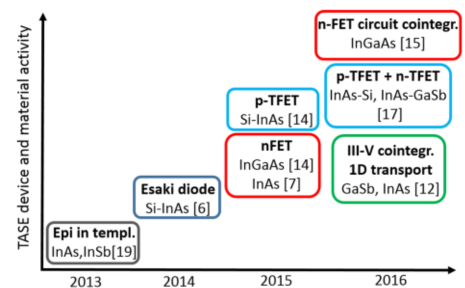

Fig. 15. Evolution of TASE-based work, spanning growth, materials and device activities all with focus towards CMOS compatibility.