RZ 3957 (#ZUR1707-067) 07/30/2017
Electrical Engineering 4 pages

Research Report

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H. Hahn[1], V. Deshpande[1], E. Caruso[2], S. Sant[3], E. O'Connor[1], Y. Baumgartner[1], M. Sousa[1], D. Caimi[1], A. Olziersky[1], P. Palestri[2], L. Selmi[2], A. Schenk[3] and L. Czornomaz[1]

[1] IBM Research GmbH Zürich Laboratory, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland

[2] Dipartimento Politecnico di Ingegneria e Architettura (DPIA), University of Udine, via delle Scienze 206, 33100 Udine, Italy

[3] Integrated Systems Laboratory, ETH Zurich, CH-8092 Zürich, Switzerland

This is the accepted version of the article published by IEEE: H. Hahn, V. Deshpande, E. Caruso, S. Sant, E. O'Connor, Y. Baumgartner, M. Sousa, D. Caimi, A. Olziersky, P. Palestri, L. Selmi, A. Schenk and L. Czornomaz, "A Scaled Replacement Metal Gate InGaAs-on-Insulator n-FinFET on Si with Record Performance," Proc. 2017 IEEE International Electron Devices Meeting (IEDM 2017). 10.1109/IEDM.2017.8268410

A Scaled Replacement Metal Gate InGaAs-on-Insulator n-FinFET on Si with Record Performance

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[3]Integrated Systems Laboratory, ETH Zurich, CH-8092 Zürich, Switzerland

email: luk@zurich.ibm.com

***Abstract*—**We demonstrate a scaled replacement-metal-gate InGaAs-on-Insulator n-FinFET on Si with L_G = 13 nm and record I_{ON} of 249 µA/µm at fixed I_{OFF} = 100 nA/µm and V_D = 0.5 V. A subthreshold swing in saturation of 89 mV/dec and a R_{on} of 355 Ω·µm is also achieved. We further investigate the transport mechanisms at play in order to shed light on the contribution from short-channel effects and carrier generation and recombination mechanisms on *SS* and I_{OFF}, at such a short gate length, using calibrated full 3D and simplified 2D TCAD simulations.

I. Introduction

High-mobility III-V materials such as InGaAs are being considered to replace strained Si in nFETs for future low power logic application [1, 2, 3]. Besides this, III-V channel materials have been shown to be well-suited for 2D co-planar [4] or 3D monolithic integration with Si/SiGe FETs [5, 6], in a 3D circuit demonstration [7]. Multi-gate device architecture has become the preferred solution for advanced technology nodes. For aggressive L_G scaling, fin dimension scaling is necessary in order to maintain electrostatic integrity [2, 8, 9]. This requires highly optimized processes both for the fin and gate definition. While small fin sizes have already been demonstrated recently with a replacement metal gate flow [10, 11], these demonstrations have been limited to relatively larger L_G. In this work, we combine small fin width and short gate length for an InGaAs-on-Insulator replacement metal gate FinFET on a Si substrate. It allows us to demonstrate a CMOS-compatible InGaAs n-FinFET suitable for both 2D and 3D monolithic integration with the highest reported performance to date on Si, at a gate length comparable to recent report on sub-7 nm node targets [12]. At L_G = 13 nm, we show low subthreshold swing (*SS*), low drain-induced barrier lowering (*DIBL*) and a record I_{ON} of 249 µA/µm at a fixed OFF-current I_{OFF} of 100 nA/µm and supply voltage V_D = 0.5 V. We also investigate the contribution from short-channel effects and carrier generation/recombination on *SS* and I_{OFF} using calibrated full 3D and simplified 2D TCAD simulations.

II. Device Fabrication

Devices were fabricated on an InGaAs-on-Insulator on Si platform. A cross-sectional schematic of the final device (**Fig. 1a**), its corresponding 3D TCAD setup (**Fig. 1b**) and the outlined process flow (**Fig. 2a**) are presented. Firstly, a 20-nm thick $In_{0.53}GaAs$ channel material was integrated on Si by direct wafer bonding technique [13]. This technique allows for thin-layer transfer even on large-scale substrates [14, 15]. In the next step, InGaAs fins were patterned by employing a dry-etch process. The fin dimensions down to W_{fin} = 17 nm were achieved. High-resolution TEM images were used to extract the gated fin perimeter for current normalization (**Figs. 2b,c**). Following this step, dummy gates were patterned using an optimized inductively-coupled plasma reactive ion etch (ICP-RIE). It allows us to obtain short gate length devices with L_G down to 13 nm, extracted as the physical length of the gate metal foot (**Figs. 2d,e**). After the subsequent regrowth of n^+-InGaAs for forming the raised source and drain (RSD), the devices were cladded with an interlayer dielectric (ILD) and planarized by chemical-mechanical polishing (CMP) that also enabled us to directly access the dummy gates. Following the dummy gate removal, a scaled Al_2O_3/HfO_2 bilayer dielectric stack was deposited using plasma-enhanced atomic layer deposition (PE-ALD). In the same step, TiN layer was also deposited *in-situ* which acts as work-function defining metal. After W-fill, a final CMP step was employed to planarize the metal gate layer. A second ILD layer was then deposited and subsequently opened to form the metal contacts (M1).

III. Device Performance and Discussion

C-V measurements performed on reference MOS capacitors (MOSCAPs) with the deposited gate stack are shown in **Fig. 3**. It shows a capacitance equivalent thickness (CET) of 1.25 nm and a low dispersion in frequency in the V_G range -0.1 V to 0.1 V pointing to a low interface state density (D_{it}). **Fig. 4** presents the transfer characteristics (I_D-V_G) of a long channel FinFET with L_G = 500 nm and W_{fin} = 17 nm. **Fig. 5** shows *SS* vs. I_D for the same device. A subthreshold swing below 70 mV/dec for over more than two orders of magnitude of drain current is observed in the V_G range -0.1 V to 0.1 V. The minimum *SS* (@V_D = 50 mV) is 65 mV/dec, which corresponds to a D_{it} of $2x10^{12}$ $cm^{-2}\cdot eV^{-1}$.

Values for linear and saturation *SS* (SS_{lin} and SS_{sat}) are plotted vs. L_G for the different W_{fin} in **Figs. 6 and 7**, respectively. For the devices with the smaller fin dimension, SS_{lin} and SS_{sat} maintain values close to 70 mV/dec and 75 mV/dec respectively, throughout the whole L_G range. The difference between SS_{lin} and SS_{sat} especially at larger W_{fin} and

L_G cannot be explained simply by short-channel effects. *DIBL* values extracted between V_D = 50 mV and 0.5 V are plotted vs. L_G in **Fig. 8**, showing a baseline *DIBL* of about 25 mV. This value increases to a moderate 49 mV for the shortest W_{fin} devices, demonstrating excellent electrostatic control down to L_G = 13 nm.

Fig. 9 presents extrinsic resistance (R_{ext}) extraction by plotting R_{on} vs. L_G for different W_{fin}. Owing to the spacer-free design of our FinFETs, the extrinsic resistance is as low as 220 Ω·µm for fin widths equal to or larger than 37 nm. R_{ext} is increasing to above 300 Ω·µm for the smallest fins. We also notice an increase in the sheet resistance of the channel (R_{on} vs. L_G slopes in Fig. 9) for the smallest fins. This indicates a decrease of the channel mobility that originates most likely from increased surface roughness scattering.

Fig. 10 shows the transfer characteristics of a scaled device with L_G = 13 nm and W_{fin} = 17 nm. A record-high ON-current of 249 µA/µm at a fixed I_{OFF} = 100 nA/µm and V_D = 0.5 V is extracted. Gate leakage (not shown) remains below 10^{-10} A/µm. The device further shows excellent low values for the linear and saturation *SS* of 69 mV/dec and 89 mV/dec respectively, and a *DIBL* of 48 mV. Owing to lower D_{it} and excellent electrostatics control of the channel such low SS values could be achieved at a gate length range targeted for sub-7 nm nodes. In terms of electrostatics, this demonstration compares very well with the state-of-the-art Si devices reported recently at similar gate length [12]. In **Fig. 11**, the output characteristics for this device are shown. The maximum drain current I_D is extracted to be above 800 µA/µm while the R_{on} of this device is 355 Ω·µm.

Fig. 12 reports I_{OFF} at V_D = 0.5 V vs L_G for various W_{fin}. It indicates that the smallest W_{fin} is required for reaching the high-performance (HP) I_{OFF} target of 100 nA/µm at the shortest L_G. It also reveals an abnormally high I_{OFF} even at longer L_G which cannot be explained by gate leakage.

The OFF-state transport mechanisms are further investigated by TCAD simulations (with Synopsis Sentaurus version M). Two setups were used: a) a full 3D TCAD setup that exactly matches our device geometry (*cf.* Fig. 1b), and b) a simplified 2D TCAD setup for which a circular symmetry was employed to approximate our smallest fin by a nanowire geometry and an infinite out-of-plane boundary condition was employed to reproduce the planar devices (not shown). Both TCAD setups were extensively calibrated as part of the III-V-MOS EU project (www.iii-v-mos-project.eu). The 3D model is matching two L_G and three W_{fin} with a single parameter set. The 2D model is matching three L_G and two different geometries (smallest W_{fin} and planar FET) with a single parameter set. In both TCAD setups, drift-diffusion transport model was used. Band-to-band tunneling (BTBT) and trap-assisted-tunneling (TAT) were taken into account only for the 2D model. In **Fig. 13**, the transfer characteristics and *SS* that were obtained with the 3D TCAD simulation for the shortest L_G = 13 nm devices for three different W_{fin} are compared with experimental values. At low V_D at which electrostatics dominates the OFF-state behavior, the 3D TCAD model reproduces very well the experimental data. For higher V_D, a large discrepancy is observed. This indicates that *SS* degradation is not only due to short-channel effects (*i.e.* electrostatic control) but also due to carrier generation and recombination processes. The 2D TCAD model including BTBT and TAT effects can reproduce these phenomena. This is shown by a comparison of experimental and simulated transfer characteristics and *SS* that are shown in **Figs. 14a** and **14b** respectively, for the shortest L_G and W_{fin} device at different V_D. It appears that the SS_{sat} of this device is limited by BTBT current amplified by the formed parasitic bipolar transistor.

We have finally plotted a benchmark (**Fig. 15**) showing I_{ON} vs. L_G for CMOS-compatible InGaAs FETs that have been integrated on Si. Compared to previous demonstrations we achieve very high ON-current for an extremely scaled gate length of 13 nm.

IV. Conclusion

We have shown record-performance InGaAs-on-Insulator FinFET with L_G down to 13 nm that reaches I_{ON} of 249 µA/µm at fixed I_{OFF} = 100 nA/µm and V_D = 0.5 V. Investigation of transport physics with 3D and 2D TCAD simulations has enabled us to show that band-to-band-tunneling and trap-assisted-tunneling are dominant mechanisms limiting the I_{OFF} at the scaled gate length. Further improvements in electrostatic control and sub-threshold performance can be achieved by source-drain junction engineering and fin width reduction. This work demonstrates the feasibility of high-performance InGaAs devices on Si at gate lengths of target for sub-7 nm nodes.

Acknowledgment

The authors acknowledge strong support from the BRNC OpTeam, MIND and NDS groups. Funding from European Union is acknowledged: FP7 program grant agreement nos. 619325 (COMPOSE3), 619326 (III-V-MOS) and 628523 (FACIT) and Horizon 2020 grant agreement no. 688784 (INSIGHT).

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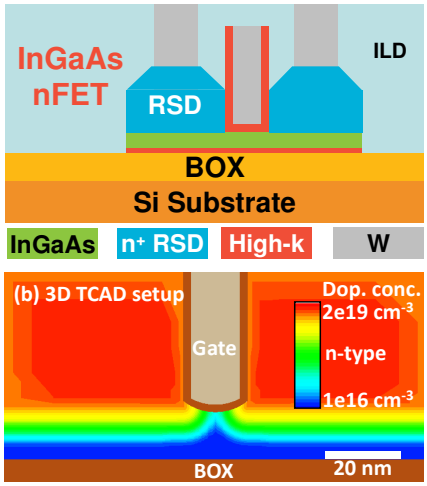


Fig. 1. (a) Cross-sectional schematic of the self-aligned spacer-free replacement metal gate InGaAs-on-Insulator devices (b) 3D TCAD setup shown across the gate with doping profile.

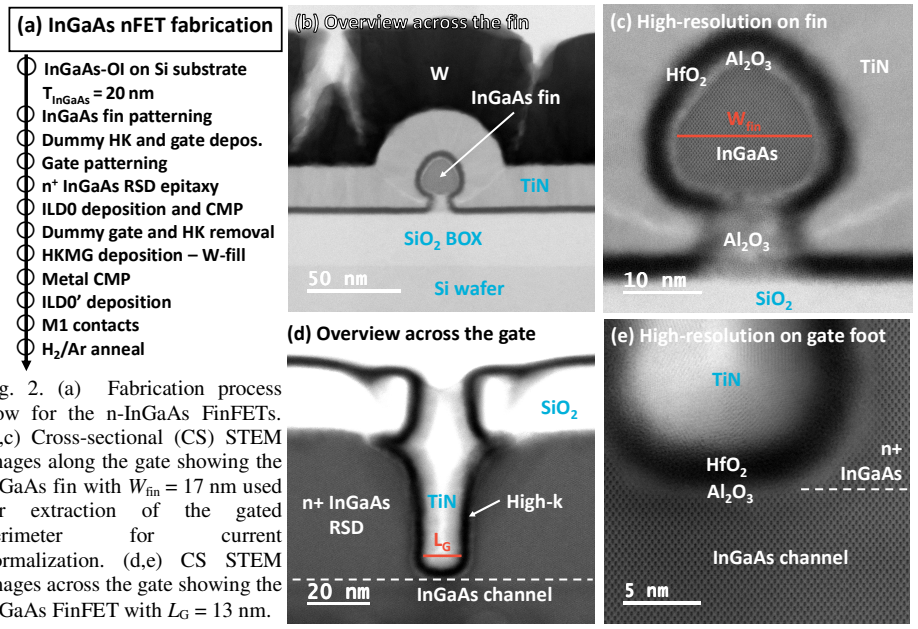


Fig. 2. (a) Fabrication process flow for the n-InGaAs FinFETs. (b,c) Cross-sectional (CS) STEM images along the gate showing the InGaAs fin with W_{fin} = 17 nm used for extraction of the gated perimeter for current normalization. (d,e) CS STEM images across the gate showing the InGaAs FinFET with L_G = 13 nm.

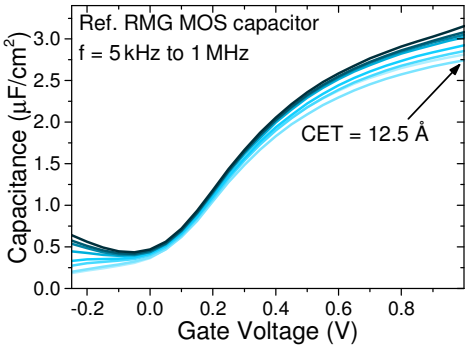


Fig. 3. C-V measurement of a reference MOS-Capacitor showing a capacitive equivalent thickness (CET) of 1.25 nm with low frequency dispersion in the V_G range -0.1 V to 0.1 V.

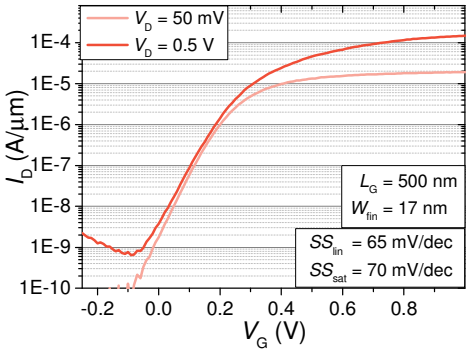


Fig. 4. Transfer characteristic of L_G = 500 nm and W_{fin} = 17 nm n-FinFET showing steep subthreshold swing in the V_G range -0.1 V to 0.1 V.

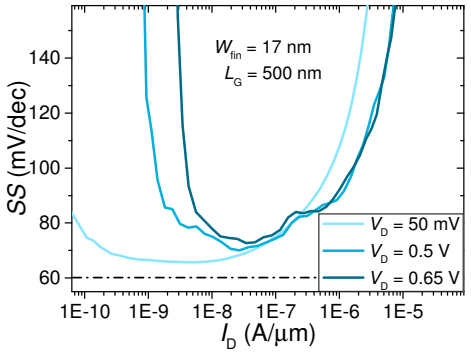


Fig. 5. Subthreshold swing (*SS*) versus drain current (I_D) of L_G = 500 nm and W_{fin} = 17 nm n-FinFET showing steep subthreshold swing below 67 mV/dec over two orders of magnitude of drain current.

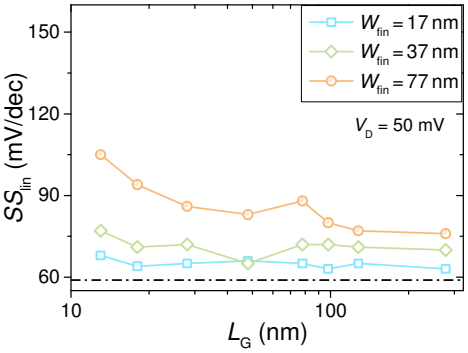


Fig. 6. Minimal linear subthreshold swing (*SS*) vs. gate length at V_D = 50 mV for devices with different fin widths. Linear subthreshold swing below 70 mV/dec is obtained for the shortest L_G devices and smallest fin width.

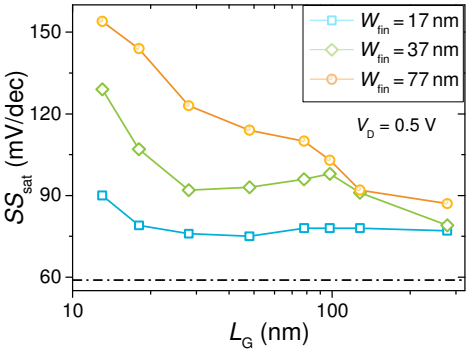


Fig. 7. Minimal saturation subthreshold swing (*SS*) vs. gate length at V_D = 0.5 V for devices with different fin widths. Saturation *SS* below 90 mV/dec is observed for the shortest L_G devices and smallest fin width.

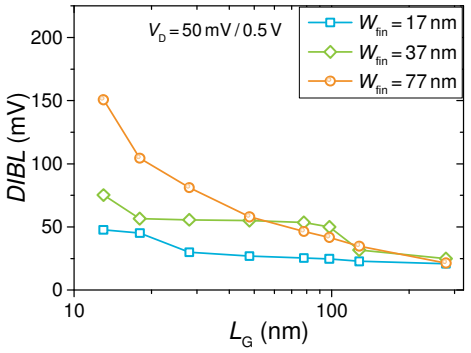


Fig. 8. Drain-induced barrier lowering (*DIBL*) vs. gate length for different fin widths. *DIBL* decreases with smaller fin widths. For the smallest fin width, *DIBL* values below 50 mV even for the shortest L_G devices are observed.

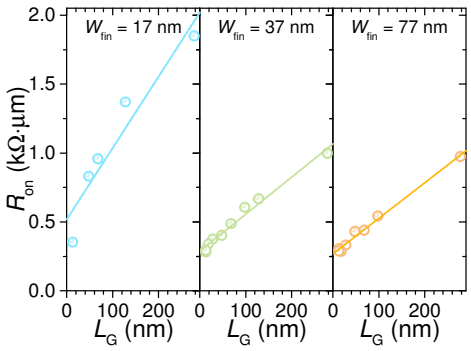


Fig. 9. ON-resistance vs. gate length for devices with small and larger fin widths. Higher access and channel resistance is observed for the smallest fin width.

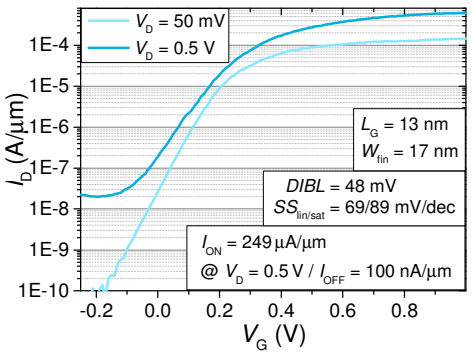


Fig. 10. Transfer characteristic of L_g = 13 nm and W_{fin} = 17 nm n-FinFET showing record-high ON-current (I_{ON}) of 249 µA/µm at I_{OFF} = 100 nA/µm and V_D = 0.5 V.

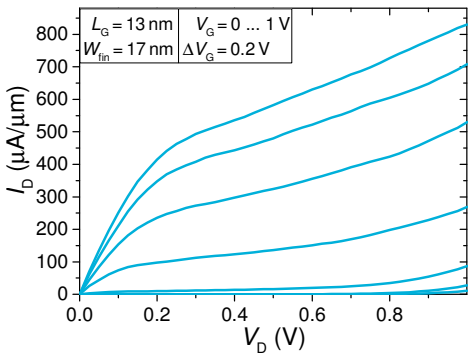


Fig. 11. Output characteristics of the short gate length, small fin width device. Only moderate short-channel effects are observed. R_{on} is extracted to be 355 Ω·µm.

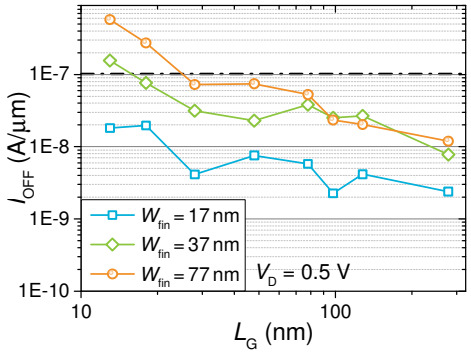


Fig. 12. OFF-current vs. gate length for devices with different fin widths. For short-channel devices, the small fin width is necessary to meet the I_{OFF} criterion of 100 nA/µm. The high OFF-current levels are limited by degraded *SS* that cannot be explained only by short-channel effects.

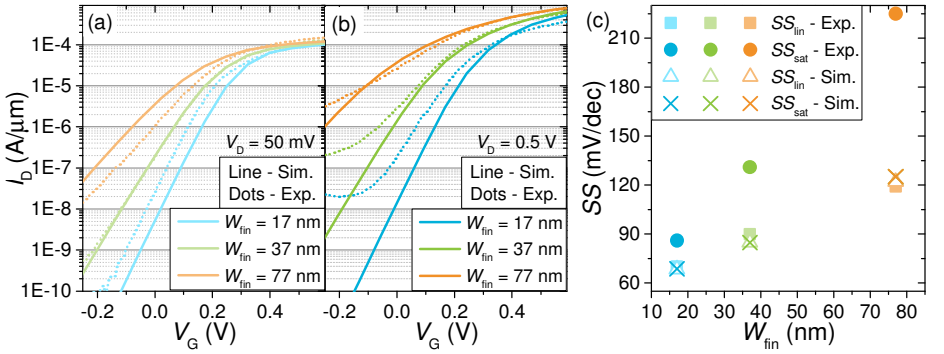
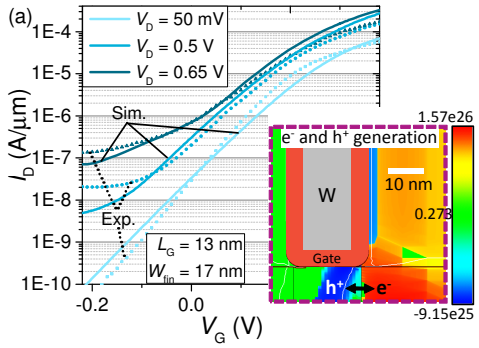


Fig. 13. Comparison of experimental (dots) and full-3D simulated (lines) transfer characteristics of L_G = 13 nm devices for different fin widths in (a) linear and (b) saturation regime. The 3D TCAD simulation does not account for BTBT and TAT effects. (c) Summary of experimental and 3D TCAD simulated *SS* versus W_{fin} for devices with L_G = 13 nm. It shows an exact matching of linear *SS* (V_D = 50 mV) where electrostatics dominate. The large discrepancy between experimental and simulated *SS* in saturation (V_D = 0.5 V) cannot be explained by short-channel effects alone.



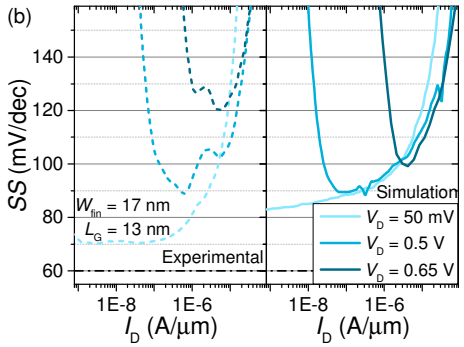


Fig. 14. (a) Comparison of experimental (dots) and simulated (lines) transfer characteristics of the FinFET of Figs. 10 and 11 for different drain voltages. A simplified 2D nanowire TCAD model is used that takes into account carrier generation/recombination effects such as band-to-band tunneling (BTBT) and trap-assisted tunneling (TAT). The color-mapped generation rate in the inset illustrates that the main reason for increased OFF-state current at higher bias due to BTBT. (b) Comparison of experimental (dots) and 2D nanowire TCAD simulated (lines) *SS* versus drain current of the FinFET of Fig. 10 for different drain voltages yielding an excellent agreement.

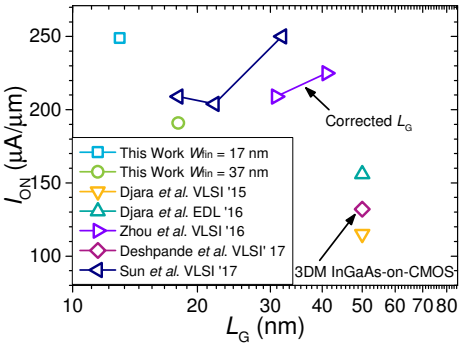


Fig. 15. I_{ON} vs. L_G Benchmark for CMOS-compatible InGaAs FETs integrated on a Si platform. I_{ON} is extracted at V_D = 0.5 V and fixed I_{OFF} of 100 nA/µm. We are able to demonstrate, for the first time, boosted I_{ON} at sub-20 nm gate length. (To equalize L_G extraction, we subtracted 15 nm of the length reported in Zhou *et al.* [3])