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Research Report

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Hybrid InGaAs/SiGe CMOS Circuits with 2D and 3D Monolithic Integration

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***Abstract*—Advanced CMOS nodes target high-performance at lower supply voltage. High-mobility III-V channel materials have the potential to meet this target. Although III-V materials such as InGaAs are beneficial for nFET channels, SiGe (or Ge) provides better hole mobility and is more suited for pFET channels. Therefore, a InGaAs/SiGe hybrid CMOS technology is being pursued for scaled nodes. There are significant challenges to co-integrate these two materials in a scalable process. In this regard, here, we present some of our recent work in InGaAs/SiGe CMOS integration through a novel direct epitaxy process for co-planar 2D integration. We also show are efforts in 3D monolithic integration of InGaAs-on-SiGe for CMOS and beyond.**

I. Introduction

High-mobility materials such as InGaAs and SiGe alloys are being considered as potential options for channel materials in leading-edge CMOS technology nodes. SiGe is already being introduced as pFET channel material at 7 nm node. InGaAs based alloys have become leading choice in the research for nFET channel material for sub-7 nm node and is a candidate with potential for replacing strained Silicon in future low power-high performance logic technology [1]. Therefore, a CMOS technology with hybrid channel materials, namely, SiGe (or Ge) for pFETs and InGaAs for nFETs is being envisaged. So it is imperative to develop a robust and scalable CMOS integration scheme starting from III-V material integration on Silicon platform to dense circuits. Due to largely different process conditions, especially with regards to the thermal budget, developing a CMOS process becomes very challenging. A reliable CMOS integration scheme can only be developed with a proper choice of material integration methods (for III-V on Silicon). Although direct wafer bonding (DWB) based integration led to the first demonstrations of InGaAs/SiGe CMOS [2], it faces challenges in terms of topography. Through a novel direct epitaxy method, we show integration approaches for a conventional co-planar 2D CMOS [3]. Utilizing standard front-end-of-line processes, we demonstrate a dense 2D integration of InGaAs and SiGe channels on Si substrate. Scaled gate length InGaAs nFETs and SiGe pFETs along with inverters and dense SRAM cells with finFET devices are demonstrated.

Besides, 3D Monolithic (3DM) integration is attracting much attention owing to density scaling benefits and the potential to stack independently optimized multifunctional layers at transistor level [4]. However, due to sequential processing of transistor layers, the thermal budget of top transistor layer can be detrimental to the bottom layer transistors. This puts a limit on the top layer thermal budget, which is typically around 600°C when the bottom layer has Si/SiGe transistors. As a typical high performance Si/SiGe MOSFET process requires high thermal budget, an alternate low temperature top layer Si/SiGe process development is necessary for a 3DM scheme and thus presents challenges to obtain high-performance MOSFETs. On the other hand, the InGaAs MOSFET processing thermal budget is significantly lower and makes it naturally suited to be used as the top layer channel material. Moreover, the higher channel mobility could enables high performance at even lower voltages. In this context we demonstrate, 3D monolithic integration of InGaAs nFETs on SiGe-on-Insulator pFETs with state-of-the-art device integration on both levels [5]. 3D inverters down to short gate lengths of L_g~30 nm are demonstrated. Going beyond CMOS circuits, 3DM integration has also been exploited to demonstrate InGaAs RF devices over SiGe pFETs, paving the way for 'functional scaling'.

II. Co-planar 2D CMOS Integration

A schematic of InGaAs/SiGe co-planar 2D CMOS integration by direct epitaxy is shown in Fig. 1. This method offers truly co-planar integration along with '-on-Insulator' device architecture which could enable Fully-depleted Silicon-on-Insulator (FDSOI) like technology. It allows a dense co-integration of InGaAs nFET with SiGe pFETs and is scalable to large wafer sizes.

Process flow of the InGaAs/SiGe CMOS integration by direct epitaxy as demonstrated in ref [3] is shown in Fig. 2. Top

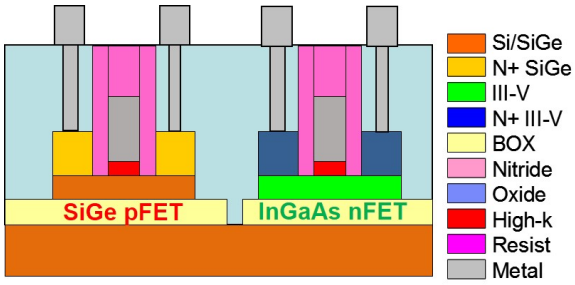

Fig. 1. Schematic showing InGaAs/SiGe co-planar 2D CMOS integration.

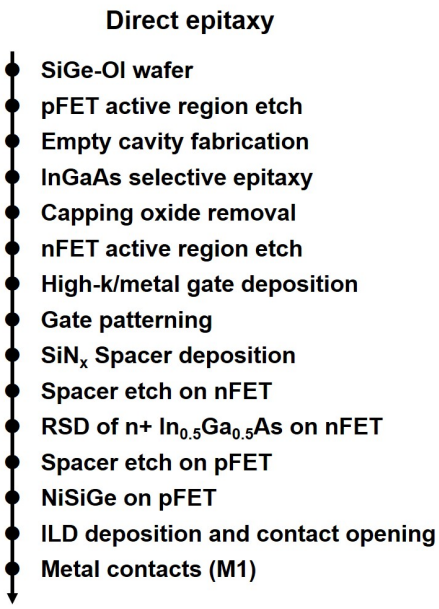

Fig. 2. Process flow of InGaAs/SiGe co-planar 2D CMOS integration by direct epitaxy.

view SEM images of at various steps of the process flow are shown in Fig. 3. The process starts with a SiGe-OI wafer and firstly, pFET active regions are formed. It is then followed by series are process steps (described in detail in ref [6]) to form SiO2 cavities which have an access to Si substrate through a seed window(Fig. 3b). This location acts as a crystalline seed to start the direct growth of III-V materials as demonstrated in ref [7] [6]. The empty SiO2 cavities are filled by InGaAs epitaxy step (Fig. 3c). Defect filtering in this growth step occurs with a change in direction of growth from vertical to lateral. The thickness of so grown InGaAs layer is set by the height of the SiO2 cavity. A 30 nm thick InGaAs (In content = 70 %) layer was grown in ref [3]. After InGaAs growth, the encapsulating SiO2 which formed the cavities is removed and InGaAs channel is exposed(Fig. 3c). Thus co-planar InGaAs and SiGe active regions are obtained. Now, standard CMOS front-end-of-line processes can be carried out to form InGaAs nFETs and SiGe pFETs. In ref [3], a gate-first flow was carried out. A common high-k dielectric and metal gate stack was deposited and gates were patterned on both n- and p-FET regions. Then spacer layer was deposited. Spacers were first formed only on nFET regions by blocking pFET region during dry etching. Thereafter, highly n-doped InGaAs raised source/drain (RSD) was grown. This was followed by spacer formation on pFET regions and Ni-SiGe alloy formation to form S/D region for SiGe pFETs. Finally encapsulating oxide was deposited, contact holes opened and metallization was carried out to form contact pads as well as circuit connections. Both planar as well as finFETs were fabricated for InGaAs and SiGe devices. A dense integration of InGaAs and SiGe active areas with 25 nm was demonstrated for the first time on Silicon platform. Although, simplified process was used for pFET S/D formation, it can readily be extended to start-of-the-art device integration with RSD. Large SRAM arrays with dense cell size were fabricated.

Well behaved device characteristics featuring n- and p-FET gate lengths down to L_g=30 nm were demonstrated. For the first time, InGaAs/SiGe SRAM cells were demonstrated down to 0.4 um^2. The electrical characteristics of an inverter, a relaxed cell-size SRAM, and a dense SRAM are shown in Fig. 4. This shows the scalability and robustness of the CMOS integration scheme.

III. 3D Monolithic CMOS Integration

The process flow of the 3DM integration demonstrated ref [5] is shown in Fig. 5. Since SiGe pFET have high thermal budget process, firstly, the bottom layer SiGe-OI fin pFETs are fabricated. This was done with a gate-first (GF) process as described in [8], [9]. The top layer nFET fabrication is carried out after the silicidation step of SiGe-OI finFET process. It begins with InGaAs layer transfer on top of fabricated pFETs. Firstly, the inter-layer oxide is deposited and chemical-mechanical-polish (CMP) planarization is carried out. The

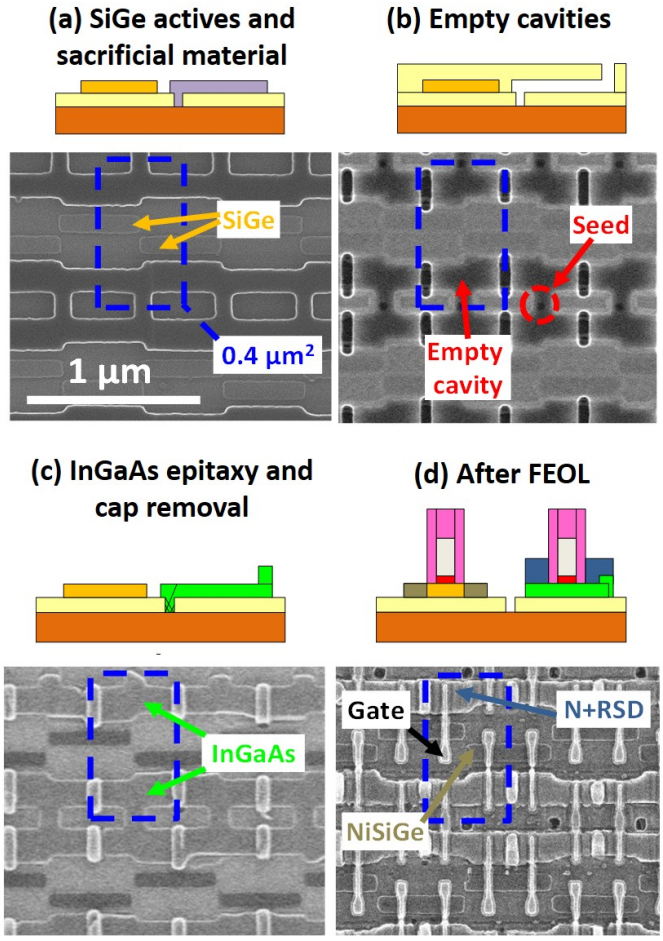

Fig. 3. Top view SEM images of at various steps of the process flow of the InGaAs/SiGe co-planar 2D CMOS integration.

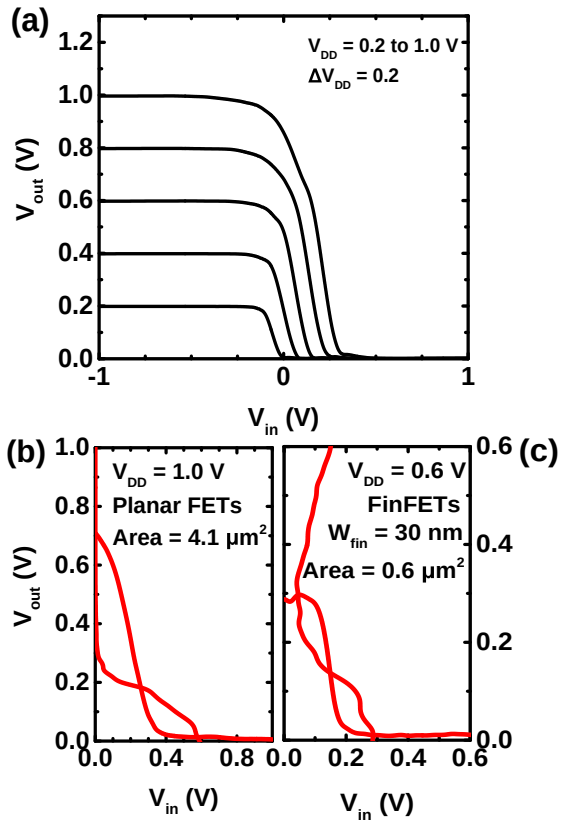

Fig. 4. (a) Voltage transfer characteristics a InGaAs/SiGe inverter. (b),(c) SRAM 'butterfly' characteristics.

InGaAs layer is transferred on to this oxide with direct wafer bonding from 2 inch InP donor wafers. InGaAs nFET fabrication is now performed with the replacement-metal-gate (RMG) process described in [10]. This involves patterning the active transistor regions followed by a dummy gate stack deposition. After patterning the dummy gate, spacers are formed on either side similar to the bottom pFET process. Then comes the critical step of selfaligned in-situ doped InGaAs epitaxy to form RSD regions. This step has relatively high thermal budget and therefore, has been optimized to minimize the process temperature while obtaining high doping in the layer as described in [5]. RMG process steps follow thereafter. An oxide layer is first deposited and planarized to expose the top of dummy gate. Then the dummy gate stack is selectively etched out. An optimized high-k/metal gate stack is deposited followed by metal CMP. Finally, oxide encapsulation is deposited and contact holes are opened to both top and bottom layers. Metallization is completed to create contact pads for both layers. The schematic of the so completed 3D monolithic stack is shown in Fig. 6.

Figure 7 shows the DC Id - Vg characteristics of top layer InGaAs nFET with Lg = 70 nm with a competitive DC performance after the 3DM fabrication. Figure 8 shows bottom SiGe-OI pFET Id-Vg after top nFET fabrication with excellent

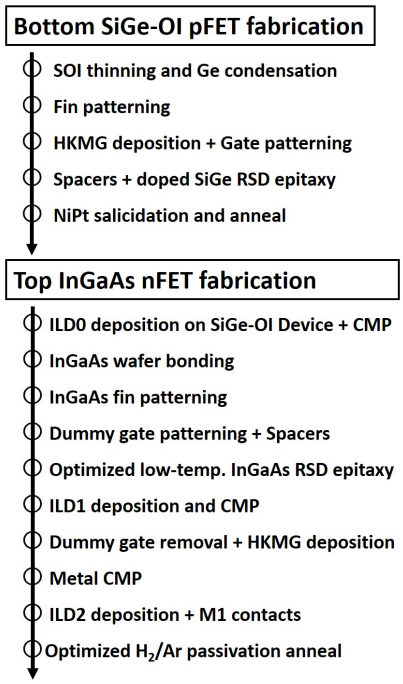

Fig. 5. Schematic showing InGaAs/SiGe 3D monolithic CMOS integration.

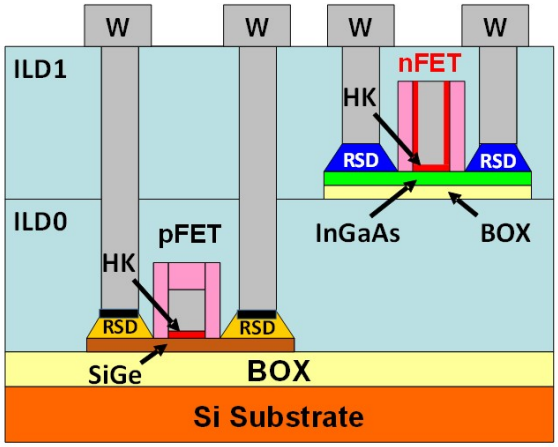

Fig. 6. Schematic showing InGaAs/SiGe 3D monolithic CMOS integration.

electrostatic integrity. Compared to the characteristics of the device before top nFET fabrication [5], the electrostatics of the device is seen to have negligible impact, demonstrating the robustness of the process. Thus an optimized performance on both, top-nFET and bottom-pFET layers can be achieved with this 3DM process.

Figure 9 shows the the voltage transfer characteristics (VTC) of scaled 3D inverters with nFET Lg = 80 nm (with pFET Lg 30 nm) and Lg 30 nm (for both nFET and pFET). Well-behaved transitions are obtained down to VDD = 0.25 V. Therefore the integration scheme shows the potential pathway towards an optimized low-voltage CMOS with with InGaAs-on-SiGe 3DM technology.

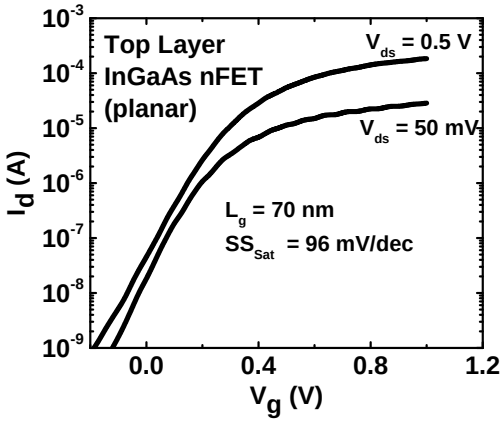

Fig. 7. Id-Vg characteristics of top layer InGaAs nFET.

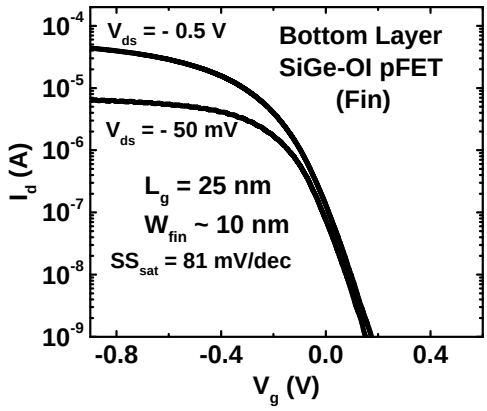

Fig. 8. Id-Vg characteristics of bottom layer SiGe-OI pFET.

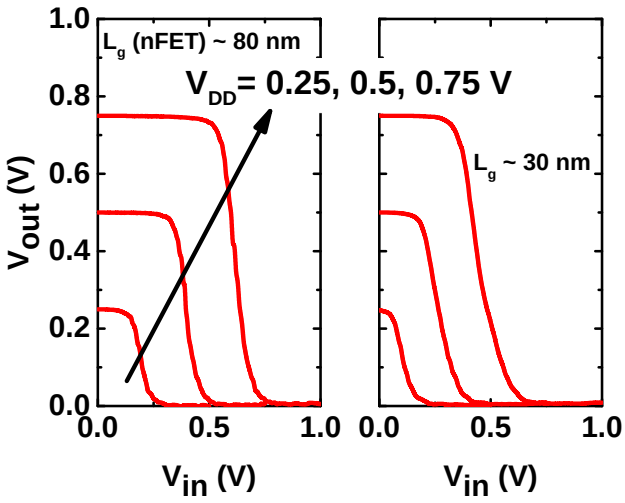

Fig. 9. Voltage transfer characteristics of InGaAs/SiGe 3D inverter.

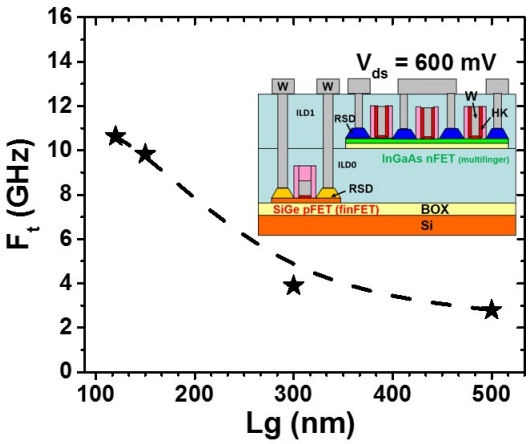

Fig. 10. Cut-off frequency for various gate lengths for top layer InGaAs RFFETs. Dotted line is guide to eye. Inset shows schematic of multifinger-gate structure of RFFETs.

Besides CMOS demonstration, the top layer InGaAs nFETs were also characterized for RF applications [11]. A multi-finger gate structure was used for such devices as shown in the inset of Fig. 10. Fig. 10 shows cut-off frequency vs. gate length plot for the InGaAs RF-FETs. Promising first results open up the opportunity for RF-over-CMOS circuits in the 3DM integration.

IV. Conclusion

A novel direct epitaxy based co-planar 2D InGaAs/SiGe CMOS integration scheme is demonstrated with potential for scalability to sub-7 nm node technology. Functional CMOS circuits, including dense SRAM cell, obtained in through the integration are testimony to the advantages of the scheme. Besides 2D integration, InGaAs-on-Si(Ge) 3D Monolithic integration scheme is demonstrated that allows low voltage high-performance CMOS circuits as well RF-over-CMOS circuits. Owing to inherent benefits of low thermal budget and high mobility InGaAs as top layer enables optimized performance at both layers. Thus building blocks for a high performance, multi-functional 3D Monolithic technology were demonstrated.

Acknowledgment

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