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Research Report

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First RF Characterization of InGaAs Replacement Metal Gate (RMG) nFETs on SiGe-OI FinFETs Fabricated by 3D Monolithic Integration

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Abstract— **We report the first RF characterization of short-channel replacement metal gate (RMG) InGaAs-OI nFETs built in a 3D Monolithic (3DM) CMOS process. This process features RMG InGaAs-OI nFET top layer and SiGe-OI fin pFET bottom layer. We demonstrate state-of-the-art device integration on both levels. The bottom layer SiGe-OI pFETs are fabricated with a Gate-First (GF) process with fins scaled down to ~15 nm width and featuring epitaxial raised source drain (RSD) and silicide. The top layer InGaAs nFETs are fabricated with a RMG process featuring a self-aligned epitaxial raised source drain (RSD). We show that the 3D monolithic integration scheme does not degrade the performance of the bottom SiGe-OI pFETs owing to an optimized thermal budget for the top InGaAs nFETs. From the RF characterizations performed (post-3D monolithic process) on multifinger-gate InGaAs-OI nFETs, we extract a cut-off frequency (F_t) of 16.4 GHz at a gate-length (L_g) of 120 nm. Measurements on various gate lengths shows increasing cut-off frequency with decreasing gate-length.**

Keywords—3D Monolithic; InGaAs; RMG; High-frequency; FinFET

I. INTRODUCTION

3D Monolithic (3DM) integration is attracting much attention owing to density scaling benefits and the potential to stack independently optimized multifunctional layers at transistor level [1]. However, due to the inherently high thermal budget of Si MOSFET process, Si(Ge)-on-Si 3DM integration scheme faces major challenges in top layer optimization without degrading bottom layer performance. This necessitates development of low temperature top layer Si/SiGe process which presents further challenges to obtaining high-performance MOSFETs on top layer. As the InGaAs MOSFET processing thermal budget is significantly lower, it is well-suited to be used as the top layer channel material. Moreover, InGaAs also has higher mobility which enables high performance at lower voltages and is also a widely used material for high-frequency devices. This aspect is of great interest as it can enable RF devices required for high-frequency analog or mixed signal circuits integrated on top of Si/SiGe MOSFETs and can provide transistor level granularity. As a step towards such a multi-functional 3D monolithic integration, here, we show RF characteristics of InGaAs nFETs fabricated with RMG process on top of SiGe-OI finFETs. We perform RF characterization of InGaAs-OI nFETs of various gate-lengths designed with optimized 'multi-finger gate' layout to enable efficient characterization. We demonstrate a cut-off frequency of 16.4 GHz for gate length (L_g) of 120 nm. Also, cut-off frequency is shown to increase with decreasing gate-lengths. We also demonstrate that the impact of 3DM integration on the bottom pFET performance is negligible, despite the top nFET RMG process featuring a self-aligned raised source drain epitaxy (with relatively high thermal budget). Thus we demonstrate the robustness of the InGaAs-on-SiGe 3DM integration.

II. DEVICE FABRICATION

The 3DM process flow is shown in Fig. 1. Firstly, bottom layer SiGe-OI fin pFETs are fabricated with a gate-first (GF) process as in [2, 3]. The process begins with thinning of silicon layer of an 8 inch SOI wafer followed by Ge condensation to obtain SiGe-OI layer (with ~25% Ge content). Then active pFET areas are patterned and gate stack (with high-k dielectric and metal gate) is deposited. This is then followed by gate patterning and spacer deposition. After forming the spacers with anisotropic dry etching, in-situ doped SiGe epitaxy is carried out to form self-aligned raised source drain (RSD) regions. Then NiPt salicidation (self-aligned

Fig. 1. InGaAs-on-SiGe 3D Monolithic integration process flow.

silicidation) is performed to obtain low contact resistivity on the pFETs. This silicide sets the thermal budget limit for the top nFET processing. The top layer nFET fabrication starts after this silicidation step of SiGe-OI finFET process. It begins with InGaAs layer transfer on top of processed pFETs. Firstly, the inter-layer oxide is deposited and chemical-mechanical-polish (CMP) planarization is carried out. The InGaAs layer is transferred on to this oxide with direct wafer bonding from 2 inch InP donor wafers [4]. InGaAs nFET fabrication is now performed with the RMG process described in [5]. This involves patterning the active transistor regions followed by a dummy gate stack deposition. After patterning the dummy gate, spacers are formed on either side similar to the bottom pFET process. Then comes the critical step of self-aligned in-situ doped InGaAs epitaxy to form RSD regions. This step has relatively high thermal budget and therefore, has been optimized to minimize the process temperature while obtaining high doping in the layer as described in [6]. RMG process steps follow thereafter. An oxide layer is first deposited and planarized to expose the top of dummy gate. Then the dummy gate stack is selectively etched out. An optimized high-k/metal gate stack [5] is deposited followed by metal CMP. Finally, oxide encapsulation is deposited and contact holes are opened to both top and bottom layers. Metallization is completed to create contact pads for both layers.

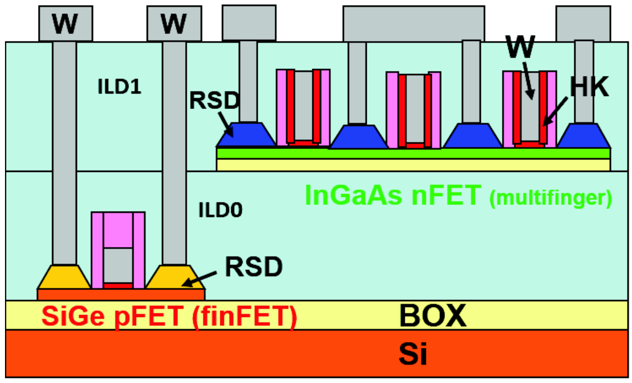

Fig. 2. Schematic of the InGaAs-on-SiGe 3DM stack showing multi-finger gate nFETs on top layer.

The schematic of the so completed 3D monolithic stack is shown in Fig. 2.

The layout of InGaAs nFETs on top layer used for RF characterization features multi-finger gate structures as shown in Fig. 2. This allows lowering the gate-resistance owing to multiple parallel gates. Also, the layout of devices characterized in this work has dense features with gate-to-contact spacing of 100 nm.

III. Electrical Characterization

Fig. 3 shows the DC I_d-V_g characteristics of a top InGaAs planar nFET with L_g = 120 nm. This device features 10 finger gates in parallel and is so designed to enable RF characterization with coplanar waveguide pad structures. DC characteristics show competitive electrostatic control with drain-induced-barrier-lowering (DIBL) of 100 mV/V and SS^{sat} = 100 mV/dec due a scaled high-k gate stack with CET of 1.6 nm and low D_{it} [5]. Fig. 4 shows the I_d-V_d characteristics for the same device. Fig. 5

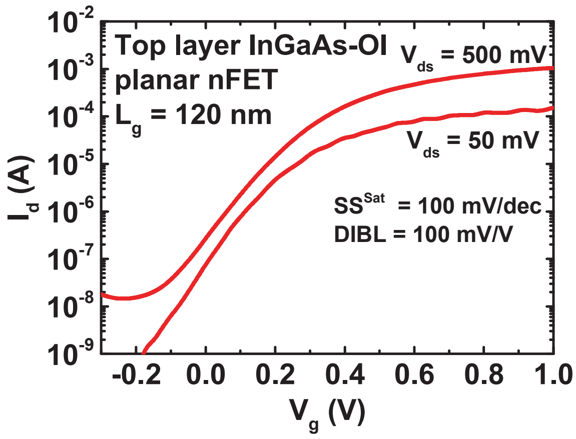

Fig. 3. DC I_d-V_g characteristics of top layer InGaAs-OI planar nFET with L_g = 120 nm.

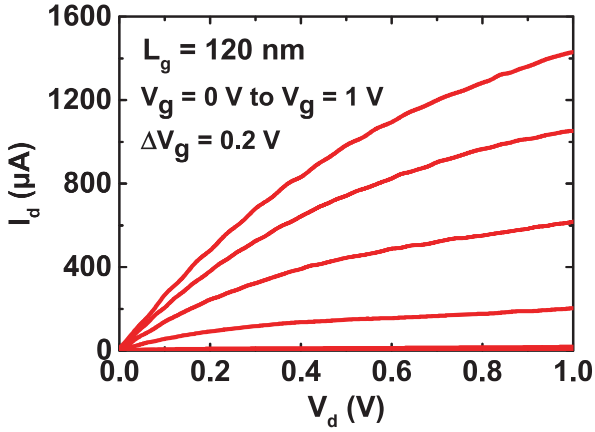

Fig. 4. DC I_d-V_d characteristics of InGaAs-OI top layer planar nFET with L_g = 120 nm.

shows the I_d-V_g characteristics of the bottom layer SiGe-OI finFET with L_g = 36 nm and fin width ~ 15 nm, before (black-dash) and after (blue-solid) top nFET fabrication. Owing to the lower thermal budget of the top layer InGaAs process, very minimal impact is observed on the bottom pFET, even for a scaled gate length. Nearly the same drain current (I_d) is maintained at both linear and saturation regime in the pFET indicating no degradation of the bottom silicide. RF characterization of the top nFET is performed on the devices with 10 parallel finger gates, each with a width of 2 µm (= total width of 20 µm), and having a ground-signal-ground (GSG) pad configuration. LRRM calibration with a vector-network-analyzer (VNA) is first carried on a standard reference calibration substrate, to move the reference plane to probe tips. Dedicated on-chip 'open' pad structures are used to de-embed the device. S-parameters are measured from 45 MHz to 40 GHz. From the measured S-parameters, current gain (|h21|) is calculated and shown

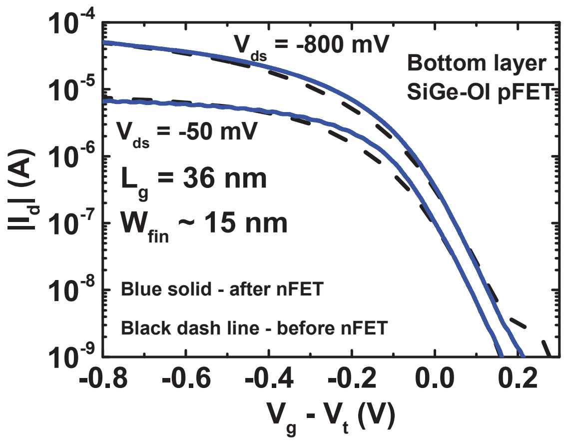

Fig. 5. Comparison of I_d-V_g characteristics of bottom layer SiGe-OI pFET before and after top nFET fabrication.

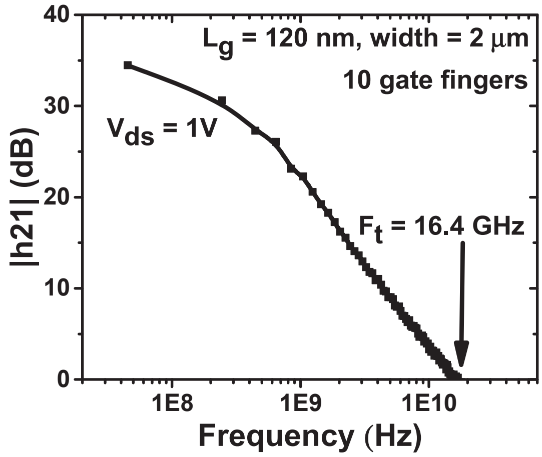

Fig. 6. Measured current gain (|h21|) vs. frequency for a InGaAs nFET (top layer) with L_g = 120 nm and 10 parallel gate fingers. Cut-off frequency (F_t) of 16.4 GHz is obtained for V_{ds} = 1V.

in Fig. 6, for a device with L_g = 120 nm. A cut-off frequency (F_t) of 16.4 GHz is obtained for V_{ds} = 1V. Lower F_t value is probably due to higher access resistance in the device and high parasitic capacitance between the gate-source/drain contacts due to short separation of 100 nm. Cut-off frequency vs. L_g plotted in Fig.7 shows an increase in cut-off frequencies with decreasing L_g. Scaling down L_g further, along with improving access resistance and a relaxed gate-contact spacing could provide a way to increase the cut-off frequency.

IV. Conclusion

We show, for the first time, RF characterization of InGaAs RMG nFETs fabricated on top of SiGe-OI finFETs in 3D Monolithic integration. A cut-off

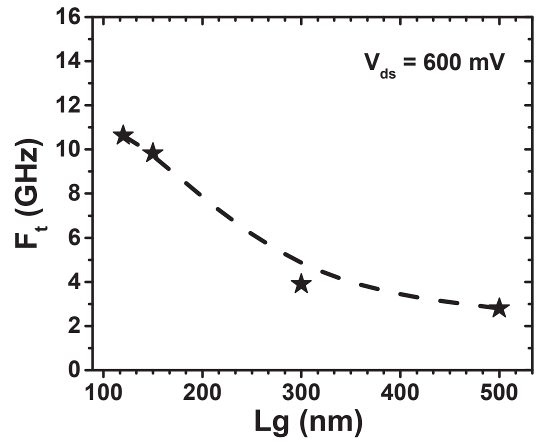

Fig. 7. Cut-off frequency vs. gate length (L_g) for top InGaAs nFETs for V_{ds} = 600 mV.

frequency of 16.4 GHz is obtained for L_g = 120 nm nFET with negligible impact on the bottom pFET performance. The InGaAs nFETs also feature a scaled gate stack and tight pitch design (gate-contact spacing = 100 nm). Thus we demonstrate the benefit of InGaAs-on-SiGe 3D monolithic integration, showing that independently optimized multi-functional layers can be fabricated exploiting the advantages of both device layers.

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