RZ 3961 (#ZUR1906-084) 06/26/2019
Electrical Engineering 2 pages

Research Report

First Demonstration of 3D SRAM Through 3D Monolithic Integration of InGaAs n-FinFETs on FDSOI Si CMOS with Inter-layer Contacts

V. Deshpande[1], H. Hahn[1], E. O'Connor[1], Y. Baumgartner[1], M. Sousa[1], D. Caimi[1], H. Boutry[2], J. Widiez[2], L. Brévard[2], C. Le Royer[2], M. Vinet[2], J. Fompeyrine[1] and L. Czornomaz[1]

[1] IBM Zurich Research Laboratory, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland

[2] CEA-Leti, MINATEC Campus, 17 rue des Martyrs, F38054, Cedex 9, France, Université Grenoble Alpes

This is the accepted version of the article published by IEEE: V. Deshpande, H. Hahn, E. O'Connor, Y. Baumgartner, M. Sousa, D. Caimi, H. Boutry, J. Widiez, L. Brévard, C. Le Royer, M. Vinet, J. Fompeyrine and L. Czornomaz, "First Demonstration of 3D SRAM Through 3D Monolithic Inte-gration of InGaAs n-FinFETs on FDSOI Si CMOS with Inter-layer Contacts," 2017 Symposium on VLSI Technology Digest of Technical Papers.
10.23919/VLSIT.2017.7998205

First Demonstration of 3D SRAM Through 3D Monolithic Integration of InGaAs n-FinFETs on FDSOI Si CMOS with Inter-layer Contacts

V. Deshpande[1], H. Hahn[1], E. O'Connor[1], Y. Baumgartner[1], M. Sousa[1], D. Caimi[1],
H. Boutry[2], J. Widiez[2], L. Brévard[2], C. Le Royer[2], M. Vinet[2], J. Fompeyrine[1] and L. Czornomaz[1]
(1) IBM Research GmbH Zürich Laboratory, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland;
(2) CEA-Leti, MINATEC Campus, 17 rue des Martyrs, F38054, Cedex 9, France, Université Grenoble Alpes;
Contact author:vee@zurich.ibm.com

Abstract We demonstrate, for the first time, the 3D Monolithic (3DM) integration of $In_{0.53}GaAs$ nFETs on FDSOI Si CMOS featuring short-channel Replacement Metal Gate (RMG) InGaAs n-FinFETs on the top layer and Gate-First Si CMOS on the bottom layer with TiN/W inter-layer contacts. State-of-the-art device integration is achieved with the top layer InGaAs utilizing raised source drain (RSD) and the bottom layer CMOS having Si RSD for nFETs, SiGe RSD for pFETs, implants, silicide and TiN/W plug contacts. The top layer InGaAs n-FinFETs are scaled down to L_g =25 nm and both the Si nFETs and pFETs in the bottom layer are scaled down to L_g ~15 nm. Finally, utilizing the inter-layer contacts, we demonstrate a densely integrated 3D 6T-SRAM circuit with InGaAs nFETs stacked on top of Si pFETs showing considerable area reduction with respect to a 2D layout.

Introduction High-mobility III-V materials such as InGaAs are being considered to replace strained Si in nFETs for future low power logic application [1-2] and a co-integrated hybrid CMOS technology with InGaAs nFETs and Si/SiGe alloy pFETs is being envisaged [3]. However, owing to largely different process thermal budgets, such a co-integration is very challenging in a 2D planar configuration. On the other hand, 3DM integration allows independent processing and optimization for each device layer while providing circuit density benefits [4, 5]. Recently, it has been demonstrated [6, 7] that InGaAs is very well suited as a top nFET layer on a bottom Si/SiGe layer with very minimal impact on the devices and without any trade-off for the process optimization of both layers. Here, we further increase the complexity and demonstrate a 'n-over-CMOS' 3DM integration of a RMG InGaAs n-FinFET layer on FDSOI Si CMOS with TiN/W inter-layer contacts. Exploiting these inter-layer contacts we show dense functional 3D 6T-SRAM circuits. These contacts could also enable local interconnects to further increase circuit density.

Device and circuit fabrication Fig. 1 shows a schematic of the 3DM 'n-over-CMOS' stack featuring a RMG InGaAs nFET layer on a FDSOI Si CMOS layer with TiN/W inter–layer contacts. The full fabrication flow of both layers is detailed in Fig. 2. No modification is made to the independently optimized flows of each layer. The fabrication flow of the bottom Si CMOS follows a typical FDSOI process [8]. The bottom layer CMOS fabrication utilizes a Gate-First process and includes a selective epitaxial RSD for both n- and pFETs (SiGe RSD), silicide and TiN/W inter-layer contacts. After this contact formation on the bottom Si CMOS, a thin inter-layer dielectric (ILD0') was deposited and CMP was performed. On this, a ~20 nm thick InGaAs layer was transferred with direct wafer bonding [9], a technique compatible with large-scale Si substrates [10, 11]. Next, a RMG process with high-k/metal gate and RSD [12] was carried out for the nFET fabrication. The cross-section TEM images of the 3DM stack are shown in Fig. 3(a-d), with an InGaAs nFET aligned on top of a Si pFET and inter-layer contacts (Fig. 3(a)). Fig. 3(b-c) show magnified TEM images of the InGaAs nFET and Si pFET with a scaled high-k (HK) layer and respective L_g of 22 nm and 13 nm. Fig. 3(d) shows a cross-section of the InGaAs fin with a fin width (W_{fin}) of 25 nm. A top view SEM image of a 3D stacked inverter (2D inverter indicated for comparison), with InGaAs nFET over Si pFET, is shown in Fig. 3(e). The bottom layer nFET and pFET contacts (for the 2D reference inverter) are visible.

Device and circuit results I_d-V_g curves of top layer InGaAs n-FinFETs with W_{fin} = 25 nm are shown in Fig. 4 for short-channel (L_g = 25 nm) and longer-channel (L_g = 50 nm). I_d-V_d curves for the corresponding devices are shown in Fig. 5. Fig. 6 and 7 respectively show I_d-V_g and I_d-V_d curves for the bottom layer n- and p-FinFETs for L_g = 30 nm and 60 nm. The SS_{lin} and SS_{sat} (@ $|V_d|$ = 0.5 V) vs. L_g roll-off for the top layer InGaAs n-FinFETs, the bottom layer Si n- and p-FinFETs are shown in Fig. 8. For the InGaAs n-FinFETs, SS_{lin} of ~70 mV/dec is maintained down to L_g = 25 nm. SS_{sat} (@V_d = 0.9 V) vs. L_g for Si n- and pFETs shows very minimal change after the 3DM process, indicating negligible impact of top nFET process. SEM images of a 3D 6T-SRAM at various stages of the fabrication are shown in Fig. 9. As seen, InGaAs nFETs are stacked over Si pFETs and inter-layer contacts are used to achieve smaller cell area compared to a 2D layout. The 3D 6T-SRAM demonstrated here consists of top layer planar InGaAs nFETs with L_g = 60 nm and bottom layer Si p-FinFETs with L_g = 30 nm and W_{fin} = 30 nm. Fig. 10 and 11, show respectively I_d-V_g of a planar InGaAs nFET and I_d-V_d characteristics of the InGaAs nFET and a Si p-FinFET, with similar L_g and width as for the devices used in the 3D 6T-SRAM circuit. CMOS functionality with similar pFET at bottom layer is shown through voltage transfer characteristics of a 2D inverter (Si n- and pFET, L_g = 30 nm, W_{fin} = 20 nm) in Fig. 12. Finally, the 'butterfly' curves (in hold state) for the inverters in the 3D SRAM are shown in Fig. 13, for various V_{dd}. Well-behaved butterfly curves that yield high static noise margin (SNM) values are obtained owing to good matching of the InGaAs nFET and the Si pFET device characteristics. Compared to previous reports [6, 13, 14], this is the first demonstration of a hybrid 3D 6T-SRAM utilizing 3DM integration of InGaAs nFETs over Si CMOS.

Conclusion We have demonstrated state-of-the-art hybrid 3DM 'n-over-CMOS' with top layer RMG InGaAs n-FinFETs and bottom layer FDSOI Si CMOS with inter-layer contacts. Competitive device performance is obtained on both layers. Utilizing 3D stacking of devices and interlayer contacts, we show functional 3D 6T-SRAM with a denser packing compared to a 2D layout. Thus, we demonstrate a robust 3D monolithic integration platform of high-mobility III-V materials with Si CMOS which opens doors for dense digital circuits as well as for functional integration of RF-over-Si CMOS.

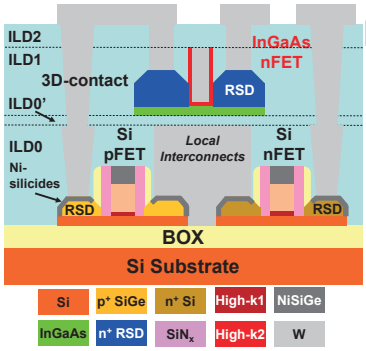

Fig. 1: Schematic showing 3D monolithic stack of RMG InGaAs nFET layer on FDSOI Si CMOS layer.

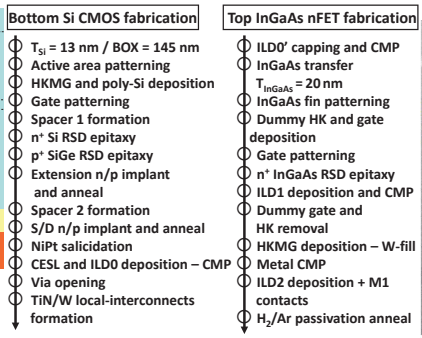

Fig. 2: Fabrication process flow for 3DM CMOS stack. Bottom CMOS has gate-first process and top layer has RMG process.

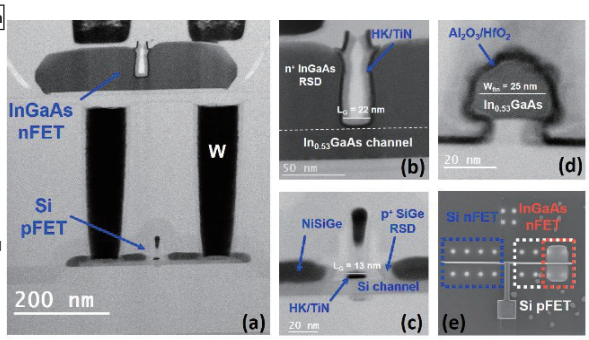

Fig. 3: 3DM InGaAs-on-Si layer stack. Cross-section TEM images show: (a) InGaAs nFET on SOI pFET along gate, zoom-in on (b) 22 nm L_g InGaAs nFET, (c) 13 nm L_g Si pFET, (d) 25 nm InGaAs fin and (e) top-view of 2D and 3D inverter.

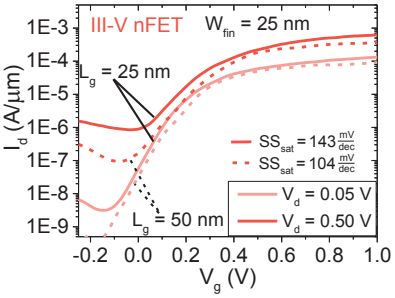

Fig. 4: I_d-V_g of L_g = 25 & 50 nm InGaAs nFET on the top layer with W_{fin} = 25 nm.

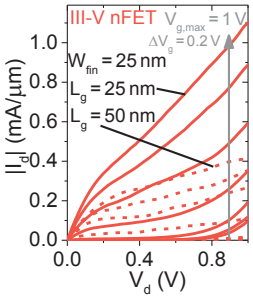

Fig. 5: I_d-V_d of the same devices as shown in Fig. 4.

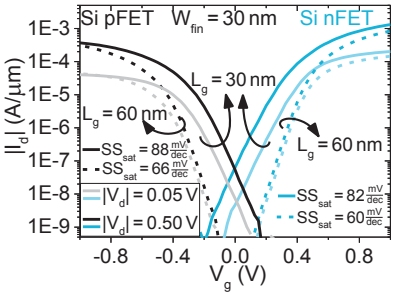

Fig. 6: I_d-V_g of L_g = 30 & 60 nm Si n- and pFET on the bottom layer with W_{fin} = 30 nm.

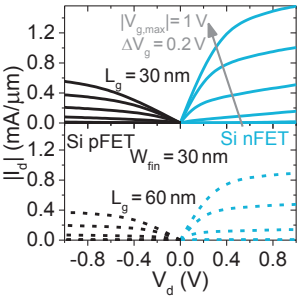

Fig. 7: I_d-V_d of the same devices as shown in Fig. 6.

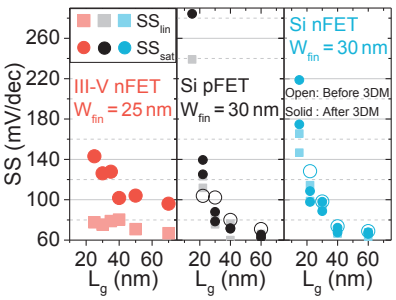

Fig. 8: SS (SS_{sat}@ $|V_d|$ = 0.5 V) vs. L_g plots for top layer InGaAs nFETs (W_{fin} = 25 nm) and bottom layer Si p- and nFETs (W_{fin} = 30 nm). SS_{sat} (open symbols) for Si FETs (n & p) before and after 3DM shows minimal change.

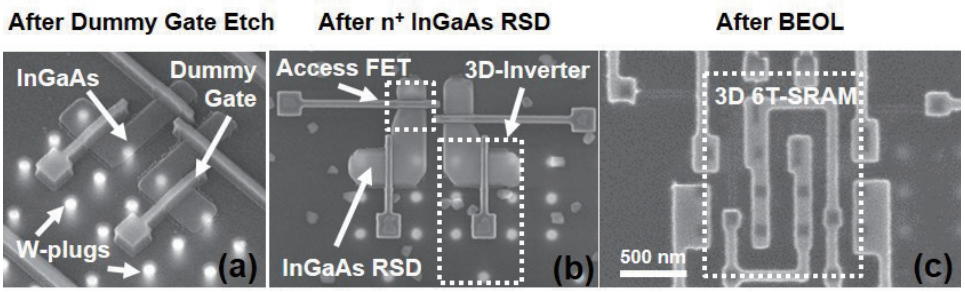

Fig. 9: Bird's-eye perspective (a) and top-view (b,c) SEM images of a 3D 6T-SRAM at different stages of the fabrication: (a) after dummy gate patterning, (b) after raised source/drain and (c) after completion of back-end-of-the-line up to the first metal layer.

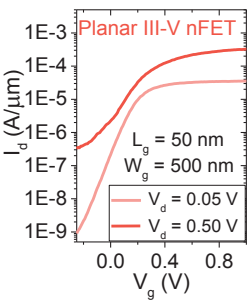

Fig. 10: I_d-V_g of L_g = 50 nm planar InGaAs nFET on the top layer with W_g = 500 nm.

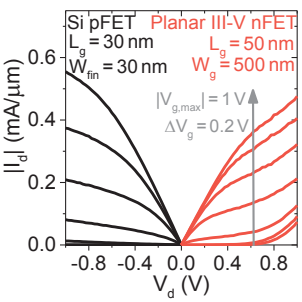

Fig. 11: I_d-V_d plots for devices similar to those used in the 3D 6T-SRAM.

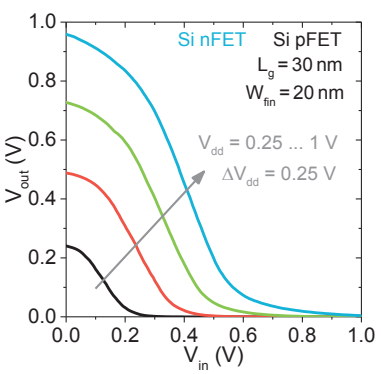

Fig. 12: Voltage transfer characteristics of a 2D inverter composed of bottom layer Si p- and n-FinFET with each having L_g = 30 nm and W_{fin} = 20 nm.

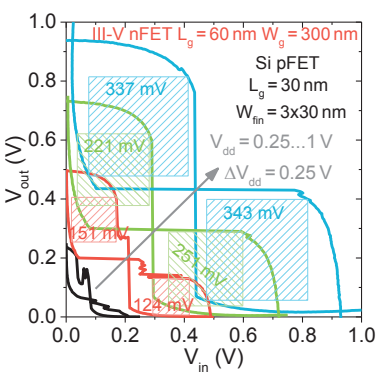

Fig. 13: Overlay of voltage transfer characteristics of the two inverters in the 3D 6T SRAM cell showing the 'butterfly' curves for different V_{dd}. SNM (indicated in the Fig.) increases with increasing V_{dd}.

Acknowledgments Funding from the EU is acknowledged (FP7-ICT-2013 COMPOSE^3 and IIIVMOS, H2020-ICT-2015 INSIGHT, PEOPLE-2013-IEF FACIT) as well as strong support from the BRNC OpTeam, MIND and NDS groups.

References [1] V. Djara *et al.*, EDL (2016), pp. 169 ; **[2]** C. Zota *et al.*, EDL (2016), pp. 1264 ; **[3]** L. Czornomaz *et al.,* VLSI Tech. Symp. (2016), pp. T-9-2-1 ; **[4]** Batude *et al.*, VLSI Tech. Symp. (2015), pp. T48. ; **[5]** L. Brunet *et al.,* VLSI Tech. Symp. (2016), pp. T-17-3 ; **[6]** V. Deshpande *et al.*, IEDM (2015), pp. 8.8.1 ; **[7]** E. Fitzgerald *et al.*, ECST (2016), 75, pp. 439 ; **[8]** S. Barraud *et al.,* VLSI Tech. Symp. (2013), pp. T-230 ; **[9]** L. Czornomaz *et al.,* IEDM (2012), pp. 23.4.1 ; **[10]** Daix *et al.,* APL Mater. (2014), pp. 086104 ; **[11]** Widiez *et al.,* JJAP (2016), pp. 04EB10 ; **[12]** V.Djara *et al.*, VLSI Tech. Symp. (2015)T-176.1 ; **[13]** T. Irisawa *et al.*, VLSI Tech. Symp. (2013) ; **[14]** T. Irisawa *et al.*, VLSI Tech. Symp. (2014)