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Investigations of UHV/CVD Deposition of SiGe Alloys on Silicon-on-Sapphire Substrates for Application to Device Fabrication Technology

P.M. Mooney, D.V. Singh, S.J. Koester, J.O. Chu, J.A. Ott
IBM Research Division
Thomas J. Watson Research Center
P. O. Box 218
Yorktown Heights, NY 10598

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

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P.M. Mooney, D.V. Singh, S.J. Koester, J.O. Chu, and J.A. Ott
IBM T.J. Watson Research Center
PO Box 218, Yorktown Heights, NY 10598

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Yield Issues Affecting Circuit Fabrication

The processing run for the frequency divider circuits completed in the previous quarter produced individual working p-MODFET devices. However several processing issues affecting device yield precluded the demonstration of a functioning frequency divider circuit. It is estimated that a device yield in excess of 95 % is required to get 10 % of the frequency divider circuits to work. Some of the key yield limiting steps in the process have been identified and are described below.

A) T-Gates: While the shape of the T-gates (Fig 1) is crucial to obtaining good device performance, it compromises their mechanical stability, especially as the gate length is scaled. This problem is further exacerbated (Fig. 2) by the necessity of doing an HF dip prior to the evaporation of Pt for the source/drain contacts. The undercutting of the T-Gates (Fig. 2) by HF poses a serious yield issue as well as an obstacle to scaling the gate length. We propose a novel spacer scheme in order to protect the neck of the T-Gate (Fig. 2). If this scheme works it will not only protect the T-gate during the HF dip, but will also provide an additional degree of mechanical support to the gates. Initial studies to test the feasibility of this idea are being carried out.

B) Source/Drain silicide formation: The Pt for the source and drain silicide regions are patterned using a lift off process. However the current lift-off process often results in lift-off flags or ears causing the source and gate to short. This limits the yield of the devices. We will have to develop a more sophisticated lift-off process in order to improve yields.

C) Lithography *issues* : The previous process mn had trouble aligning the metal contacts to the T-Gates. The poor alignment arises due to wafer slippage during contact with the mask. In the current run we plan on using a projection aligner as opposed to the contact aligner (Karl Suss) used previously. This should address the wafer slippage problem and result in improved alignment.

UHV/CVD growth of -MODFET Device Structures and Circuit Fabrication

A modified process run for fabricating divider circuits has been started this quarter. The p-MODFET layer structure was grown epitaxially on 4” bulk Si substrates and is similar to that described in earlier reports. The results of Hall effect measurements on one wafer (Govt61.10) are shown in Fig. 3. The room temperature hole mobility is 475 $cm^2/Vsec.$ So far we have completed the alignment mark and the mesa lithography steps in the device and circuit fabrication. A spacer scheme and an improved lift-off process for the source/drain silicide formation are being developed in parallel.

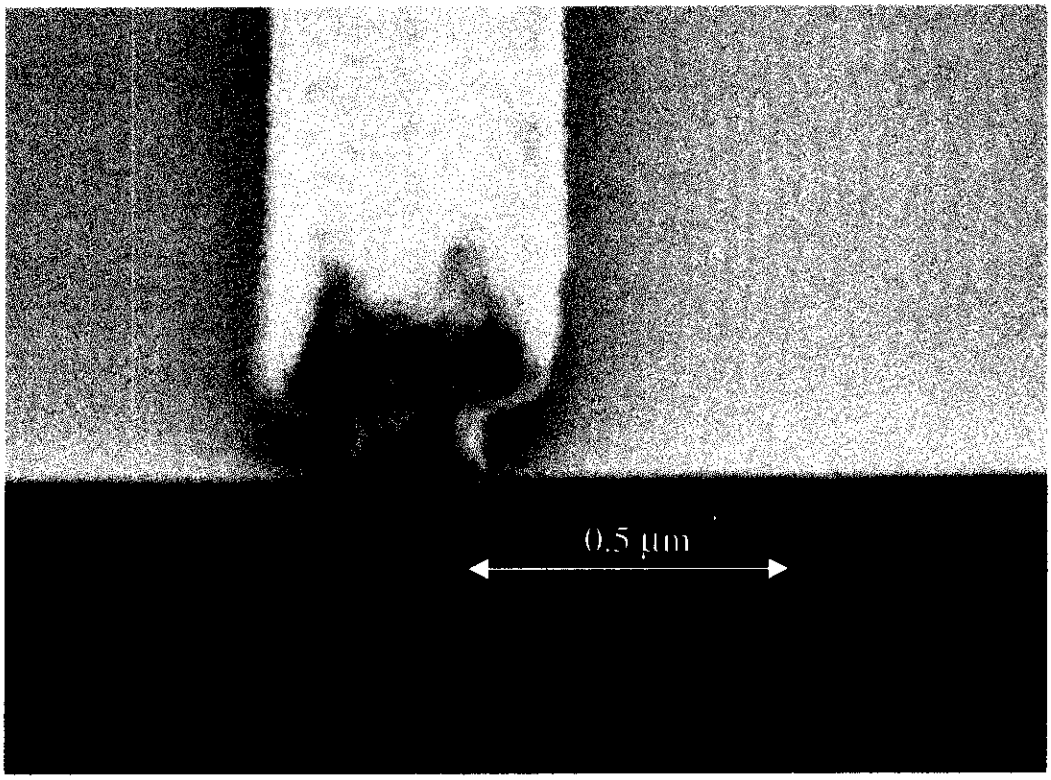

Figure 1. SEM of a T-Gate formed by lift-off.

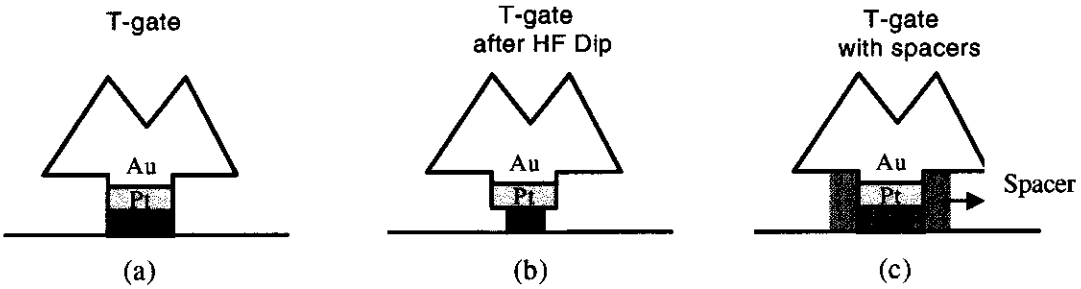

Figure 2. (a) Cross-section of a T-gate after lift-off. (b) HF etches the Ti layer in the gate making it mechanically unstable. (c) A spacer layer using an appropriate material can be used to protect the delicate neck of the T-gate while providing some additional mechanical support.

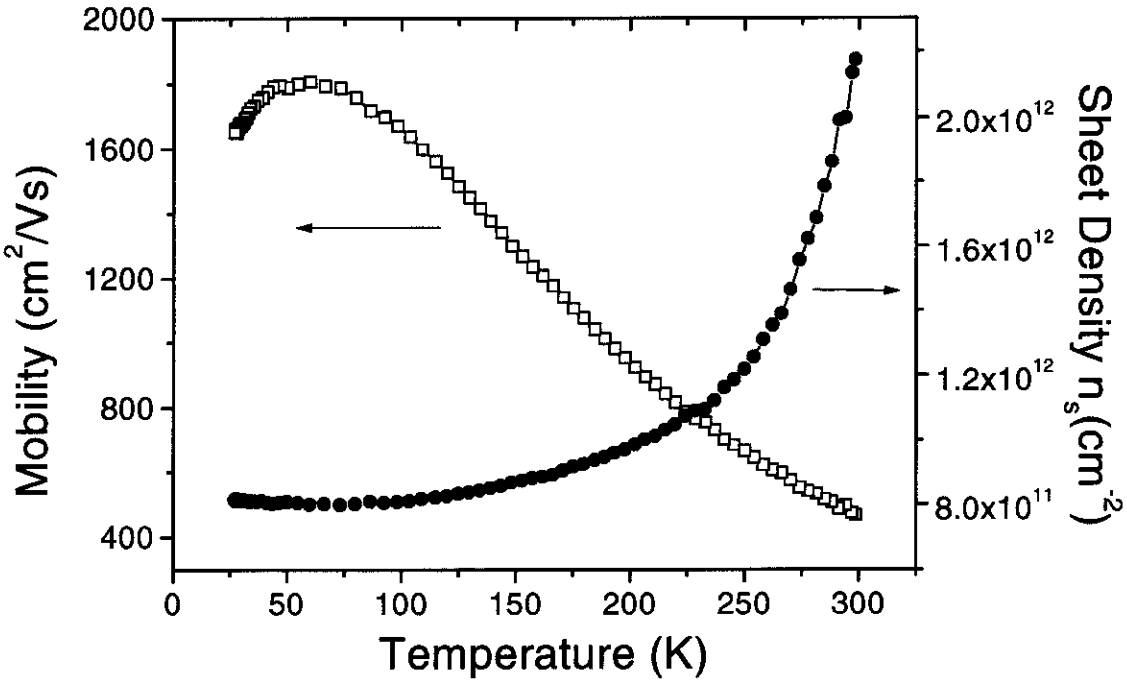

Figure 3. Hall effect results from a p-MODFET wafer (Govt61.10).